



GM72V66441ET/ELT

4,194,304 WORD x 4 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

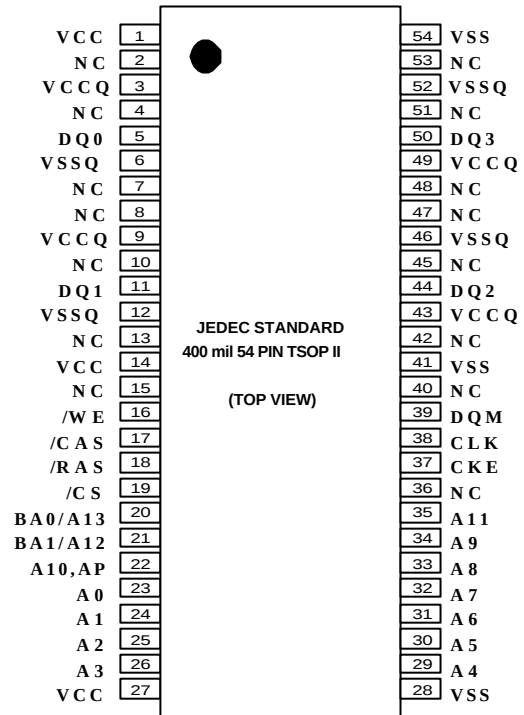
The GM72V66441ET/ELT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logic including input and output circuits operating synchronously by referring to the positive edge of the externally provided Clock.

The GM72V66441ET/ELT provides four banks of 4,194,304 word by 4 bit to realize high bandwidth with the Clock frequency up to 143 Mhz.

Features

- * PC133/PC100/PC66 Compatible
 - 7(143MHz)/-75(133MHz)/-8(125MHz)
 - 7K(PC100,2-2-2)/-7J(PC100,3-2-2)
- * 3.3V single Power supply
- * LVTTL interface
- * Max Clock frequency
143/133/125/100MHz
- * 4,096 refresh cycle per 64 ms
- * Two kinds of refresh operation
Auto refresh / Self refresh
- * Programmable burst access capability ;
 - Sequence: Sequential / Interleave
 - Length : 1/2/4/8/FP
- * Programmable CAS latency : 2/3
- * 4 Banks can operate independently or simultaneously
- * Burst read/burst write or burst read/single write operation capability
- * Input and output masking by DQM input
- * One Clock of back to back read or write command interval
- * Synchronous Power down and Clock suspend capability with one Clock latency for both entry and exit
- * JEDEC Standard 54Pin 400mil TSOP II Package

Pin Configuration



Pin Name

CLK	Clock
CKE	Clock Enable
CS	Chip Select
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A13	Bank select
~BA1/A12	
DQ0~DQ7	Data input / Data output
DQM	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Ground for internal circuit
NC	No Connection

The diagram illustrates a 4-bank memory architecture. At the top, address lines A0 to A13 are connected to a Column address buffer and a Row address counter. The Column address buffer also receives A0 to A9 and outputs to a Column address counter. The Row address counter also receives A0 to A13 and outputs to a Refresh counter. The Column address counter and Row address counter are connected to a common bus that feeds into the Column decoder and Row decoder of each of the four memory banks (Bank 0 to Bank 3). Each bank contains a Memory array (4096 row x 1024 column x 4 bit), a Row decoder, and a Column decoder/Sense amplifier & I/O bus. The Column decoder/Sense amplifier & I/O bus is connected to a common data bus that leads to an Input buffer and an Output buffer. The Input buffer and Output buffer are connected to a DQ0 to DQ3 data bus. A Control logic & timing generator provides signals: CLK, CKE, CS, RAS, CAS, WE, and DQM.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V _{SS}	V _T	-0.5 to V _{CC} +0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to V _{SS}	V _{CC}	-0.5 to +4.6	V	1
Short circuit output current	I _{OUT}	50	mA	
Power dissipation	P _T	1.0	W	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +125	°C	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (T_a = 0 to + 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V _{CC} , V _{CCQ}	3.0	3.6	V	1
	V _{SS} , V _{SSQ}	0	0	V	
Input high voltage	V _{IH}	2.0	V _{CC} +0.3	V	1, 2
Input low voltage	V _{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.6V for pulse width ≤ 3ns

3. V_{IL} (min) = -2.0V for pulse width ≤ 3ns

DC Characteristics (Ta = 0 to 70C, VCC, VCCQ = 3.3 V +/- 0.3 V, VSS, VSSQ = 0 V)

Parameter		Symbol	- 7	- 75	- 8	-7K	-7J	Unit	Test conditions	Notes
			Max	Max	Max	Max	Max			
Operating current		ICC1	85	85	80	80	80	mA	Burst length= 1 t _{RC} = min	1, 2, 3
Standby current in power down		ICC2P	2					mA	CKE = V _{IL} , t _{CK} = 12 ns	5
Standby current in power down (input signal stable)		ICC2PS	2					mA	CKE=V _{IL} , t _{CK} = infinity	6
			0.4							6,8
Standby current in non power down (CAS Latency=2)		ICC2N	15					mA	CKE,CS = V _{IH} , t _{CK} = 12ns	4
Standby current in non power down (input signal stable)		ICC2NS	12					mA	CKE = V _{IH} , t _{CK} = infinity	4
Active standby current in power down		ICC3P	6					mA	CKE = V _{IL} , t _{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		ICC3PS	5					mA	CKE = V _{IL} , t _{CK} = infinity	2,6
Active standby current in non power down		ICC3N	30					mA	CKE,CS = V _{IH} , t _{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		ICC3NS	20					mA	CKE = V _{IH} , t _{CK} = infinity	2,9
Burst operating current	(CL= 2)	ICC4	120					mA	t _{CK} = min BL = 4	1,2,3
	(CL= 3)	ICC4	150	150	150	120	120	mA		
Refresh current		ICC5	160					mA	t _{RC} = min	3
Self refresh current		ICC6	1					mA	V _{IH} >=V _{CC} - 0.2 V _{IL} <=0.2V	7
			0.4							7,8

DC Characteristics ($T_a = 0$ to 70°C , V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, V_{SS} , $V_{SSQ} = 0\text{ V}$)
(Continued)

Parameter	Symbol	- 7, -75, - 8, - 7K, - 7J		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	-1.5	1.5	μA	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	$I_{OH} = -2\text{ mA}$	
Output low voltage	V_{OL}	-	0.4	V	$I_{OL} = 2\text{ mA}$	

- Notes :
1. I_{CC} depends on output load condition when the device is selected. $I_{CC}(\text{max})$ is specified at the output open condition.
 2. One bank operation.
 3. Addresses are changed once per one cycle.
 4. Addresses are changed once per two cycles.
 5. After Power down mode, CLK operating current.
 6. After Power down mode, no CLK operating current.
 7. After self refresh mode set, self refresh current.
 8. L-Version.
 9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($T_a = 25^\circ\text{C}$, V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Min.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	2.5	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	2.5	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	4.0	6.5	pF	1, 2, 3, 4

- Notes :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. DQM = V_{IH} to disable Dout.
 3. This parameter is sampled and not 100% tested.
 4. Measured with 1.4 V bias and 200mV swing at the pin under measurement.

AC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC}, V_{CCQ} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS}, V_{SSQ} = 0 \text{ V}$)

Parameter		Symbol	- 7		- 75		- 8		- 7K		- 7J		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	10	-	10	-	10	-	10	-	15	-	ns	1
	(CL=3)	t_{CK}	7	-	7.5	-	8	-	10	-	10	-		
CLK high pulse width		t_{CKH}	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	6	-	6	-	6	-	6	-	8	ns	1, 2
	(CL=3)	t_{AC}	-	5.4	-	5.4	-	6	-	6	-	6		
Data-out hold time		t_{OH}	2.7	-	2.7	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t_{LZ}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2,3)		t_{HZ}	-	5.4	-	5.4	-	6	-	6	-	6	ns	1, 4
Data-in setup time		t_{DS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	62	-	65	-	68	-	70	-	70	-	ns	1
Active to Precharge command period		t_{RAS}	42	120000	45	120000	48	120000	50	120000	50	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	20	-	20	-	20	-	20	-	ns	1
Precharge to active command period		t_{RP}	20	-	20	-	20	-	20	-	20	-	ns	1

AC Characteristics ($T_a = 0$ to 70°C , $V_{CC}, V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS}, V_{SSQ} = 0\text{ V}$)
(Continued)

Parameter	Symbol	- 7		- 75		- 8		- 7K		- 7J		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	7	-	7.5	-	8	-	10	-	10	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	15	-	16	-	20	-	20	-	ns	1
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes $t_r = 1\text{ ns}$. Reference level for timing of input signals is 1.40V.

If t_r is longer than 1ns, transition time compensation should be considered.

2. Access time is measured at 1.40V. Load condition is $C_L = 50\text{ pF}$ without termination.

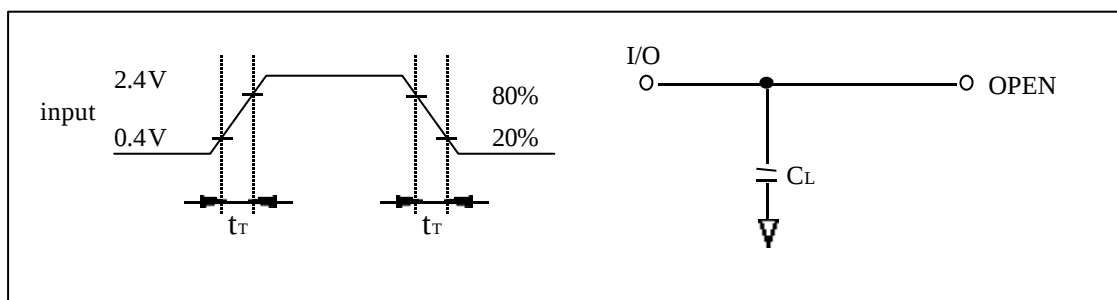
3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except Power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-75		-8		-7K		-7J		Notes
frequency(MHz)			143	100	133	100	125	100	100	100	100	66	
t _{CK} (ns)			7	10	7.5	10	8	10	10	10	10	15	
Active command to column command (same bank)		I _{RCD}	3	2	3	2	3	2	2	2	2	2	1
Active command to active command (same bank)		I _{RC}	9	7	9	7	9	7	7	7	7	6	= [I _{RAS} + I _{RP}], 1
Active command to Precharge command (same bank)		I _{RAS}	6	5	6	5	6	5	5	5	5	4	1
Precharge command to active command (same bank)		I _{RP}	3	2	3	2	3	2	2	2	2	2	1
Write recovery or last data-in to Precharge command (same bank)		I _{RWL}	1	1	1	1	1	1	1	1	1	1	1
Active command to active command (different bank)		I _{RRD}	2	2	2	2	2	2	2	2	2	2	1
Self refresh exit time		I _{SREX}	1	1	1	1	1	2	1	1	1	2	
Last data in to active command (Auto Precharge, same bank)		I _{APW}	4	3	4	3	4	3	3	3	3	3	= [I _{RWL} + I _{RP}], 1
Self refresh exit to command input		I _{SEC}	9	7	9	7	9	7	7	7	7	6	= [I _{RC}]
Precharge command to high impedance	(CL=2)	I _{HZP}	-	2	-	2	-	2	2	2	-	2	
	(CL=3)	I _{HZP}	3	3	3	3	3	3	3	3	3	3	
Last data out to active command (auto Precharge) (same bank)		I _{APR}	1	1	1	1	1	1	1	1	1	1	
Last data out to Precharge (early Precharge)	(CL=2)	I _{EP}	-	-1	-	-1	-	-1	-1	-1	-	-1	
	(CL=3)	I _{EP}	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	
Column command to column command		I _{CCD}	1	1	1	1	1	1	1	1	1	1	
Write command to data in latency		I _{WCD}	0	0	0	0	0	0	0	0	0	0	
DQM to data in		I _{DID}	0	0	0	0	0	0	0	0	0	0	
DQM to data out		I _{DOD}	2	2	2	2	2	2	2	2	2	2	
CKE to CLK disable		I _{CLE}	1	1	1	1	1	1	1	1	1	1	
Register set to active command		I _{RSA}	1	1	1	1	1	1	1	1	1	1	
CS̄ to command disable		I _{CDD}	0	0	0	0	0	0	0	0	0	0	
Power down exit to command input		I _{PEC}	1	1	1	1	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-75		- 8		- 7K		- 7J		Notes
frequency(MHz)			143	100	133	100	125	100	100	100	100	66	
t _{CK} (ns)			7	10	7.5	10	8	10	10	10	10	15	
Burst stop to output valid data hold	(CL=2)	I _{BSR}	-	1	-	1	-	1	1	1	-	1	
	(CL=3)	I _{BSR}	2	2	2	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	I _{BSH}	-	2	-	2	-	2	2	2	-	2	
	(CL=3)	I _{BSH}	3	3	3	3	3	3	3	3	3	3	
Burst stop to write data ignore		I _{BSW}	0	0	0	0	0	0	0	0	0	0	

Notes : 1. I_{RCD} to I_{RRD} are recommended value.

Package Dimensions

GM72V66441ET/ELT Series (TTP-54D)

