FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16616-1E

32-bit Microcontroller

CMOS

FR60 MB91460H Series

MB91F464HB

DESCRIPTION

MB91460H series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family* of CPUs.

This series contains the LIN-USART and CAN controllers.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Microelectronics Limited.

FEATURES

1. FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)

32-bit multiplication: 5 cycles
16-bit multiplication: 3 cycles
ts (save PC/PS) : 6 cycles (16 priority levels)
d architecture enabling program access and data access to be performed simultaneously
ions compatible with the FR family

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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2. Internal peripheral resources

- General-purpose ports : Maximum 108 ports
- DMAC (DMA Controller)
  Maximum of 5 channels able to operate simultaneously
  2 transfer sources (internal peripheral/software)
  Activation source can be selected using software
  Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  Transfer data size selectable from 8/16/32-bit
  Multi-byte transfer enabled (by software)
  DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  10-bit resolution: maximum 32 channels
  Conversion time: minimum 1 µs
- External interrupt inputs : maximum 16 channels
  3 channels shared with CAN RX or I^2C pins
- Bit search module (for REALOS)
  Function to search the first bit position of ‘’1”, ‘’0”, ‘’changed” from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 4 or 7 channels
  Clock synchronous/asynchronous selectable
  Sync-break detection
  Internal dedicated baud rate generator
- I^2C bus interface (supports 400 kbps): 2 channels
  Master/slave transmission and reception
  Arbitration function, clock synchronization function
- CAN controller (C-CAN): 1 channel
  Maximum transfer speed: 1 Mbps
  32 transmission/reception message buffers
- Sound generator : 1 channel
  Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  Monitor external voltage
  Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : maximum 16 channels
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: maximum 8 channels (operates in conjunction with the free-run timer)
- Output compare: maximum 8 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 2 channels (2*8-bit or 1*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit

(Continued)

(Continued)

- Clock supervisor
  Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration
  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

3. Package and technology

- Package : QFP-144
- CMOS 180 nm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between - 40°C and + 105°C

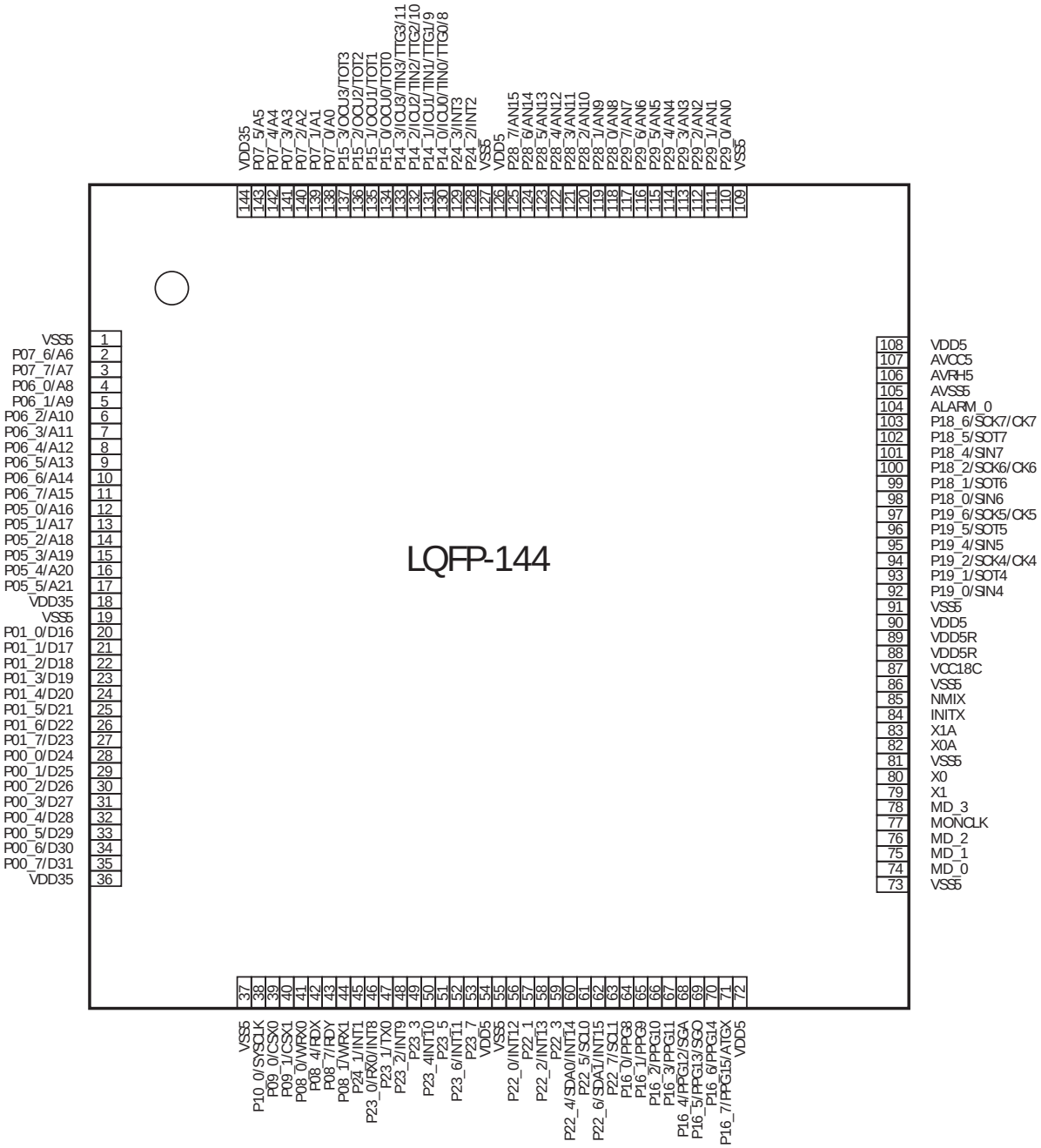
PRODUCT LINEUP

Feature	MB91FV460B	MB91F464HB
Max. core frequency (CLKB)	100 MHz	100 MHz
Max. resource frequency (CLKP)	50 MHz	50 MHz
Max. external bus frequency (CLKT)	50 MHz	50 MHz
Max. CAN frequency (CLKCAN)	50 MHz	50 MHz
Technology	0.18µm	0.18µm
Watchdog	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Clock Modulator	yes	yes
Clock Monitor	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MMU/MPU	MPU (16 ch)*1	MPU (8 ch)*1
Flash memory	Internal Flash memory 2112KB + external emulation SRAM with 64bit read data	416 KByte
Flash Protection	yes	yes
D-RAM	64 KByte	24 KByte
ID-RAM	64 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte
Boot-ROM / BI-ROM	16 KByte Boot Flash + 1KB Boot ROM	4 KByte
RTC	1 ch	1 ch
Free Running Timer	12 ch	8 ch*2
ICU	10 ch	MD_3=0: 8 ch MD_3=1: 4 ch*3
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch*4
Reload Timer	16 ch	8 ch*5
PPG 16-bit	32 ch	MD_3=0: 16 ch MD_3=1: 8 ch*6
Sound Generator	1 ch (old) + 1 ch (new)	1 ch (old)
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA*7
C_CAN	6 ch (128msg)	1 ch (32msg)
LIN-USART	16 ch (FIFO)	MD_3=0: 3 ch + 4 ch FIFO*8 MD_3=1: 4 ch FIFO
I^2C (400K)	8 ch	2 ch
FR external bus	yes (32bit addr, 32bit data)	MD_3=0: no MD_3=1: yes (22bit addr, 16bit data)

PIN ASSIGNMENT

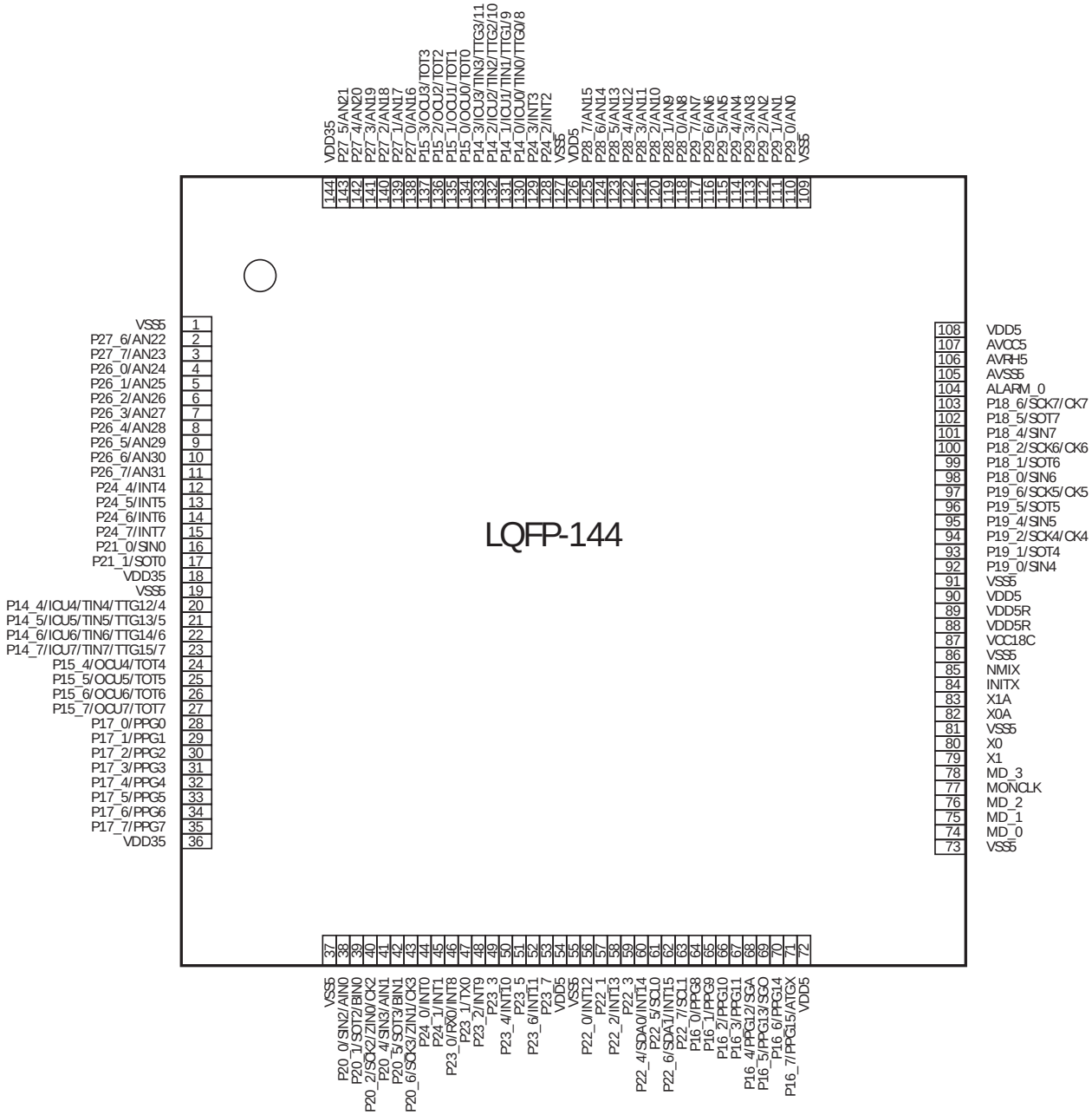
1. MB91F464HB with MD_3=1

(TOP VIEW)



2. MB91F46HB with MD_3=0

(TOP VIEW)



PIN DESCRIPTION

1. MB91F464HB with MD_3=1

Pin no.	Pin name	I/O	I/O circuit type*	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

Pin no.	Pin name	I/O	I/O circuit type*	Function
69	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output port
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pin
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6

[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

2. MB91F464HB with MD_3=0

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin

Pin no.	Pin name	I/O	I/O circuit type*	Function
63	P22_7	I/O	C	General-purpose input/output ports
	SCL1			I^2C bus clock input/output pin (open drain)
64 to 67	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
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82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5

Pin no.	Pin name	I/O	I/O circuit type*	Function
97	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output ports
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output ports
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output ports
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P27_0 to P27_5	I/O	B	General-purpose input/output ports
	AN16 to AN21			Analog input pins of A/D converter

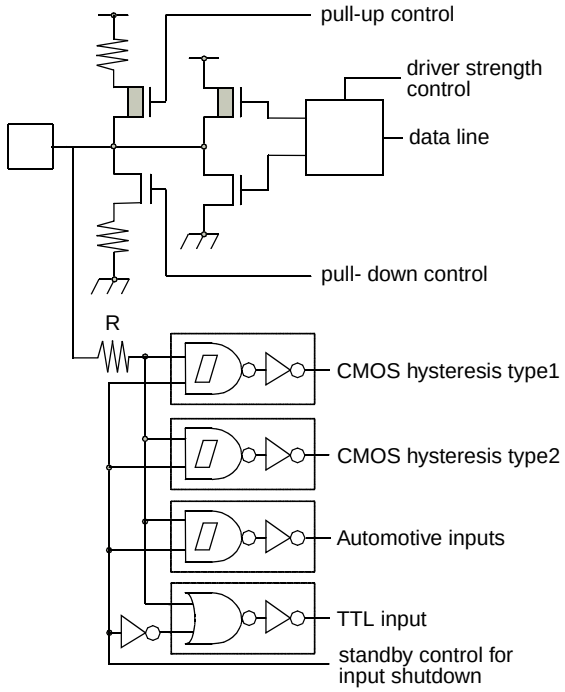
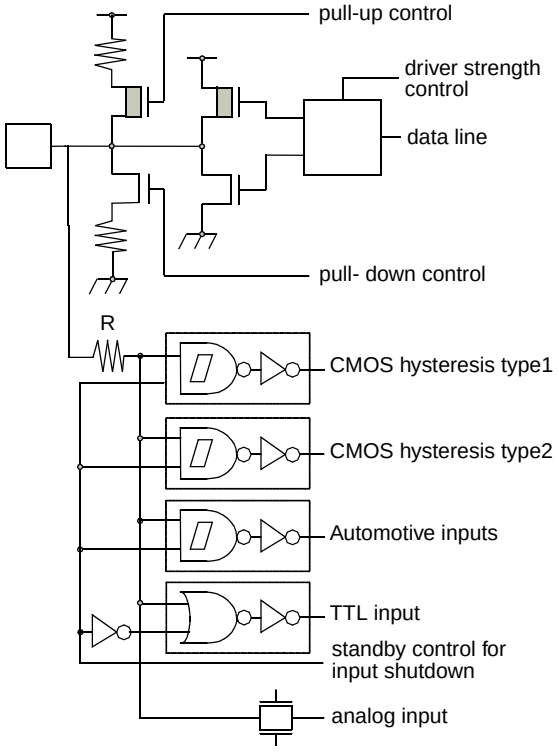
* : For information about the I/O circuit type, refer to “ I/O CIRCUIT TYPES”.

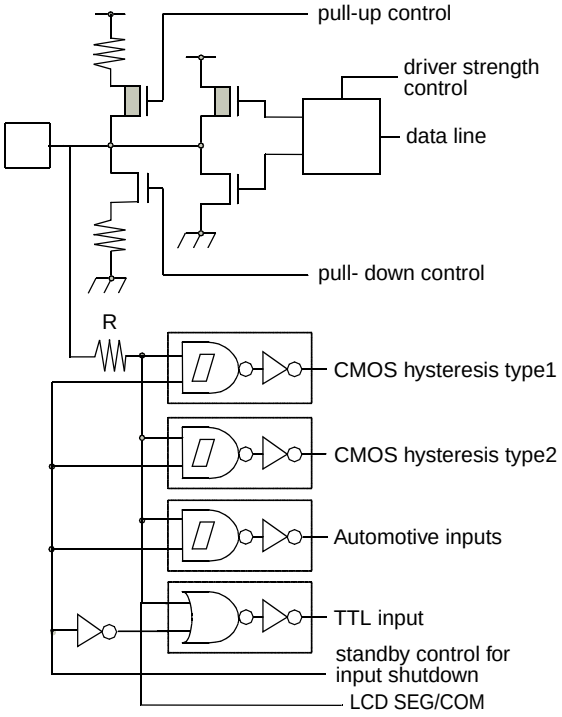
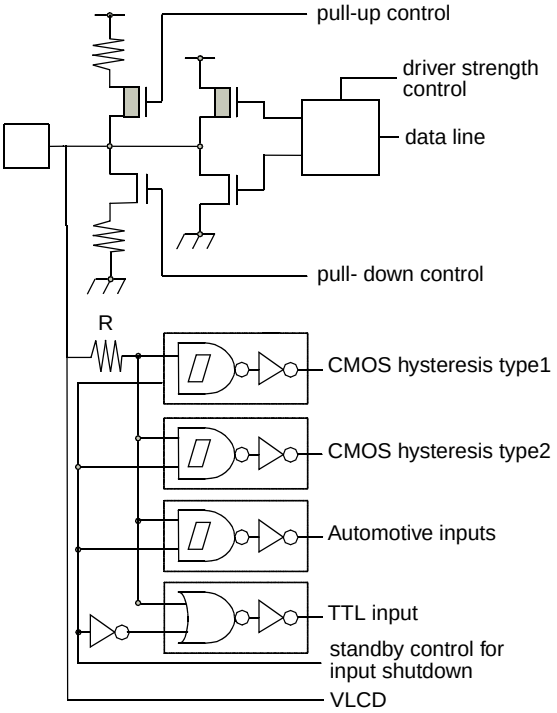
[Power supply/Ground pins]

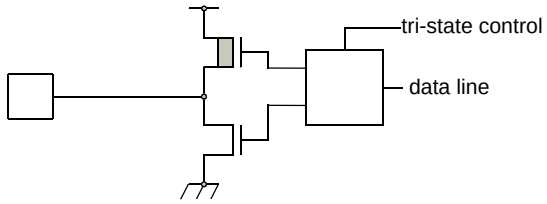
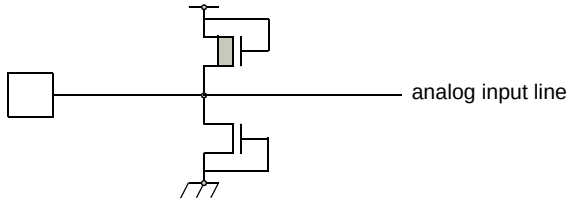
Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

* : For information about the I/O circuit type, refer to “ I/O CIRCUIT TYPES”.

I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

HANDLING DEVICES

1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

3. Power supply pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

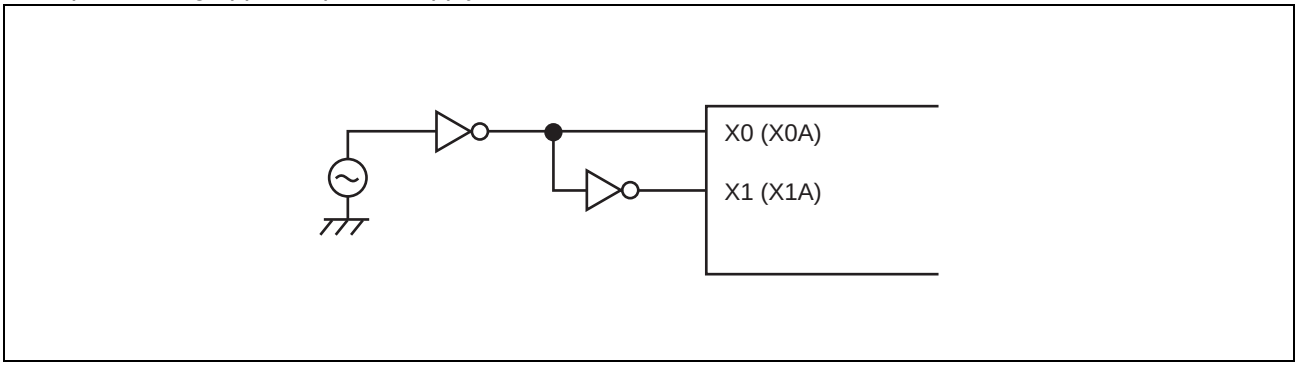
5. Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

(Continued)

(Continued)

Example of using opposite phase supply



6. Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

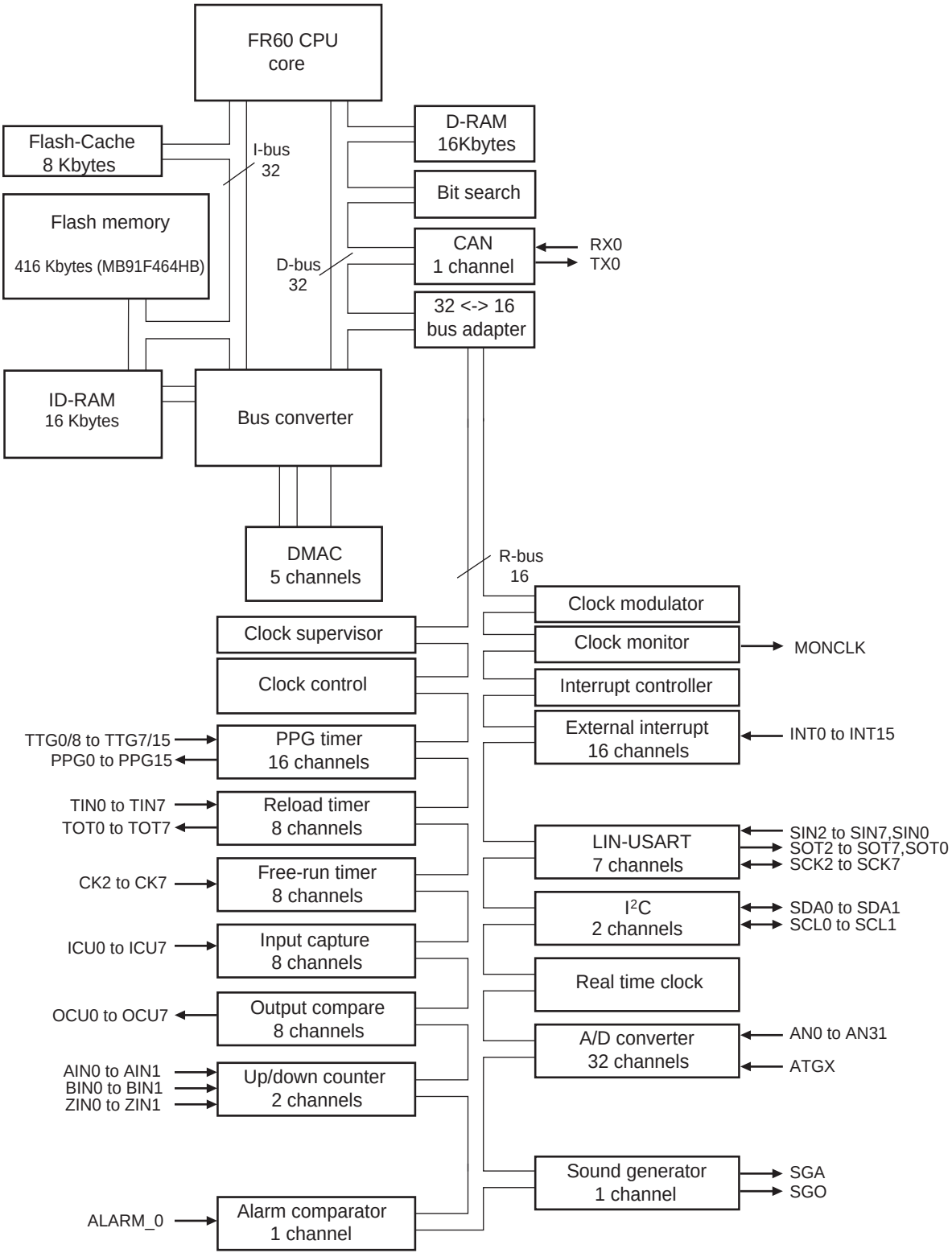
7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

2. MB91F464HB with MD_3=0



CPU AND CONTROL UNIT

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

1. Features

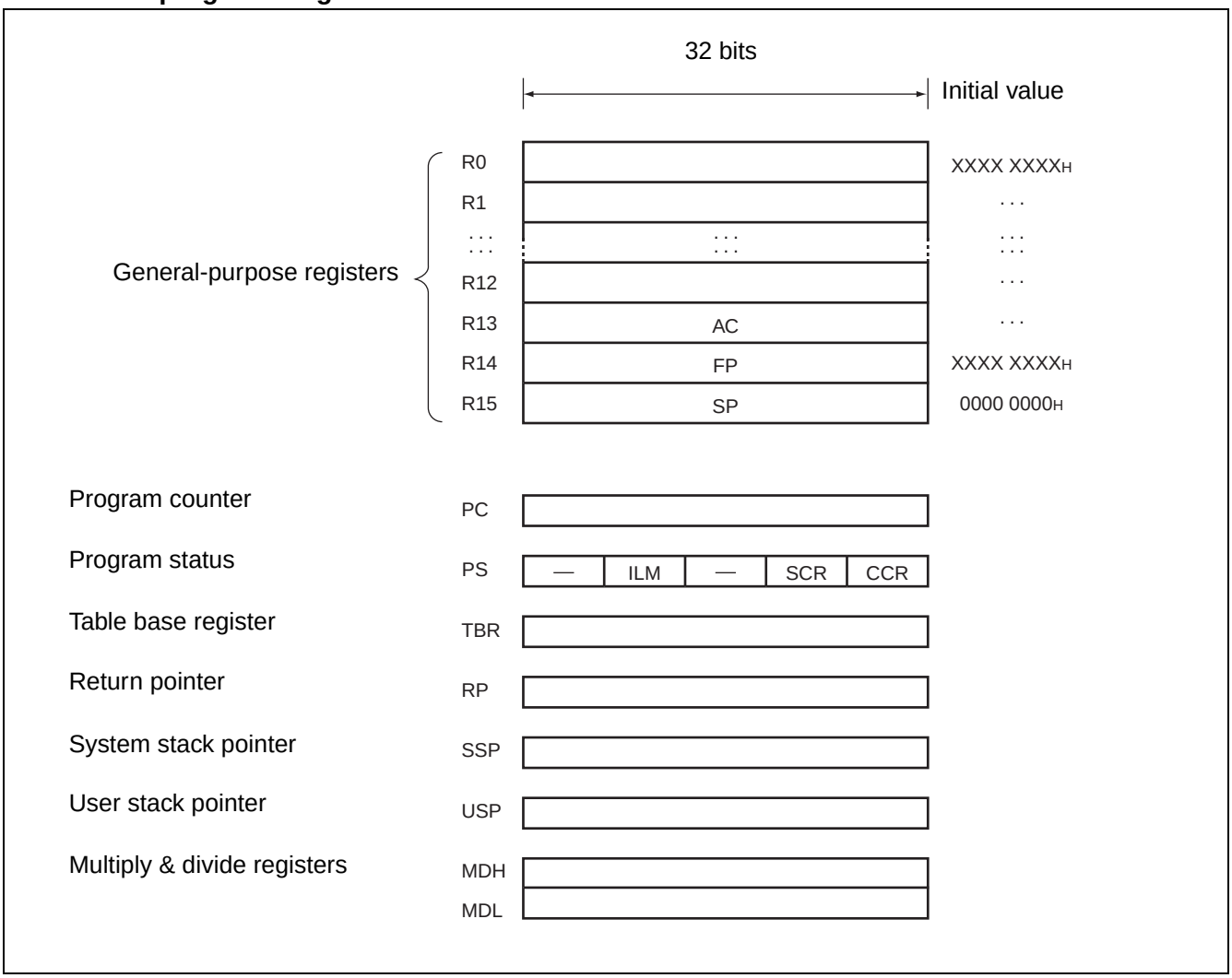
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

2. Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

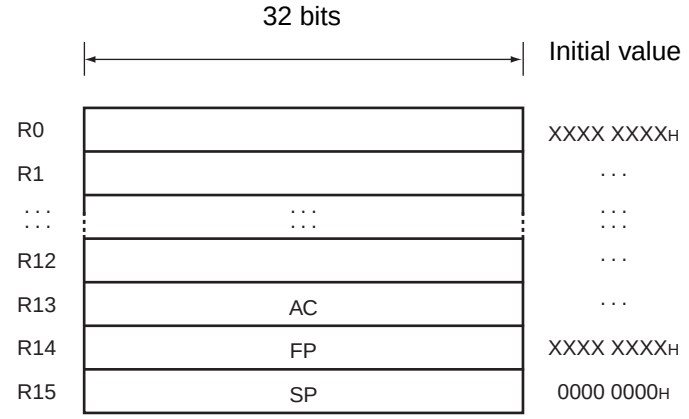
3. Programming model

3.1. Basic programming model



4. Registers

4.1. General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

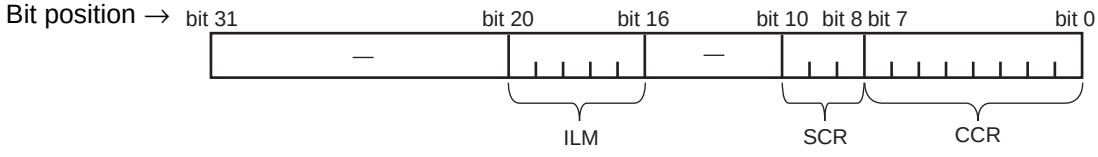
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

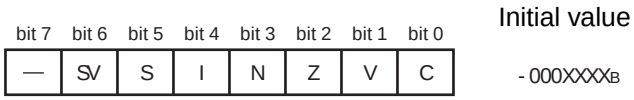
4.2. PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.

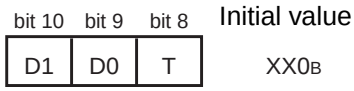


4.3. CCR (Condition Code Register)



SV : Supervisor flag
S : Stack flag
I : Interrupt enable flag
N : Negative enable flag
Z : Zero flag
V : Overflow flag
C : Carry flag

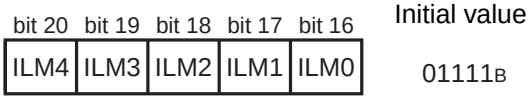
4.4. SCR (System Condition Register)



Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

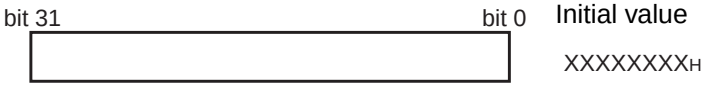
4.5. ILM (Interrupt Level Mask register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111_B” at reset.

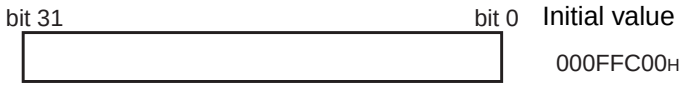
4.6. PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

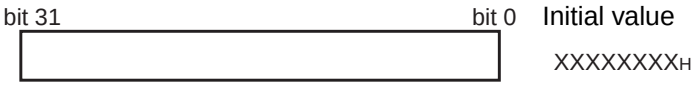
4.7. TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

4.8. RP (Return Pointer)



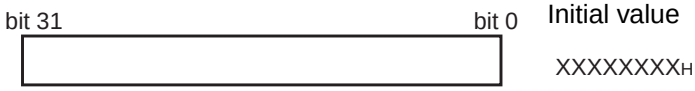
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

4.9. USP (User Stack Pointer)



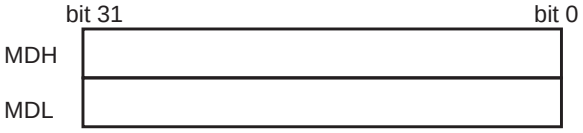
The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.

  The initial value at reset is undefined.

- This register cannot be used with RETI instructions.

4.10. Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

3.2. Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

3.2.1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	

3.2.2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	

3.3. Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

3.3.1. Address mapping MB91F464HB

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

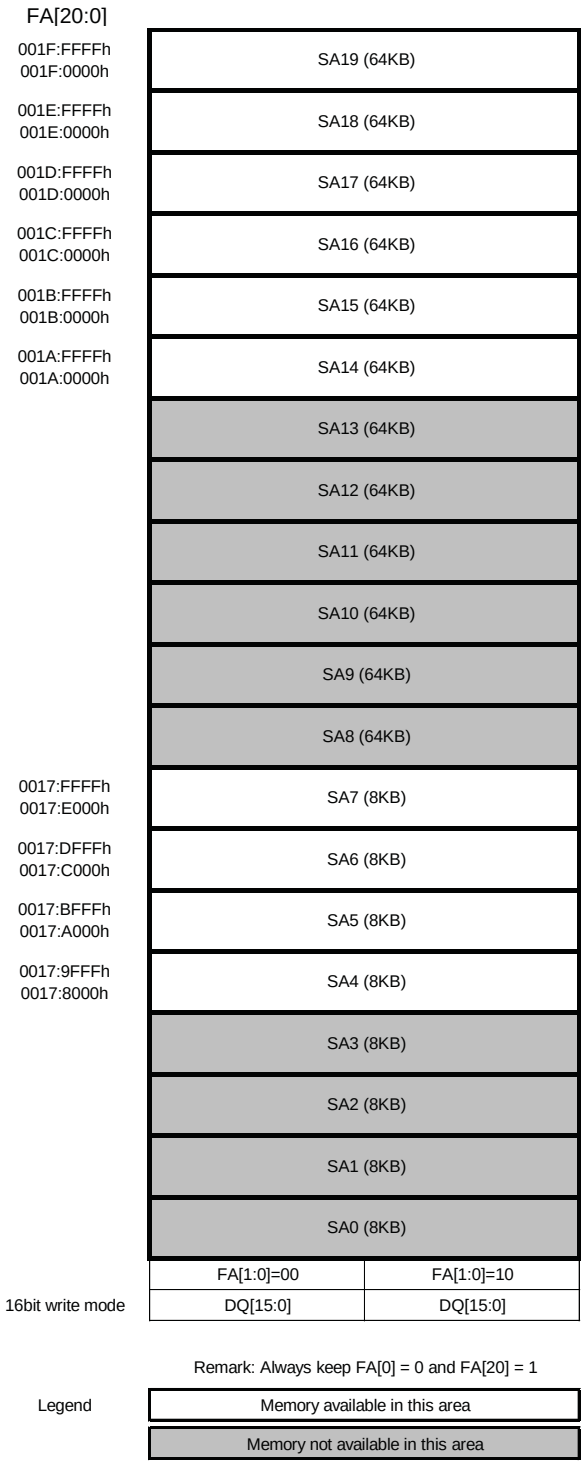
Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

4. Parallel Flash programming mode

4.1. Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F464HB



Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend	
	Memory available in this area
	Memory not available in this area

4.2. Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F464HB external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to ‘1’
-	-	MD1	MD1	75	Set to ‘1’
-	-	MD0	MD0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to ‘H’	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to ‘0’
-		EQIN	GP18_5	102	Set to ‘0’
-		TESTX	GP16_5	69	Set to ‘1’
-		RDYI	GP18_4	101	Set to ‘0’
A-1	Internal address bus	FA0	GP05_5	17	Set to ‘0’
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A18		FA17 to FA19	GP05_0 to GP05_2	12 to 14	
A19		FA20	GP05_3	15	Set to ‘1’
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

5. Poweron Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

6. Flash Security

6.1. Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

6.2. Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

6.2.1. FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to ‘0’	set to ‘0’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘0’	Write Protection (all device modes, without exception)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes)
set all to ‘0’	set to ‘1’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘0’	Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”)

6.2.2. FSV1 (bit15 to bit0) MB91F464HB

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[3:0]	—	—	—	not available
FSV1[4]	SA4	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[15:8]	—	—	—	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

6.3. Security Vector FSV2 MB91F464HB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[5:0]	—	—	—	not available
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	—	—	—	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

MEMORY SPACE

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to $0FF_H$

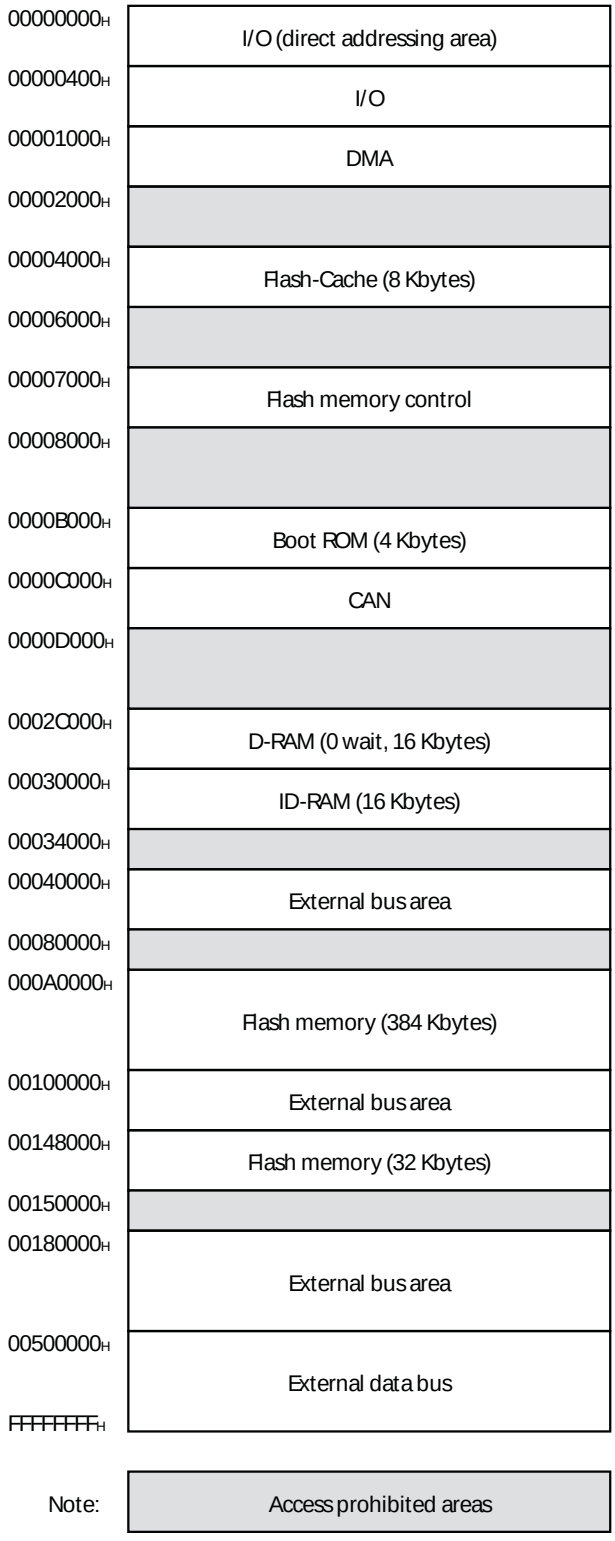
Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

MEMORY MAPS

1. MB91F464HB

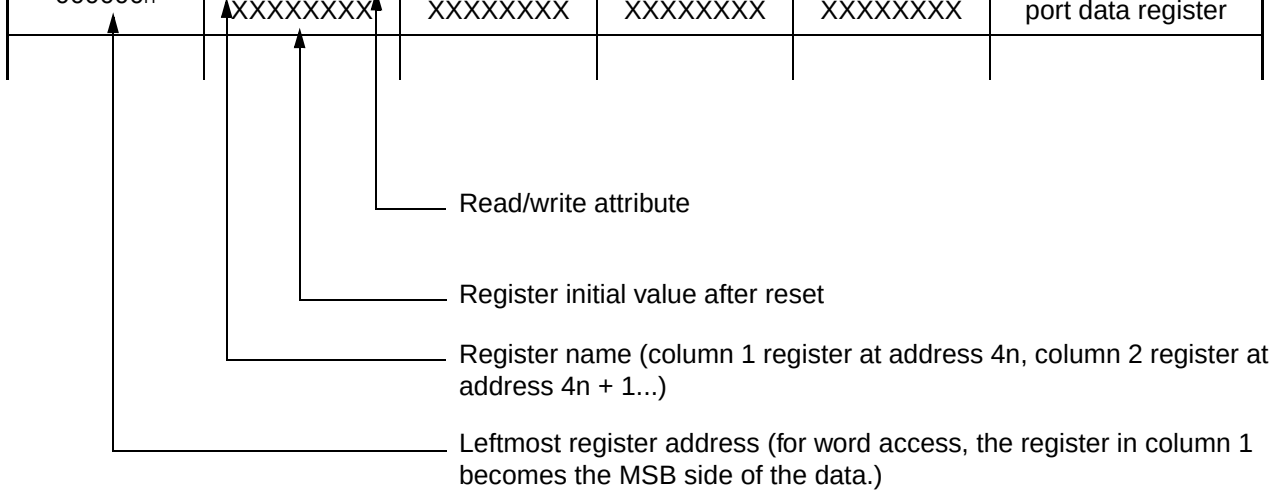
MB91F464HB



I/O MAP

1. MB91F464HB

Address	Register				Block
	+ **0**	+ **1**	+ **2**	+ **3**	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:
- " 1 " : Initial value " 1 "
- " 0 " : Initial value " 0 "
- " X " : Initial value " undefined "
- " - " : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004H	Reserved	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008H	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	Reserved	
00000CH	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
00001CH	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020H to 00002CH	Reserved				
000030H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC		Delay interrupt
00003CH	Reserved				Reserved
000040H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048H 00004CH	Reserved				Reserved
000050H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000058H	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005CH	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		
000060H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006CH	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007CH	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	Reserved	Reserved	Baud rate Generator LIN-USART 0 to 7
000084H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008CH	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090H to 0000CCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
0000D0H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I²C 0
0000D4H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	
0000DCH	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I²C 1
0000E0H	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
0000E4H	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	
0000E8H to 0000FCH	Reserved				Reserved
000100H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011CH	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
00012CH	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000138H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013CH	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015CH	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016CH	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170H to 00017CH	Reserved				Reserved
000180H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
00018CH	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019CH	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
0001ACH	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	Alarm Comparator 0 to 1
0001B0H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4H	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BCH	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4H	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
0001C8H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CCH	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4H	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
0001D8H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DCH	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0H	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4H	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001ECH	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FCH	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] 00 - - 0000	Reserved			
000244H to 0002CCH	Reserved				Reserved
0002D0H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DCH	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		OCS67 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 4 to 7
0002E0H	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
0002E4H	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
0002E8H to 0002ECH	Reserved				Reserved
0002F0H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
0002F4H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4, OCU 5)
0002FCH	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6, OCU 7)

Address	Register				Block
	+0	+1	+2	+3	
000300H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
00030CH to 00031CH	Reserved				Reserved
000320H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324H to 00032CH	Reserved				Reserved
000330H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033CH	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034CH	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350H to 00038CH	Reserved				Reserved
000390H	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394H to 0003ECH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34[R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	

Address	Register				Block
	+0	+1	+2	+3	
00047C$_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480$_H$	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484$_H$	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488$_H$	Reserved				Reserved
00048C$_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Interface
000490$_H$	PLLCTRL [R/W] - - - - 0000	Reserved			
000494$_H$	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)
000498$_H$	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
0004A0$_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4$_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8$_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
0004AC$_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] - 011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor /Selector/ Monitor
0004B0$_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4$_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
0004B8$_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
0004BC$_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0$_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - 000000	Reserved		CAN Clock Control
0004C4$_H$	LVSEL [R/W] 00000111	LVDET [R/W] 00000 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8$_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 001	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer

Address	Register				Block
	+0	+1	+2	+3	
0004CC$_H$	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control / Main/Sub Regulator Control
0004D0$_H$ to 00063C$_H$	Reserved				Reserved
000640$_H$	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000*2		External Bus Unit
000644$_H$	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648$_H$	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064C$_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650$_H$	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654$_H$	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658$_H$	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065C$_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660$_H$	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664$_H$	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668$_H$	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066C$_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670$_H$	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674$_H$	Reserved				
000678$_H$	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C$_H$	Reserved				
000680$_H$	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *3	
000684$_H$	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000688H to 0007F8H	Reserved				External Bus Unit
0007FCH	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800H to 000CFCH	Reserved				Reserved
000D00H	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
000D04H	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08H	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
000D0CH	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
000D10H	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14H	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
000D18H	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1CH	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
000D20H to 000D3CH	Reserved				
000D40H	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
000D44H	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48H	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - -0	Reserved	
000D4CH	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
000D50H	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54H	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
000D58H	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5CH	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000D60H to 000D7CH	Reserved				Reserved
000D80H	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		R-bus Port Function Register
000D84H	Reserved	PFR05 [R/W] - - 111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88H	PFR08 [R/W] 1 - - 1 - - 11	PFR09 [R/W] - - - - - - 11	PFR10 [R/W] - - - - - - -1	Reserved	
000D8CH	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
000D90H	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94H	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - - - - - - 00	PFR22 [R/W] 0000-0-0	PFR23 [R/W] -0000000	
000D98H	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9CH	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
000DA0H to 000DC4H	Reserved				
000DC8H	Reserved		EPFR10 [R/W] - - - - - - - 0	Reserved	R-bus Port Extra Function Register
000DCCH	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
000DD0H	EPFR16 [R/W] 0 - 00 - - - -	Reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
000DD4H	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - - - - - - - - -	Reserved		
000DD8H	Reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDCH to 000DFCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000E00H	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
000E04H	Reserved	PODR05 [R/W] - - 000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08H	PODR08 [R/W] 0 - - 0 - - - 0	PODR09 [R/W] - - - - - - 00	PODR10 [R/W] - - - - - - - 0	Reserved	
000E0CH	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
000E10H	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14H	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - - - - - - 00	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
000E18H	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1CH	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
000E20H to 000E3CH	Reserved				Reserved
000E40H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
000E44H	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48H	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - - 00	PILR10 [R/W] - - - - - - - 0	Reserved	
000E4CH	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
000E50H	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - - 000	PILR19 [R/W] - 000 - 000	
000E54H	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
000E58H	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5CH	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
000E60H to 000E7CH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000E80H	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
000E84H	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88H	EPILR08 [R/W] 0 - - 0- - - 0	EPILR09 [R/W] - - - - - - 00	EPILR10 [R/W] - - - - - - - 0	Reserved	
000E8CH	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
000E90H	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - - 000	EPILR19 [R/W] - 000 - 000	
000E94H	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
000E98H	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9CH	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
000EA0H to 000EBCH	Reserved				Reserved
000EC0H	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
000EC4H	Reserved	PPER05 [R/W] - - 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8H	PPER08 [R/W] 0 - - 0 - - - 0	PPER09 [R/W] - - - - - - 00	PPER10 [R/W] - - - - - - - 0	Reserved	
000ECCH	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
000ED0H	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
000ED4H	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - - - - - - 00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
000ED8H	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDCH	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
000EE0H to 000EFCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000F00H	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
000F04H	Reserved	PPCR05 [R/W] - - 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08H	PPCR08 [R/W] 1 - - 1 - - - 1	PPCR09 [R/W] - - - - - - 11	PPCR10 [R/W] - - - - - - - 1	Reserved	
000F0CH	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
000F10H	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
000F14H	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] - - - - - - 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
000F18H	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
000F1CH	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
000F20H to 000F3CH	Reserved				Reserved
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 003FFCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
002000H to 006FFCH	Flash-cache size is 8 Kbytes : 004000H to 005FFCH				Flash-cache / I-RAM area
007000H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008H	FMAC [R] 00000000 00000000 00000000 00000000				
00700CH	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cache-able area setting Register
007010H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014H to 007FFCH	Reserved				Reserved
008000H to 00BFFCH	Boot-ROM size is 4 Kbytes : 00B000H to 00BFFCH (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000H	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
00C004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008H	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00CH	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

Address	Register				Block
	+0	+1	+2	+3	
00C010H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01CH	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
00C024H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028H to 00C02CH	Reserved				
00C030H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038H to 00C03CH	Reserved				
00C040H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
00C04CH	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058H to 00C05CH	Reserved				
00C060H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068H to 00C07CH	Reserved				
00C080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
00C084H to 00C08CH	Reserved		Reserved		
00C090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094H to 00C09CH	Reserved		Reserved		
00C0A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4H to 00C0ACH	Reserved		Reserved		
00C0B0H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4H to 00C0FCH	Reserved		Reserved		
00C100H to 00EFFCH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
00F000H	BCTRL [R/W] - - - - - - - - - - - - - - - - 11111100 00000000				EDSU / MPU
00F004H	BSTAT [R/W] - 000 00000000 10 - - 000000				
00F008H	BIAC [R] - - - - - - - - - - - - - - - - 00000000 00000000				
00F00CH	BOAC [R] - - - - - - - - - - - - - - - - 00000000 00000000				
00F010H	BIRQ [R/W] - - - - - - - - - - - - - - - - 00000000 00000000				
00F014H to 00F01CH	Reserved				
00F020H	BCR0 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F024H	BCR1 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F028H	BCR2 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F02CH	BCR3 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F030H to 00F07CH	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
00F080H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08CH	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F09CH	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0H	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4H	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8H	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0ACH	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0H	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4H	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8H	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BCH	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0H to 01FFFCH	Reserved				EDSU / MPU
020000H to 02FFFCH	D-RAM size is 16 Kbytes : 02C000H - 02FFFCH (data access is 0 wait cycles)				D-RAM area
030000H to 03FFFCH	ID-RAM size is 16 Kbytes : 030000H - 033FFCH (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

*1 : depends on the number of available CAN channels

*2 : ACR0 [11 : 10] depends on Mode vector fetch information on bus width

*3 : TCR [3 : 0] INIT value = 0000, keeps value after RST

2. Flash memory and external bus area

2.1. MB91F464HB

32bit read	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000H to 05FFF8H	Reserved				Reserved				ROMS0
060000H to 07FFF8H	Reserved				Reserved				ROMS1
080000H to 09FFF8H	Reserved				Reserved				ROMS2
0A0000H to 0BFFF8H	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000H to 0DFFF8H	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000H to 0FFFF0H	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8H	FMV [R] 06 00 00 00H				FRV [R] 00 00 BF F8H				
100000H to 11FFF8H	External Bus Area								ROMS6
120000H to 13FFF8H									
140000H to 143FF8H	External Bus Area								ROMS7
144000H to 17FF8H									
148000H to 14BFF8H	SA4 (8KB)				SA5 (8KB)				
14C000H to 14FFF8H	SA6 (8KB)				SA7 (8KB)				
150000H to17FFF8H	Reserved								

(Continued)

(Continued)

32bit read	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000H to 1BFFF8H	External Bus Area								ROMS8
1C0000H to 1FFFF8H									ROMS9
200000H to 27FFF8H									ROMS10
280000H to 2FFFF8H									ROMS11
300000H to 37FFF8H									ROMS12
380000H to 3FFFF8H									ROMS13
400000H to 47FFF8H									ROMS14
480000H to 4FFFF8H									ROMS15

Note: Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read.

INTERRUPT VECTOR TABLE

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	—	3EC$_H$	000FFFEC$_H$	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	3E8$_H$	000FFFE8$_H$	—
Memory Protection exception *5	6	06	—	—	3E4$_H$	000FFFE4$_H$	—
System reserved	7	07	—	—	3E0$_H$	000FFFE0$_H$	—
System reserved	8	08	—	—	3DC$_H$	000FFFDC$_H$	—
System reserved	9	09	—	—	3D8$_H$	000FFFD8$_H$	—
System reserved	10	0A	—	—	3D4$_H$	000FFFD4$_H$	—
System reserved	11	0B	—	—	3D0$_H$	000FFFD0$_H$	—
System reserved	12	0C	—	—	3CC$_H$	000FFFCC$_H$	—
System reserved	13	0D	—	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	F$_H$ fixed		3C0$_H$	000FFFC0$_H$	—
External Interrupt 0	16	10	ICR00	440$_H$	3BC$_H$	000FFFBC$_H$	0, 16
External Interrupt 1	17	11			3B8$_H$	000FFFB8$_H$	1, 17
External Interrupt 2	18	12	ICR01	441$_H$	3B4$_H$	000FFFB4$_H$	2, 18
External Interrupt 3	19	13			3B0$_H$	000FFFB0$_H$	3, 19
External Interrupt 4	20	14	ICR02	442$_H$	3AC$_H$	000FFFAC$_H$	20
External Interrupt 5	21	15			3A8$_H$	000FFFA8$_H$	21
External Interrupt 6	22	16	ICR03	443$_H$	3A4$_H$	000FFFA4$_H$	22
External Interrupt 7	23	17			3A0$_H$	000FFFA0$_H$	23
External Interrupt 8	24	18	ICR04	444$_H$	39C$_H$	000FFF9C$_H$	—
External Interrupt 9	25	19			398$_H$	000FFF98$_H$	—
External Interrupt 10	26	1A	ICR05	445$_H$	394$_H$	000FFF94$_H$	—
External Interrupt 11	27	1B			390$_H$	000FFF90$_H$	—
External Interrupt 12	28	1C	ICR06	446$_H$	38C$_H$	000FFF8C$_H$	—
External Interrupt 13	29	1D			388$_H$	000FFF88$_H$	—
External Interrupt 14	30	1E	ICR07	447$_H$	384$_H$	000FFF84$_H$	—
External Interrupt 15	31	1F			380$_H$	000FFF80$_H$	—

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Reload Timer 0	32	20	ICR08	448H	37CH	000FFF7CH	4, 32
Reload Timer 1	33	21			378H	000FFF78H	5, 33
Reload Timer 2	34	22	ICR09	449H	374H	000FFF74H	34
Reload Timer 3	35	23			370H	000FFF70H	35
Reload Timer 4	36	24	ICR10	44AH	36CH	000FFF6CH	36
Reload Timer 5	37	25			368H	000FFF68H	37
Reload Timer 6	38	26	ICR11	44BH	364H	000FFF64H	38
Reload Timer 7	39	27			360H	000FFF60H	39
Free Run Timer 0	40	28	ICR12	44CH	35CH	000FFF5CH	40
Free Run Timer 1	41	29			358H	000FFF58H	41
Free Run Timer 2	42	2A	ICR13	44DH	354H	000FFF54H	42
Free Run Timer 3	43	2B			350H	000FFF50H	43
Free Run Timer 4	44	2C	ICR14	44EH	34CH	000FFF4CH	44
Free Run Timer 5	45	2D			348H	000FFF48H	45
Free Run Timer 6	46	2E	ICR15	44FH	344H	000FFF44H	46
Free Run Timer 7	47	2F			340H	000FFF40H	47
CAN 0	48	30	ICR16	450H	33CH	000FFF3CH	—
Reserved	49	31			338H	000FFF38H	—
Reserved	50	32	ICR17	451H	334H	000FFF34H	—
Reserved	51	33			330H	000FFF30H	—
Reserved	52	34	ICR18	452H	32CH	000FFF2CH	—
Reserved	53	35			328H	000FFF28H	—
LIN-USART 0 RX	54	36	ICR19	453H	324H	000FFF24H	6, 48
LIN-USART 0 TX	55	37			320H	000FFF20H	7, 49
Reserved	56	38	ICR20	454H	31CH	000FFF1CH	8, 50
Reserved	57	39			318H	000FFF18H	9, 51
LIN-USART 2 RX	58	3A	ICR21	455H	314H	000FFF14H	52
LIN-USART 2 TX	59	3B			310H	000FFF10H	53
LIN-USART 3 RX	60	3C	ICR22	456H	30CH	000FFF0CH	54
LIN-USART 3 TX	61	3D			308H	000FFF08H	55
System Reserved	62	3E	ICR23 *3	457H	304H	000FFF04H	—
Delayed Interrupt	63	3F			300H	000FFF00H	—
System Reserved *4	64	40	ICR24	458H	2FCH	000FFEFCH	—
System Reserved *4	65	41			2F8H	000FFEF8H	—

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
LIN-USART (FIFO) 4 RX	66	42	ICR25	459H	2F4H	000FFEF4H	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0H	000FFEF0H	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	45AH	2ECH	000FFEECH	12, 58
LIN-USART (FIFO) 5 TX	69	45			2E8H	000FFEE8H	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	45BH	2E4H	000FFEE4H	60
LIN-USART (FIFO) 6 TX	71	47			2E0H	000FFEE0H	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	45CH	2DCH	000FFEDCH	62
LIN-USART (FIFO) 7 TX	73	49			2D8H	000FFED8H	63
I²C 0	74	4A	ICR29	45DH	2D4H	000FFED4H	—
I²C 1	75	4B			2D0H	000FFED0H	—
Reserved	76	4C	ICR30	45EH	2CCH	000FFECCH	64
Reserved	77	4D			2C8H	000FFEC8H	65
Reserved	78	4E	ICR31	45FH	2C4H	000FFEC4H	66
Reserved	79	4F			2C0H	000FFEC0H	67
Reserved	80	50	ICR32	460H	2BCH	000FFEBCH	68
Reserved	81	51			2B8H	000FFEB8H	69
Reserved	82	52	ICR33	461H	2B4H	000FFEB4H	70
Reserved	83	53			2B0H	000FFEB0H	71
Reserved	84	54	ICR34	462H	2ACH	000FFEACH	72
Reserved	85	55			2A8H	000FFEA8H	73
Reserved	86	56	ICR35	463H	2A4H	000FFEA4H	74
Reserved	87	57			2A0H	000FFEA0H	75
Reserved	88	58	ICR36	464H	29CH	000FFE9CH	76
Reserved	89	59			298H	000FFE98H	77
Reserved	90	5A	ICR37	465H	294H	000FFE94H	78
Reserved	91	5B			290H	000FFE90H	79
Input Capture 0	92	5C	ICR38	466H	28CH	000FFE8CH	80
Input Capture 1	93	5D			288H	000FFE88H	81
Input Capture 2	94	5E	ICR39	467H	284H	000FFE84H	82
Input Capture 3	95	5F			280H	000FFE80H	83
Input Capture 4	96	60	ICR40	468H	27CH	000FFE7CH	84
Input Capture 5	97	61			278H	000FFE78H	85
Input Capture 6	98	62	ICR41	469H	274H	000FFE74H	86
Input Capture 7	99	63			270H	000FFE70H	87

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Output Compare 0	100	64	ICR42	46A$_H$	26C$_H$	000FFE6C$_H$	88
Output Compare 1	101	65			268$_H$	000FFE68$_H$	89
Output Compare 2	102	66	ICR43	46B$_H$	264$_H$	000FFE64$_H$	90
Output Compare 3	103	67			260$_H$	000FFE60$_H$	91
Output Compare 4	104	68	ICR44	46C$_H$	25C$_H$	000FFE5C$_H$	92
Output Compare 5	105	69			258$_H$	000FFE58$_H$	93
Output Compare 6	106	6A	ICR45	46D$_H$	254$_H$	000FFE54$_H$	94
Output Compare 7	107	6B			250$_H$	000FFE50$_H$	95
Sound Generator	108	6C	ICR46	46E$_H$	24C$_H$	000FFE4C$_H$	—
Reserved	109	6D			248$_H$	000FFE48$_H$	—
System Reserved	110	6E	ICR47 *3	46F$_H$	244$_H$	000FFE44$_H$	—
System Reserved	111	6F			240$_H$	000FFE40$_H$	—
PPG 0	112	70	ICR48	470$_H$	23C$_H$	000FFE3C$_H$	15, 96
PPG 1	113	71			238$_H$	000FFE38$_H$	97
PPG 2	114	72	ICR49	471$_H$	234$_H$	000FFE34$_H$	98
PPG 3	115	73			230$_H$	000FFE30$_H$	99
PPG 4	116	74	ICR50	472$_H$	22C$_H$	000FFE2C$_H$	100
PPG 5	117	75			228$_H$	000FFE28$_H$	101
PPG 6	118	76	ICR51	473$_H$	224$_H$	000FFE24$_H$	102
PPG 7	119	77			220$_H$	000FFE20$_H$	103
PPG 8	120	78	ICR52	474$_H$	21C$_H$	000FFE1C$_H$	104
PPG 9	121	79			218$_H$	000FFE18$_H$	105
PPG 10	122	7A	ICR53	475$_H$	214$_H$	000FFE14$_H$	106
PPG 11	123	7B			210$_H$	000FFE10$_H$	107
PPG 12	124	7C	ICR54	476$_H$	20C$_H$	000FFE0C$_H$	108
PPG 13	125	7D			208$_H$	000FFE08$_H$	109
PPG 14	126	7E	ICR55	477$_H$	204$_H$	000FFE04$_H$	110
PPG 15	127	7F			200$_H$	000FFE00$_H$	111
Up/Down Counter 0	128	80	ICR56	478$_H$	1FC$_H$	000FFDFC$_H$	—
Up/Down Counter 1	129	81			1F8$_H$	000FFDF8$_H$	—
Reserved	130	82	ICR57	479$_H$	1F4$_H$	000FFDF4$_H$	—
Reserved	131	83			1F0$_H$	000FFDF0$_H$	—
Real Time Clock	132	84	ICR58	47A$_H$	1EC$_H$	000FFDEC$_H$	—
Calibration Unit	133	85			1E8$_H$	000FFDE8$_H$	—

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
A/D Converter 0	134	86	ICR59	47B$_H$	1E4$_H$	000FFDE4$_H$	14, 112
System reserved	135	87			1E0$_H$	000FFDE0$_H$	—
Alarm Comparator 0	136	88	ICR60	47C$_H$	1DC$_H$	000FFDDC$_H$	—
Reserved	137	89			1D8$_H$	000FFDD8$_H$	—
Low Voltage Detection	138	8A	ICR61	47D$_H$	1D4$_H$	000FFDD4$_H$	—
Reserved	139	8B			1D0$_H$	000FFDD0$_H$	—
Time base Overflow	140	8C	ICR62	47E$_H$	1CC$_H$	000FFDCC$_H$	—
PLL Clock Gear	141	8D			1C8$_H$	000FFDC8$_H$	—
DMA Controller	142	8E	ICR63	47F$_H$	1C4$_H$	000FFDC4$_H$	—
Main/Sub OSC stability wait	143	8F			1C0$_H$	000FFDC0$_H$	—
Security vector	144	90	—	—	1BC$_H$	000FFDBC$_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	1B8$_H$ to 000$_H$	000FFDB8$_H$ to 000FFC00$_H$	—

*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00$_H$) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00$_H$ after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03$_H$: IOS[0])

*4 : Used by REALOS

*5 : Memory Protection Unit (MPU) support

RECOMMENDED SETTINGS

1. PLL and Clockgear settings

Please note that for MB91F464HB the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash .

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

2. Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	88	79.5	98.5
1	3	026F	84	76.1	93.8
1	3	026F	80	72.6	89.1
1	5	02AE	80	68.7	95.8
2	3	046E	80	68.7	95.8
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
1	7	02ED	76	62	98.1
2	3	046E	76	65.3	90.8
3	3	066D	76	62	98.1
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
3	3	066D	72	58.8	92.7
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
1	11	036B	64	47.6	97.6
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1
5	3	0A6B	64	47.6	97.6
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73

ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	$V_{DD}5R$	- 0.3	+ 6.0	V	
Power supply voltage 2*1	$V_{DD}5$	- 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output.
		$V_{SS}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	All pins of the Ports 26 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage*1	$AV_{CC}5$	- 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH	- 0.3	+ 6.0	V	*2
Input voltage 1*1	V_{I1}	Vss5 - 0.3	$V_{DD}5$ + 0.3	V	
Analog pin input voltage*1	V_{IA}	AVss5 - 0.3	AVcc5 + 0.3	V	
Output voltage 1*1	V_{O1}	Vss5 - 0.3	$V_{DD}5$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	- 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
"L" level maximum output current*4	I_{OL}	—	10	mA	
"L" level average output current*5	I_{OLAV}	—	8	mA	
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current*6	ΣI_{OLAV}	—	50	mA	
"H" level maximum output current*4	I_{OH}	—	- 10	mA	
"H" level average output current*5	I_{OHAV}	—	- 4	mA	
"H" level total maximum output current	ΣI_{OH}	—	- 100	mA	
"H" level total average output current*6	ΣI_{OHAV}	—	- 25	mA	
Power consumption	P_D	—	600	mW	at T_A = 105°C
Operating temperature	T_A	- 40	+ 105	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

*1 : The parameter is based on $V_{SS}5$ = $AV_{SS}5$ = 0.0 V.

2. Recommended operating conditions

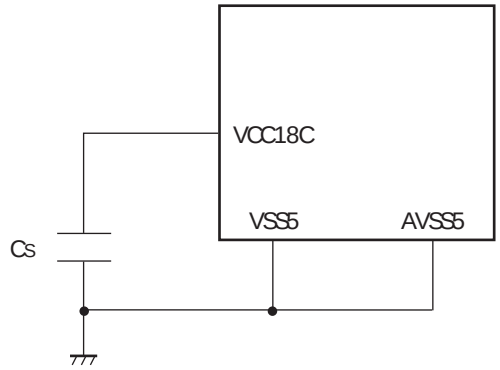
($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T_A	– 40	—	+ 105	°C	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kΩ $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	$VDD_{CORE} \geq$ 1.65V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



3. DC characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	—	V_{DD} + 0.3	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				0.74 × V_{DD}	—	V_{DD} + 0.3	V	3 V ≤ V_{DD} < 4.5 V
		—	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	
		—	Port inputs if TTL input is selected	2.0	—	V_{DD} + 0.3	V	
	V_{IHR}	INITX	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	—	V_{DD} - 0.3	—	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	V_{DD} + 0.3	V	External clock in “Oscillation mode”
	V_{IHX0F}	X0	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	External clock in “Fast Clock Input mode”
Input “L” voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	—	0.2 × V_{DD}	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	—	0.3 × V_{DD}	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	—	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} - 0.3	—	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		—	Port inputs if TTL input is selected	V_{SS} - 0.3	—	0.8	V	
	V_{ILR}	INITX	—	V_{SS} - 0.3	—	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	—	V_{SS} - 0.3	—	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	V_{SS} - 0.3	—	0.5	V	External clock in “Oscillation mode”

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current MB91F464HB	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	100	130	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	-	30	150	µA	At stop mode *5
			T_A = + 105 °C	-	300	2000	µA	
			T_A = + 25 °C	-	100	500	µA	RTC : 4 MHz mode *5
			T_A = + 105 °C	-	500	2400	µA	
			T_A = + 25 °C	-	50	250	µA	RTC : 100 kHz mode *5
			T_A = + 105 °C	-	400	2200	µA	
	I_{LVE}	$V_{DD}5$	—	—	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.

4. A/D converter characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

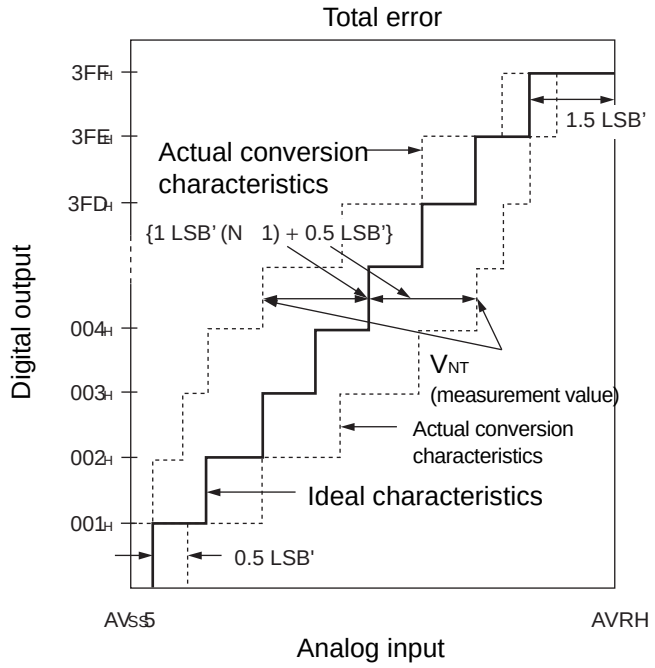
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 3	—	+ 3	LSB	
Nonlinearity error	—	—	− 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	− 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL− 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH− 3.5 LSB	AVRH− 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	—	0.6	—	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	− 1	—	+ 1	µA	T_A = + 25 °C
			− 3	—	+ 3	µA	T_A = + 105 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

Definition of A/D converter terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point (00 0000 0000$_B$ ↔ 00 0000 0001$_B$) and the full scale transition point (11 1111 1110$_B$ ↔ 11 1111 1111$_B$).
- Differential nonlinearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



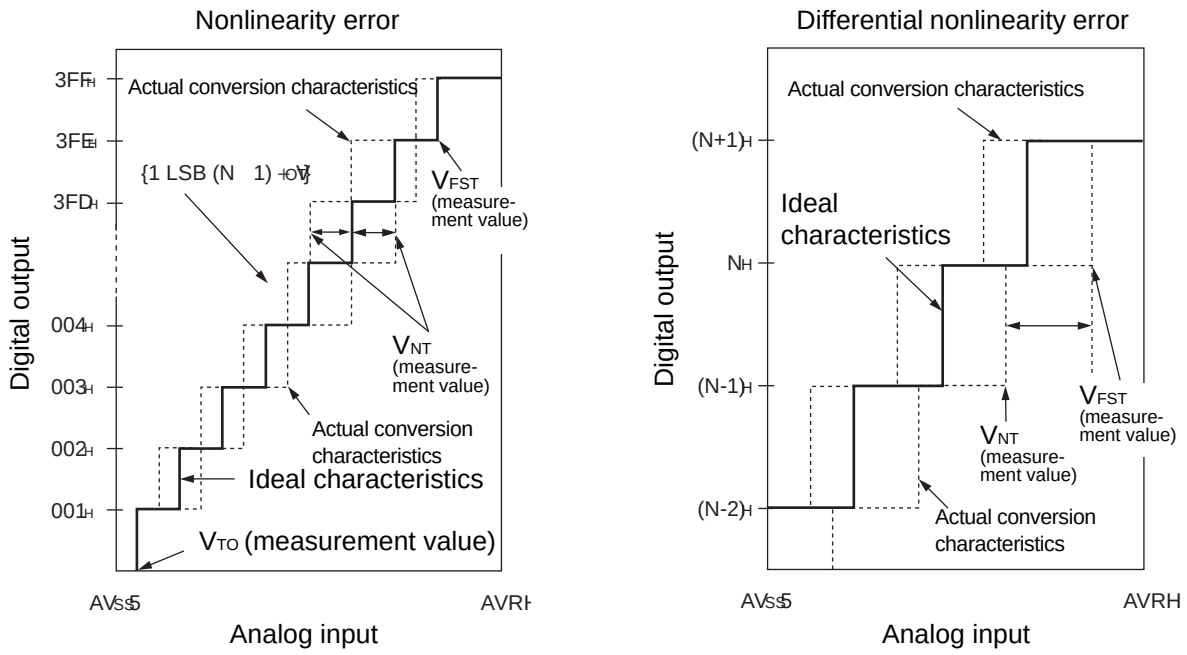
$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5$ + 0.5 LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from (N + 1) $_H$ to N$_H$

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

5. Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	- 1	—	+ 1	µA	T_A=25 °C
			- 3	—	+ 3	µA	T_A=105 °C
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ - 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ - 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparion time	t_{COMPF}		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: *1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

6. FLASH memory program/erase characteristics

6.1. MB91F464HB

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit or 32-bit width) programming time	-	23	370	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

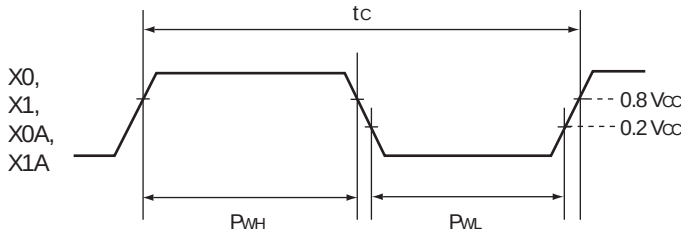
7. AC characteristics

7.1. Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

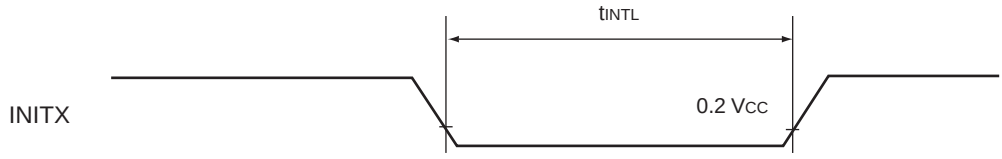
• Clock timing condition



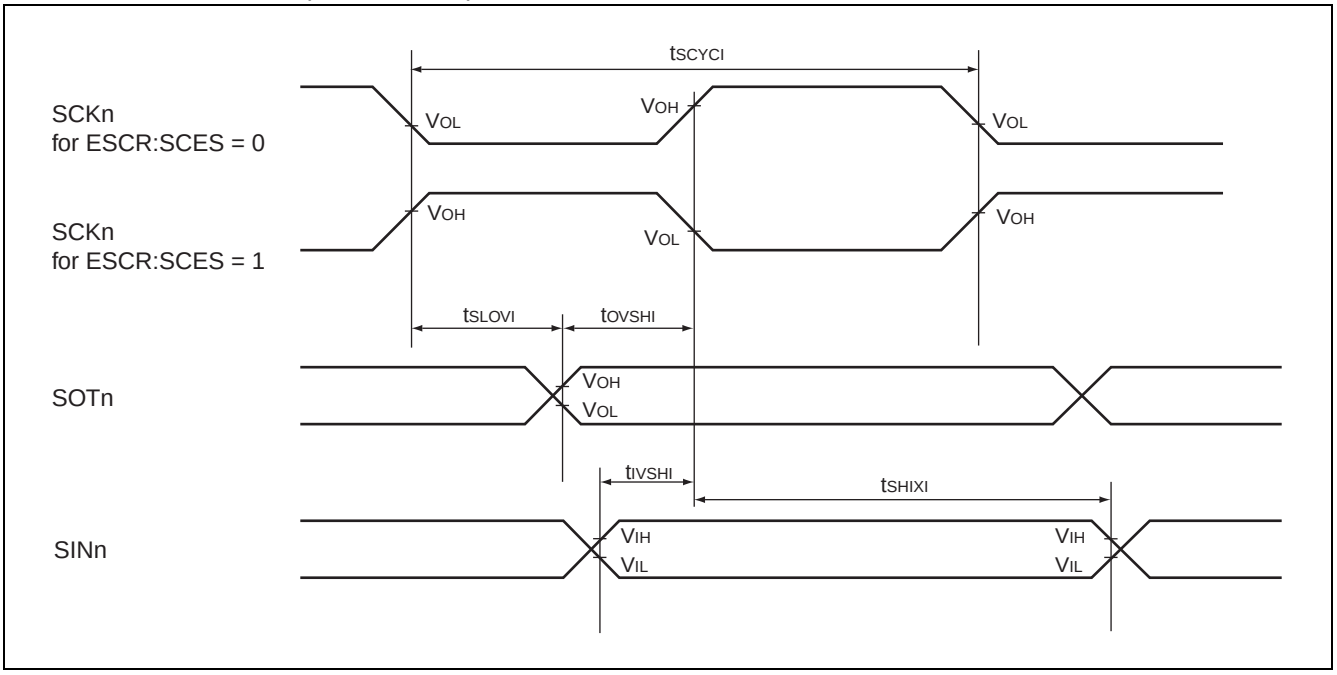
7.2. Reset input ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

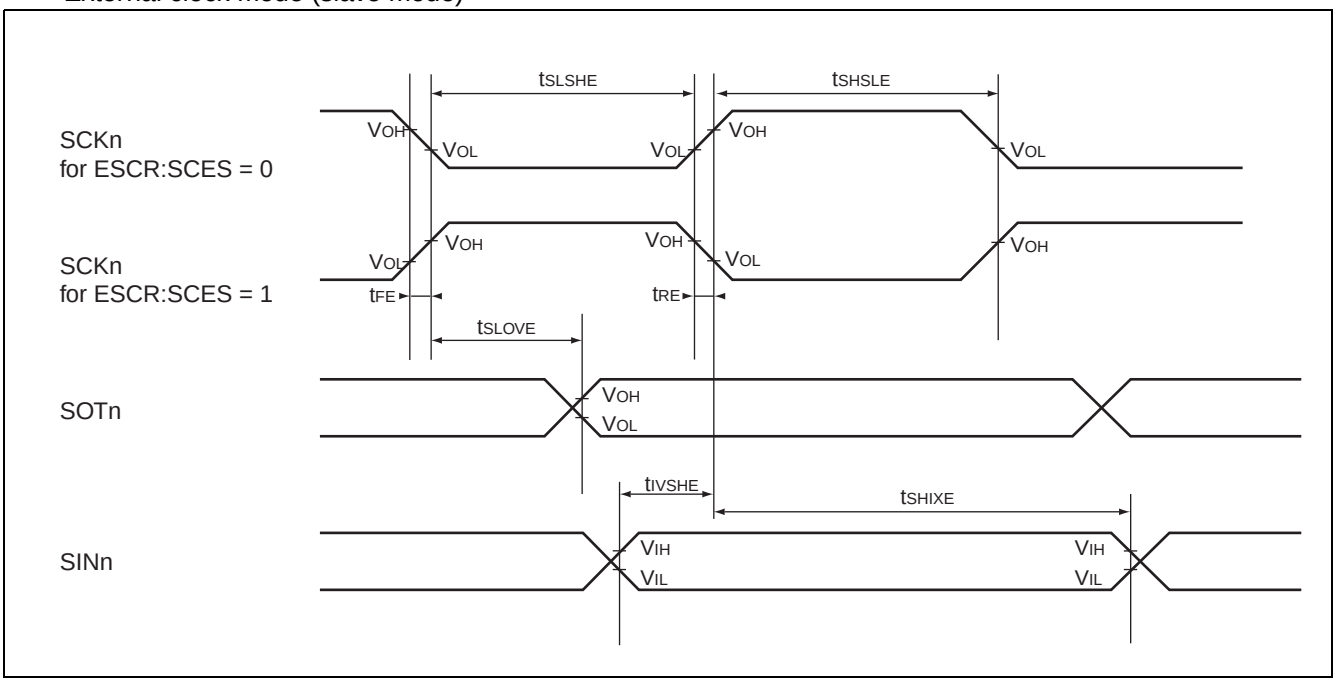
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



• Internal clock mode (master mode)



• External clock mode (slave mode)



7.4. I²C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = - 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

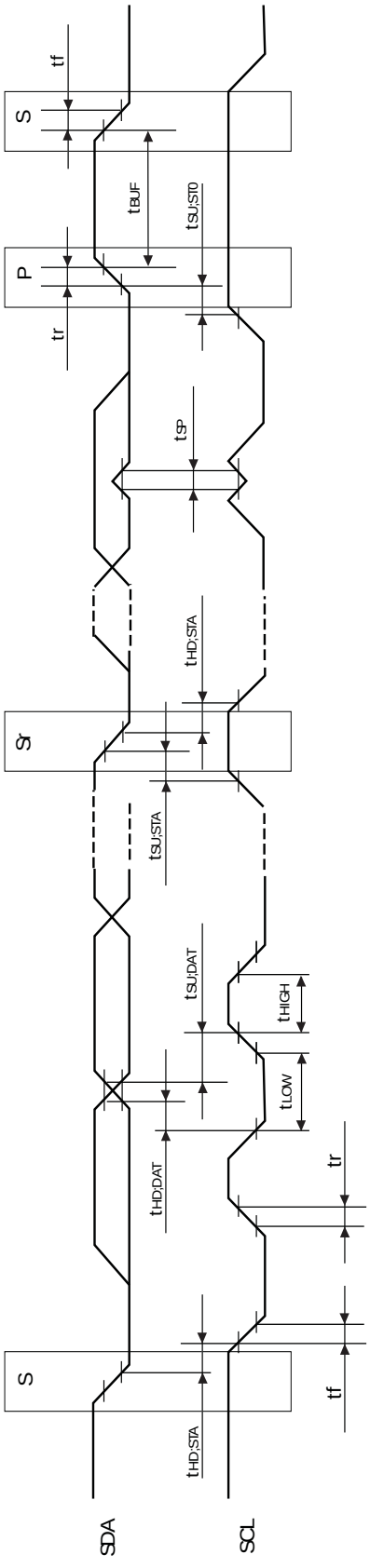
Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I²C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I²C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

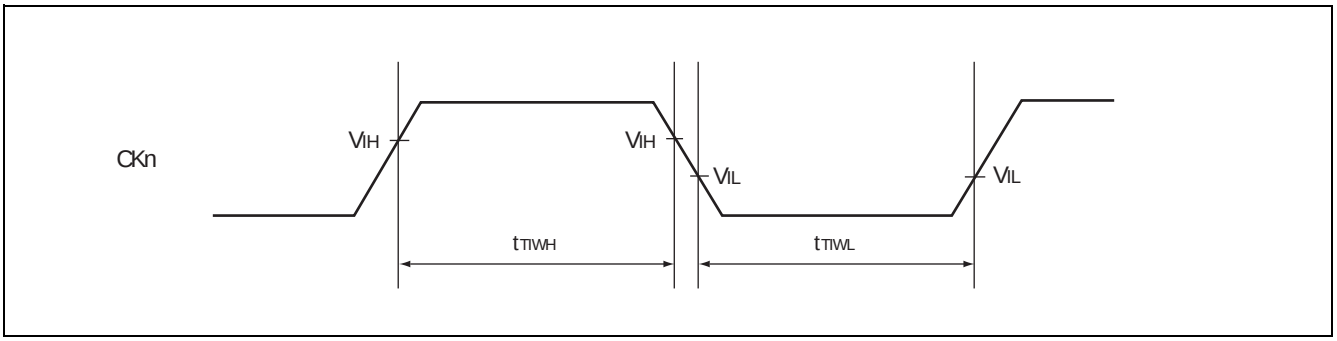

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
tf
S
tHD;STA
SDA
SCL

7.5. Free-run timer clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

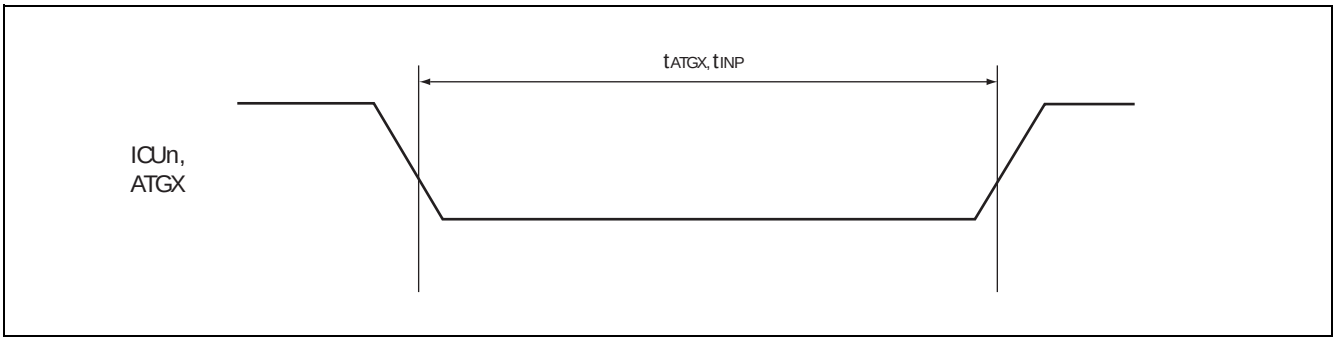


7.6. Trigger input timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.



7.7. External Bus AC Timings at $V_{DD}35$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = - 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.5 × $V_{DD}35$
  - VOH = 0.5 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

7.7.1. Basic Timing

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

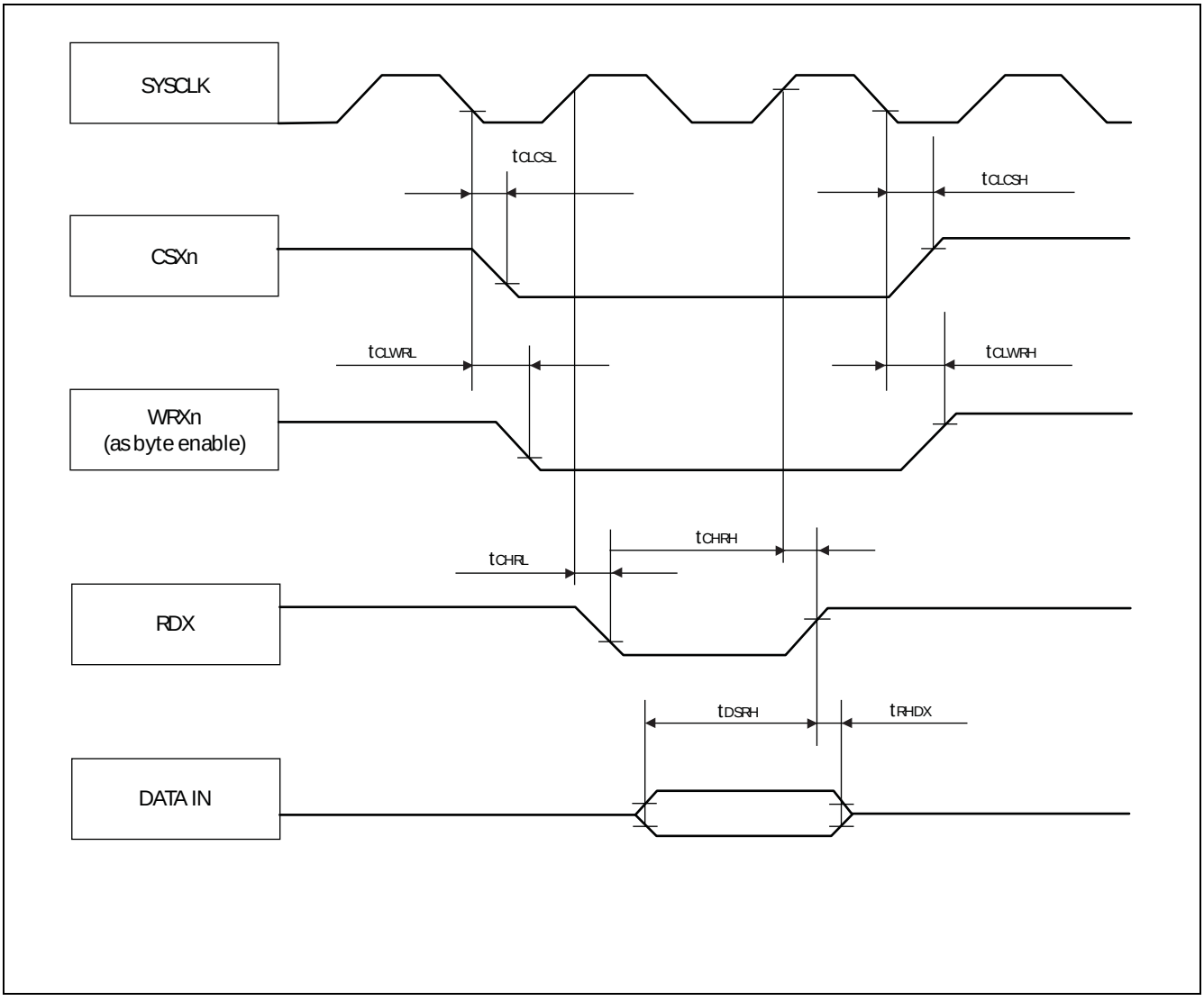
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 × t_{CLKT} - 1	1/2 × t_{CLKT} + 9	ns
	t_{CHCL}		1/2 × t_{CLKT} - 9	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	8	ns
	t_{CLCSH}		—	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	—	13	ns

Note : t_{CLKT} is the cycle time of the external bus clock.

7.7.2. Synchronous/Asynchronous read access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

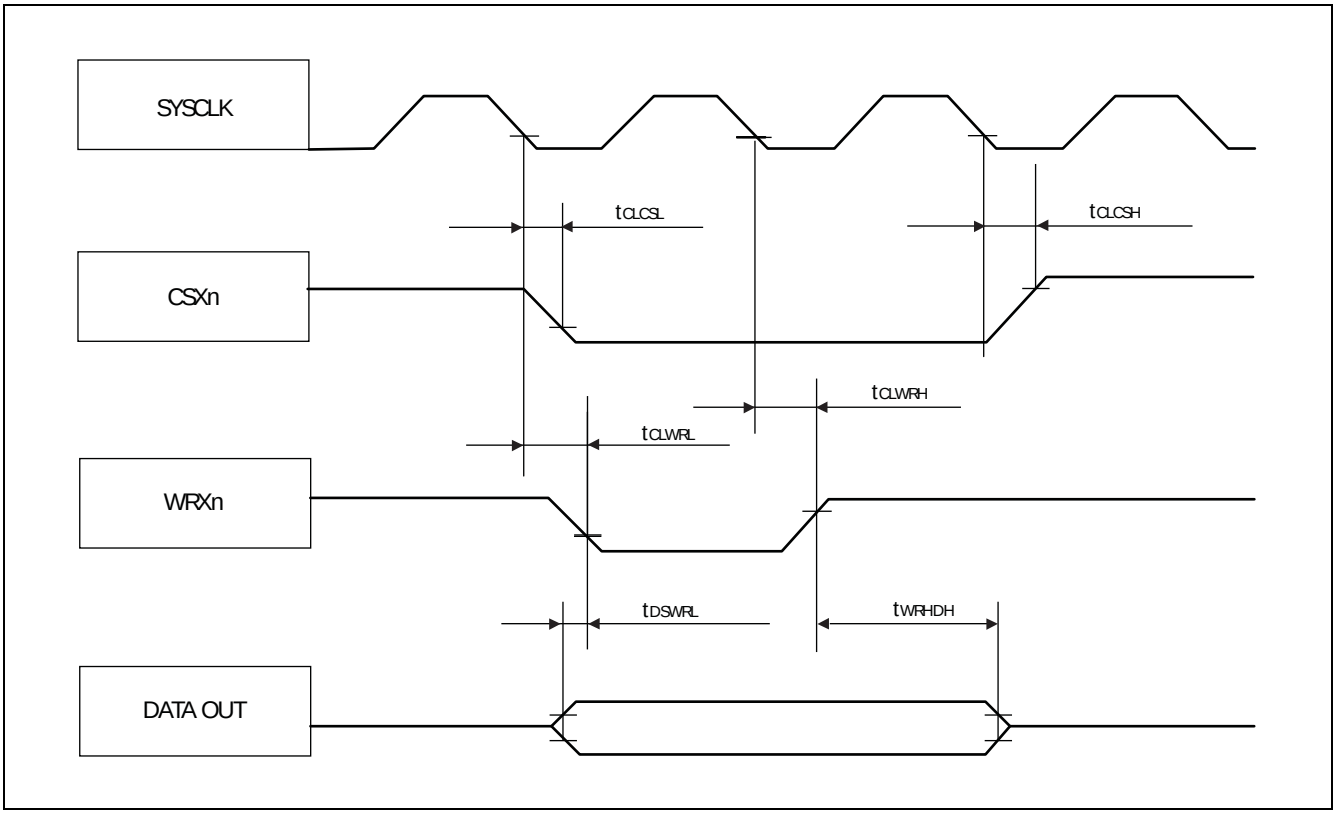
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	- 7	1	ns
	TCHRH		- 4	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	33	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	8	ns
	TCLWRH		0	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	12	ns



7.7.3. Synchronous write access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

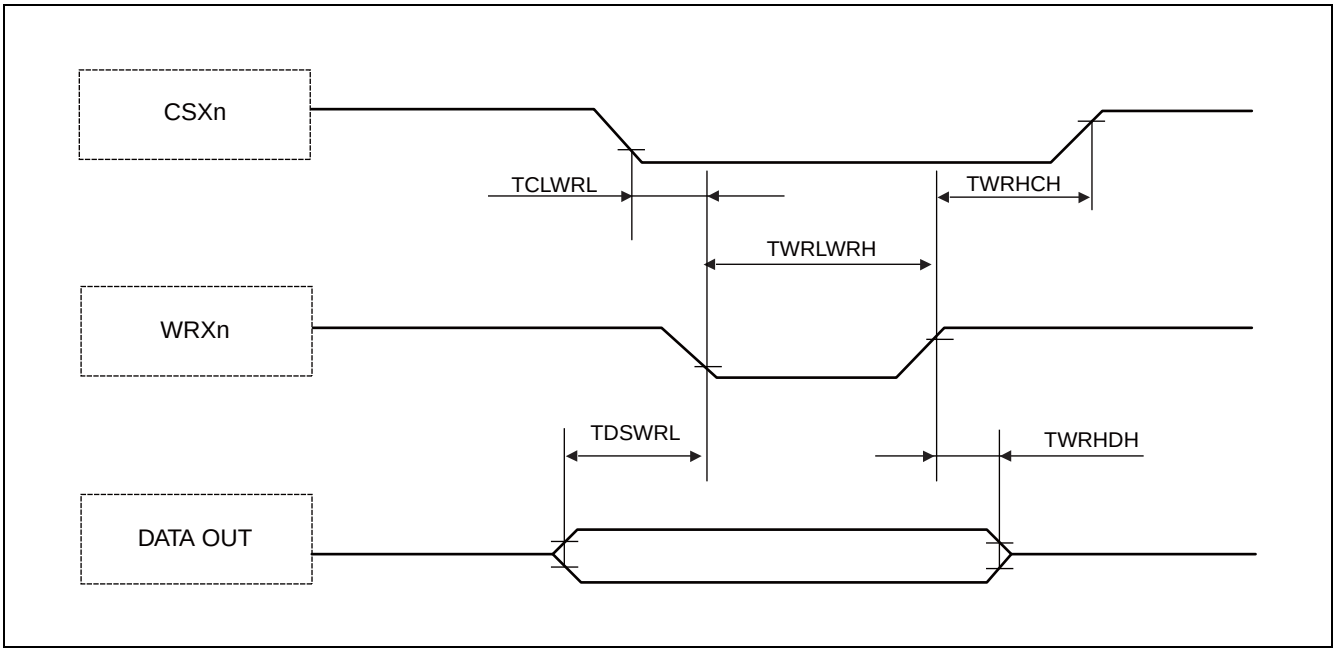
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	8	ns
	TCLWRH		0	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	- 7	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} - 20	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	12	ns



7.7.4. Asynchronous write access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

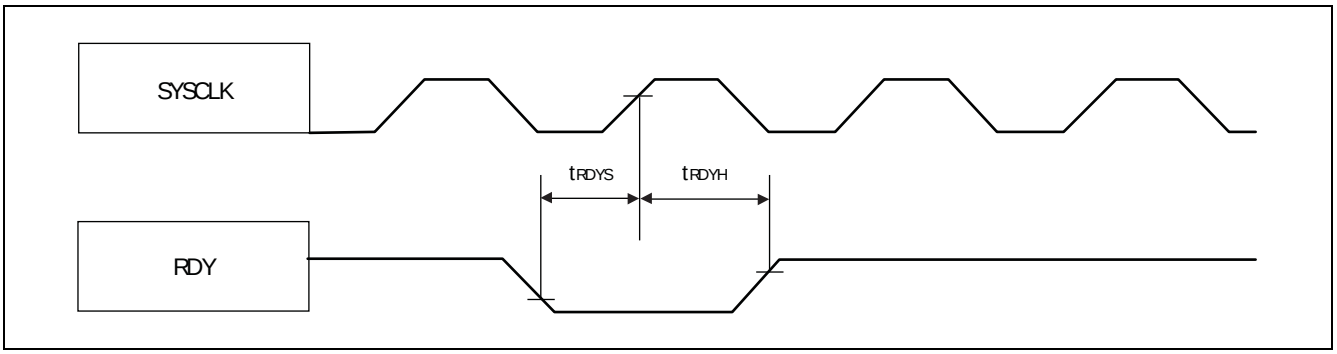
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT}	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} - 10	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} - 19	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT}	ns
	TWRHCH		1/2 × t_{CLKT}	—	ns



7.7.5. RDY waitcycle insertion

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	34	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns

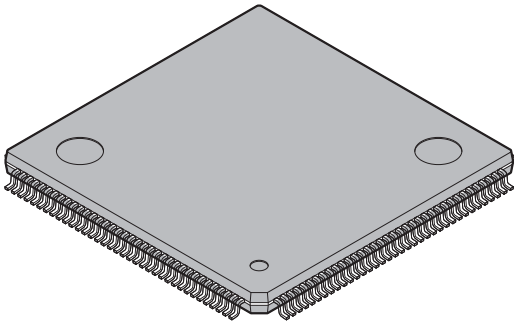


ORDERING INFORMATION

Part number	Package	Remarks
MB91F464HBPMC-GSE2	144-pin plastic LQFP (FPT-144P-M08)	Lead-free package

PACKAGE DIMENSION

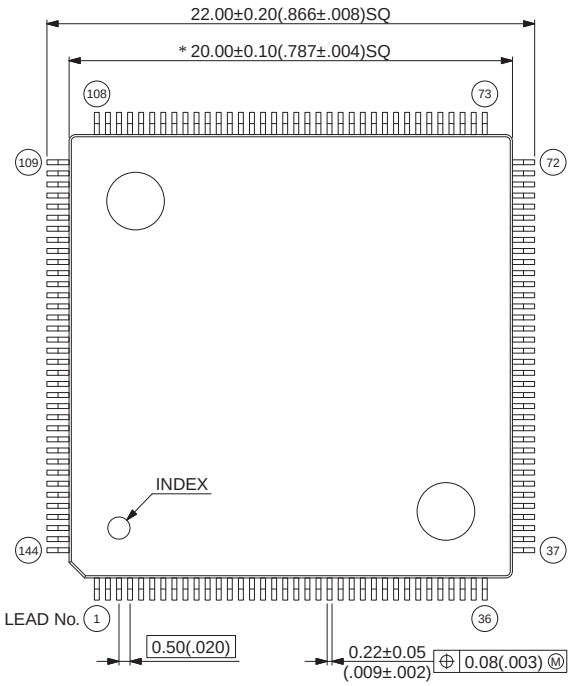
144-pin plastic LQFP

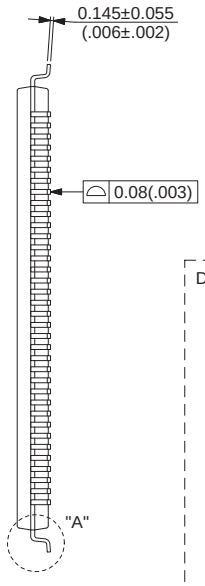


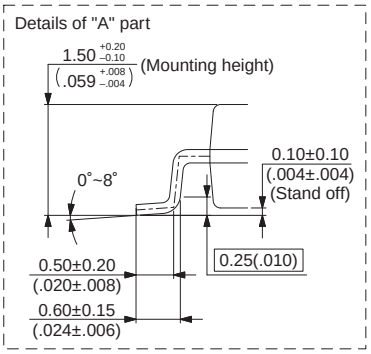
(FPT-144P-M08)

Lead pitch	0.50 mm
Package width × package length	20.0 × 20.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	1.20g
Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)







Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.

http://edevice.fujitsu.com/package/en-search/

REVISION HISTORY

Version	Date	Remark
2.0	2009-01-07	Initial version

MEMO

MEMO

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