32Mbit, 1MX32, 5V CMOS S-RAM MODULE

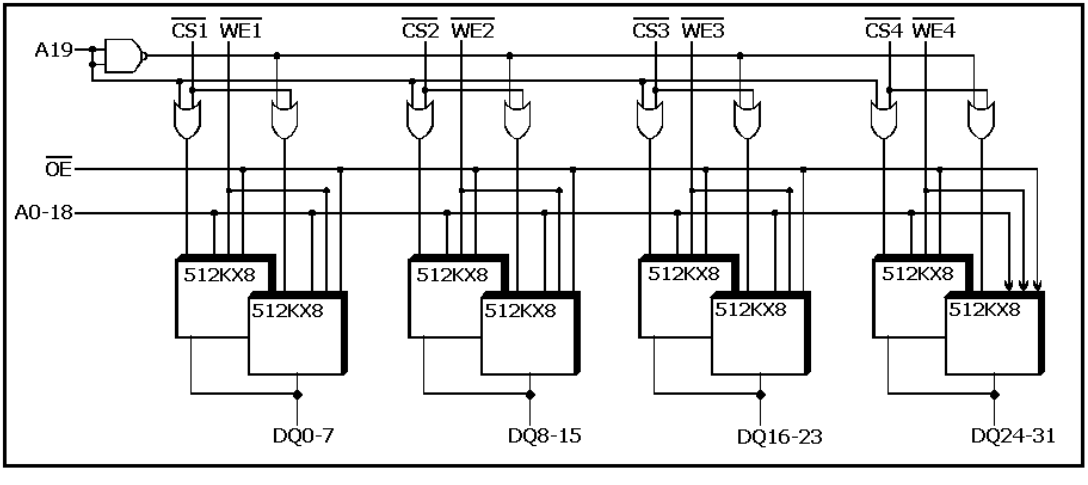
Features

- Module Access Times: 20, 35 & 45ns
- Package:
  - 66-Pin Ceramic PGA 1.385" SQ
  - Package Height 0.215"/ 0.160”
- Single 5V (±10%) Power Supply
- Industrial and Military Screening
- Organized as two banks of 512Kx32
- User Configurable as :
  - 1Mx32, 2Mx16 or 4Mx8
- TTL Compatible Input/Output

Product Description

The MES1M32 is a 32 megabit High Speed Static Ram MCM. Each MCM is constructed from 8 -512KX8 SRam assembled in a multilayered cofired ceramic package, designed with power and ground planes for lower noise and better ground bounce. These MCMs are available in 20 to 45ns versions.

Block Diagram



Elisra Microelectronics TEL: 972-3-6175015 Fax: 972-3-6175650 Email: microel@elisra.com

Pin Names

Pin Name	Pin Function
A0÷A19	Address Inputs
DQ0÷DQ31	Data Inputs/Outputs
CS1#÷CS4#	Chip Selects
WE1#÷WE4#	Write Enables
OE#	Output Enable
GND	Ground
Vcc	Power (+5V ±10%)
NC	No Connection

Truth Table (H=V_{IH}, L=V_{IL}, X=Don't Care)

OE#	WE#	CS#	I/O	Mode
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Out Disable

Note: # Symbol means Active Low Signal

Pin Configuration for 66-Pin PGA (G1,G2) (Top View)

	A	B	C	F	G	H
1	● DQ8	● WE2#	● DQ15	DQ24 ●	VCC ●	DQ31 ●
2	● DQ9	● CS2#	● DQ14	DQ25 ●	CS4# ●	DQ30 ●
3	● DQ10	● GND	● DQ13	DQ26 ●	WE4# ●	DQ29 ●
4	● A13	● DQ11	● DQ12	A6 ●	DQ27 ●	DQ28 ●
5	● A14	● A10	● OE#	A7 ●	A3 ●	A0 ●
6	● A15	● A11	● A18	NC ●	A4 ●	A1 ●
7	● A16	● A12	● WE1#	A8 ●	A5 ●	A2 ●
8	● A17	● VCC	● DQ7	A9 ●	WE3# ●	DQ23 ●
9	● DQ0	● CS1#	● DQ6	DQ16 ●	CS3# ●	DQ22 ●
10	● DQ1	● A19	● DQ5	DQ17 ●	GND ●	DQ21 ●
11	● DQ2	● DQ3	● DQ4	DQ18 ●	DQ19 ●	DQ20 ●

Absolute Maximum Ratings

Item	Rating
Supply Voltage Relative to GND	-0.5V to +7.0V
Voltage on Any Pin Relative to GND	-0.5V to V_{CC} +0.5V
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating (Military)	T_A	-55	+125	°C
Temperature (Industrial)		-40	+85	°C

Capacitance (T_A = +25°C, V_{IN} = 0V, f = 1.0 MHz)

Description	Symbol	Limits		Unit
		Min	Max	
OE# Capacitance	C_{OE}		20	pF
WE1# to WE4# Capacitance	C_{WE}		20	pF
CS1# to CS4# Capacitance	C_{CS}		20	pF
DQ0 to DQ31 Capacitance	$C_{I/O}$		30	pF
A0 to A19 Capacitance	C_{AD}		20	pF

These parameters are guaranteed, but not tested.

DC Characteristics (Vcc = 5V)

Parameter	Symbol		Min	Max	Units
Input Leakage Current	I_{LI}(1)		-1	10	µA
Output Leakage Current	I_{LO}(2)		-1	10	µA
Output Low Voltage	V_{OL}(3)			0.4	V
Output High Voltage	V_{OH}(4)		2.4		V
Standby Supply Current	I_{SB}(5)	20ns		80	mA
		45ns		60	
Dynamic Operating Current (32 bit operation mode)	I_{CC}(6)	20ns		300	mA
		45ns		260	

Notes:

(1) V_{CC} = Max, $V_{I/O}$ = V_{CC} to GND

(2) $V_{I/O}$ = V_{CC} to GND, CS# ≥ V_{IH}, OE# ≥ V_{IH}

(3) V_{CC} = Min, I_{OL} = +8mA

(4) V_{CC} = Min, I_{OH} = -4mA

(5) CS # = V_{IH}, OE # = V_{IH}, V_{CC} = Max, f = 5.0 MHz

(6) V_{CC} = Max, CS# = V_{IL}, OE# = V_{IH}, f = 5.0 MHz

AC Characteristics

Write Cycle

Parameter	Symbol	20ns	35ns	45ns	Limits	Units
Write Cycle Time	TAVAV	20	35	45	min	ns
Address Set-up Time	TAVWL	0	0	0	min	ns
Address Valid to End of Write	TAVWH	15	25	35	min	ns
Data Valid to End of Write	TDVWH	10	20	30	min	ns
Chip Select Low to End of Write	TELWH	15	25	35	min	ns
Write Pulse Width	TWLWH	15	25	35	min	ns
Address Hold from Write End	TWHAX	2	2	2	min	ns
Data Hold Time	TWHDX	0	0	0	min	ns
Write Low to High Z	TWLQZ *	13	15	15	max	ns
Output Active from End of Write	TWHQX *	0	0	0	min	ns

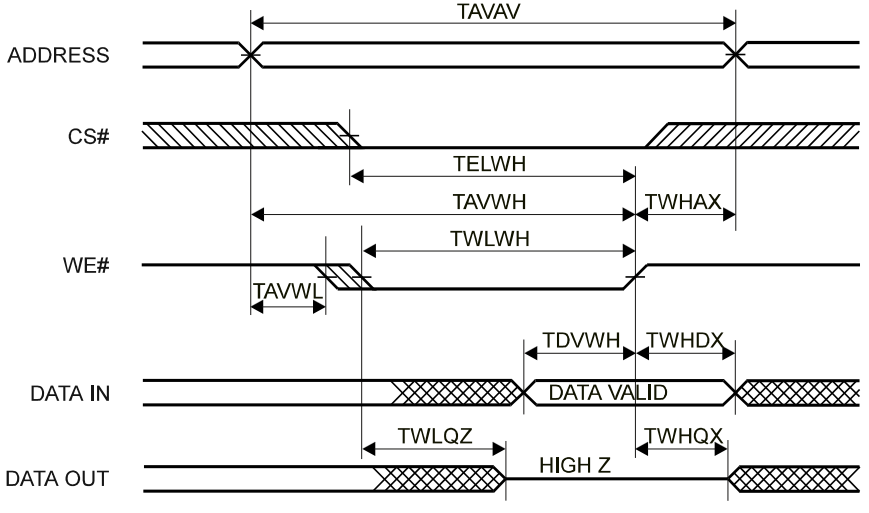
Read Cycle

Parameter	Symbol	20ns	35ns	45ns	Limits	Units
Read Cycle Time	TAVAV	20	35	45	min	ns
Address Access Time	TAVQV	20	35	45	max	ns
Output Hold from Address Change	TAVQX	5	5	5	min	ns
Chip Select Access Time	TELQV	20	35	45	max	ns
Output Enable to Output Valid	TGLQV	12	25	35	max	ns
Chip Select to Output in Low Z	TELQX*	3	4	4	min	ns
Chip Disable to Output in High Z	TEHQZ*	10	15	15	max	ns
Output Enable to Output in Low Z	TGLQX*	0	0	0	min	ns
Output Disable to Output in High Z	TGHQZ*	10	15	15	max	ns

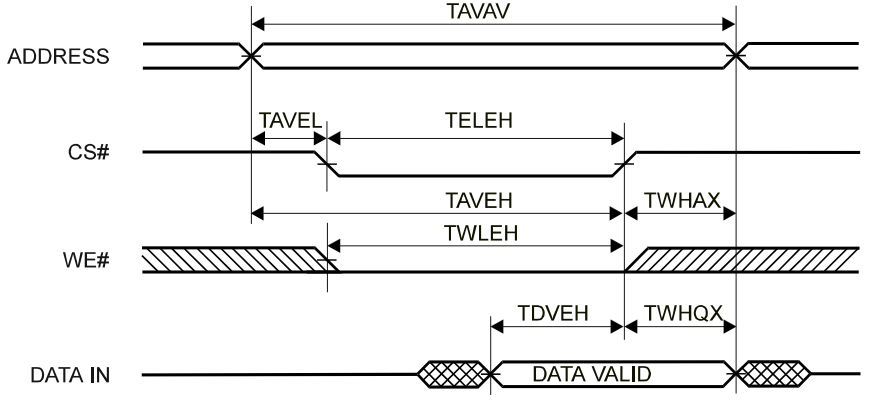
(*) - Parameter is guaranteed, but not tested.

Timing Waveforms of Write Cycle

Write Cycle 1: WE# Controlled (OE# = VIH)

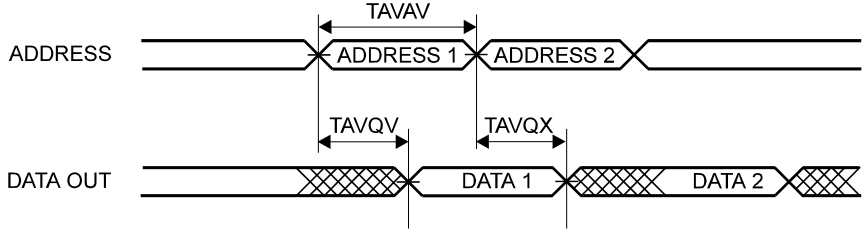


Write Cycle 2: CS# Controlled (OE# = VIH)

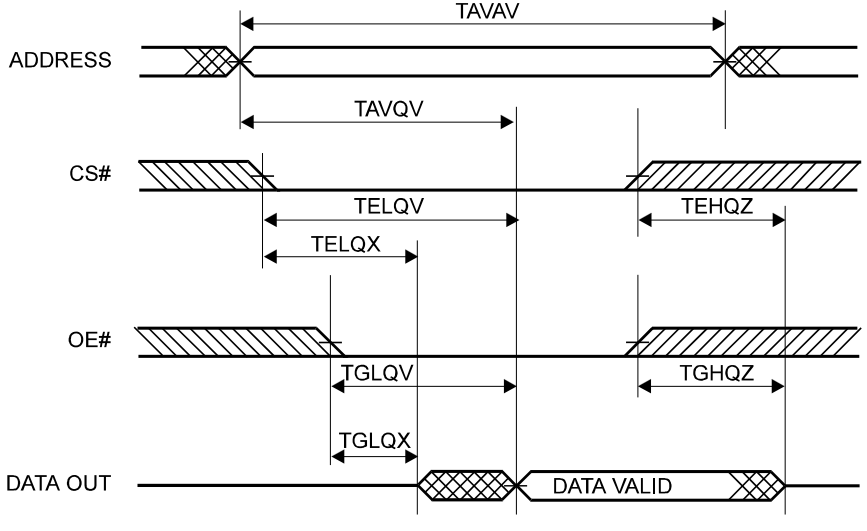


Timing Waveforms of Read Cycle

Read Cycle 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



Read Cycle 2 (WE# = V_{IH})

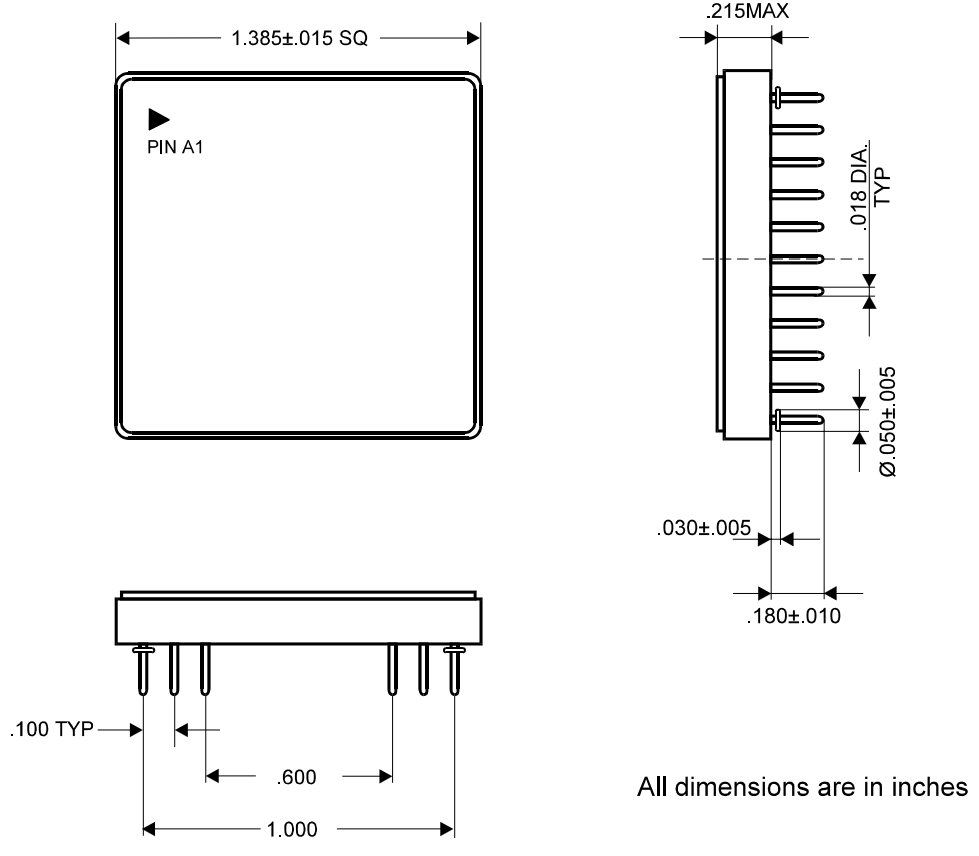


AC Test Conditions

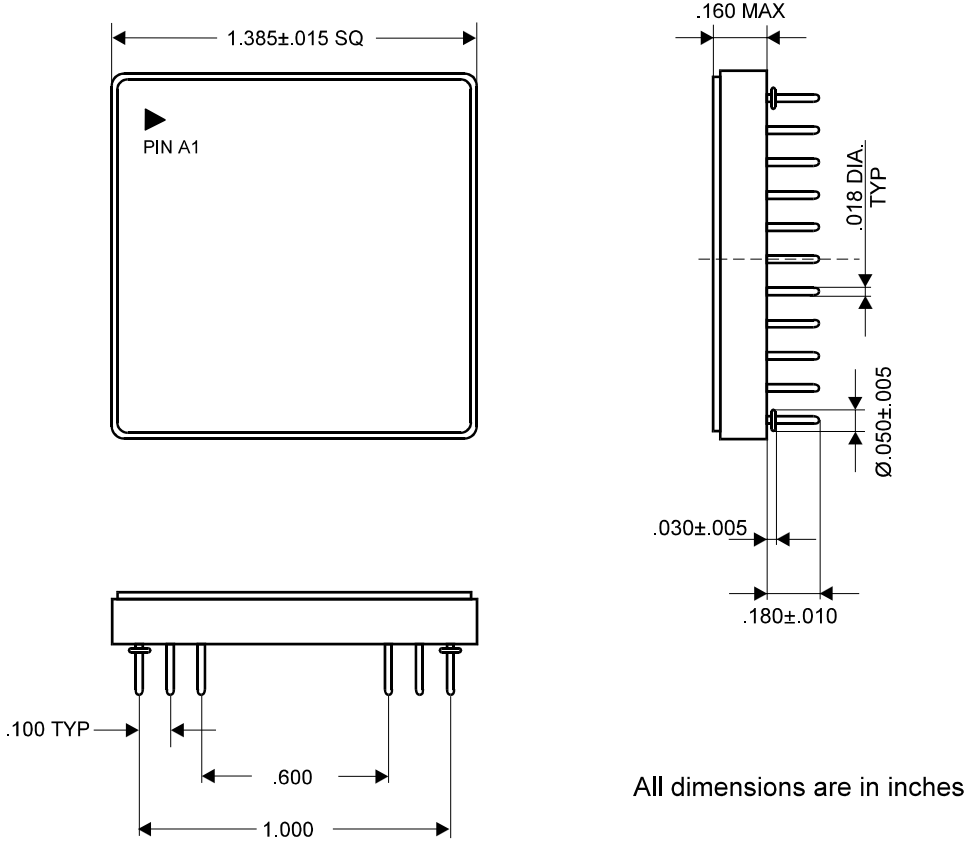
Item		Conditions
Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times		5ns
Input Timing Reference Level		1.5V
Output Timing Reference Level		1.5V
Output Load:	17ns to 70ns	1 TTL Load, CL=30pF
	85ns and up	1 TTL Load, CL=100pF

Note: For TWHQX, TWLQZ, TELQX, TEHQZ, TGLQX and TGHQZ CL = 5pF

Outline Drawing for 66-Pin Ceramic PGA (G1)



Outline Drawing for 66-Pin Thin Ceramic PGA (G2)



All dimensions are in inches

Ordering Information (Standard Military Screened Products*)

Model Number	*Speed*	*Package*
MES1M32G120M	**20ns**	**CPGA**
MES1M32G135M	**35ns**	**CPGA**
MES1M32G145M	**45ns**	**CPGA**
MES1M32G220M	**20ns**	**CPGA**
MES1M32G235M	**35ns**	**CPGA**
MES1M32G245M	**45ns**	**CPGA**

(*) - Contact Elisra for additional designs

Part Number Breakdown