T-52-13-07

GigaBit Logic

16G075

Laser Diode Driver
3 Gbit/s NRZ Data Rate

FEATURES

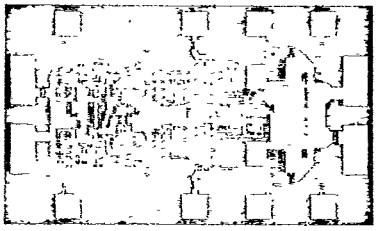
- High speed operation (2Gbps, 3 Gbps NRZ)
- Differential ECL compatible interface
- Single power supply (-5.2V)
- 25 to 50 mA p-p modulation current
- 0 to 40 mA bias current
- Maximum bias current preset control
- Auto Power Control provides protection against laser thermal runaway
- Low modulation current variation with temperature -5% ~ +15% at 0 to 50°C
- Available in 18 pin leadless chip carrier, die, or as an assembled and tested evaluation board

FUNCTIONAL DESCRIPTION

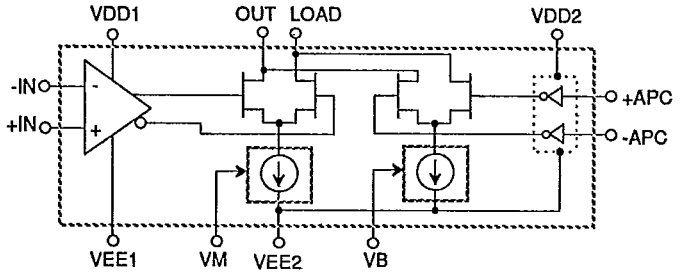
The 16G075 is a high performance (3 Gbit/s NRZ data rate) GaAs IC laser diode driver. It features single -5.2V supply operation, 0 to 40 mA presettable bias current and up to 50 mA modulation current while dissipating 650 mW typ.

The 16G075 features a differential, ECL compatible input for direct control from ECL or GaAs PicoLogic™ ICs. Two unique Auto Power Controls (+APC, -APC) permit modulation of the bias current control setting as a mechanism to protect the laser diode against thermal runaway. The APC controls may be modulated at rates up to 100 MHz.

CHIP PHOTOMICROGRAPH



CIRCUIT DIAGRAM



ORDERING INFORMATION

Package Type	SPEED	
	3 Gbit/s	2 Gbit/s
18-pin LCC	16G075-3L1	16G075-2L1
Die	16G075-3X	16G075-2X
Evaluation Board (Assembled & Tested)	16G075-3L1E	16G075-2L1E

EVALUATION BOARD

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ABSOLUTE MAXIMUM RATINGS (VDD = GND)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
VEE	Supply Voltage	-7 ~ +0.5V
PD	Power Dissipation	1.3W
+IN, -IN	Input Voltage	VEE to +0.5V
VOUT1,2	Output Voltage	VEE to +0.5V
VM	Modulation Current Control Voltage	VEE -1 to VEE +7V
VB	Maximum Bias Current Setting Voltage	VEE - 1 to +0.5V
+APC, -APC	APC (Auto Power Control) Voltage	VEE to +0.5V
TSTOR	Storage Temperature	-55 to + 150°C
TA	Ambient Operating Temperature	-55 to + 120°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS
VEE	Supply Voltage	-5.0	-5.2	-5.5	V
VOUT1,2	Output Voltage	-2.0	-1.0	0.0	V

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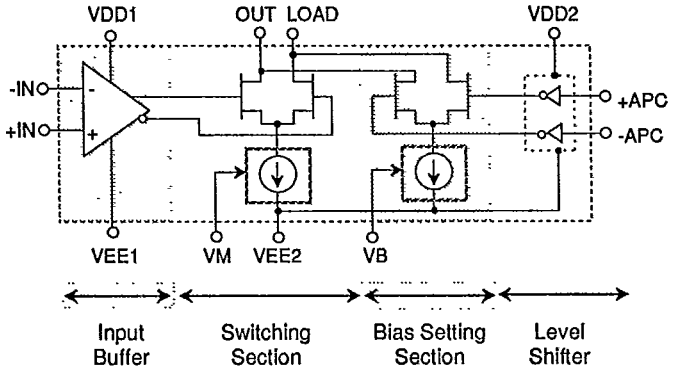
CIRCUIT DIAGRAM



PIN DESCRIPTIONS

VDD1, VDD2	Ground	VM	Modulation Current Control Voltage
+IN, -IN	Differential Mode Input	VB*	Maximum Bias Current (IBMAX) Setting Voltage
OUT	Output. The laser diode is connected to OUT in a common anode configuration	+APC	APC Signal Input
LOAD	Output for Load termination resistor (RLoad). RLoad should be approximately equal to LD Ron+OUT series resistance.	-APC	APC Reference Voltage Input
		VEE1,VEE2	-5.2V Supply Voltage

* IBMAX is divided into OUT and LOAD according to the differential voltage between +APC and -APC. The current flowing into OUT is the real bias current to the laser diode: IB. Thus, IB is limited at IBMAX during APC operation. This mechanism protects the laser diode against thermal runaway.

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ELECTRICAL CHARACTERISTICS

VDD = GND, VEE = -5.2V, VOUT1,2 = GND, TA = 25°C

Parameter	Symbol	Test Conditions		Value Min	Value Typ	Value Max	Units
Circuit Current	IEE	VM = -5.2V, VB = -5.2V				120*†	mA
Input Voltage	VIH	Differential Mode		-0.9		-0.7	V
	VIL			-1.9		-1.7	V
Input Current	+IN, -IN	+IN, -IN = -0.7V				150	µA
Modulation Current	IMMAX	VM = -4.2V, VB= -5.2V Note 1,4		50			mA
	IMMIN	VM = -5.2V, VB= -5.2V Note 1,4				25	mA
Bias Current	IBMAX	VB = -4.2, VM = -5.2V Note 2,3		40			mA
	IBMIN	VB = -5.2, VM = -5.2V Note 2,3				1	mA
Rise Time	tr	RL = 25Ω	16G075-3			200	ps
			16G075-2			300	
Fall Time	tf	RL = 25Ω	16G075-3			200	ps
			16G075-2			300	
Max. output current	Iout			90			mA
Max. APC input freq.	$f_{APC\ Max.}$				100		MHz

*† except modulation and bias current

NOTES:
1. Modulation circuit on: -IN = -1.7V, +IN = -0.9V
2. Modulation circuit off: -IN = -0.9, +IN = -1.7V
3. Bias circuit on: +APC = 0V, -APC = -2.5V
4. Bias circuit off: +APC = -2.5V, -APC = 0V
5. Variation of IM is -5% to + 15% under the ambient temperature range TA = 0°C to 50°C.
6. Usual control voltages are as follows:
   VB, VM: VEE to VEE + 1.0V
   +APC, -APC: -2.5 to 0.0V

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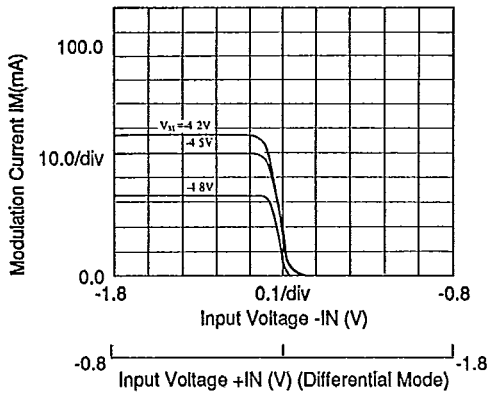
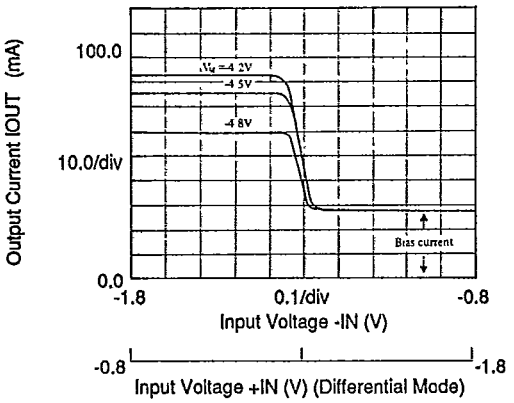
TYPICAL DC CHARACTERISTICS

1) Switching characteristics



a) MODULATION CURRENT SWITCHING
(IBMAX = 56mA, +APC = -2.0V, -APC = 0.0V



b) BIAS CURRENT 28 mA
(IBMAX = 56mA, +APC = -APC = -1.3V)

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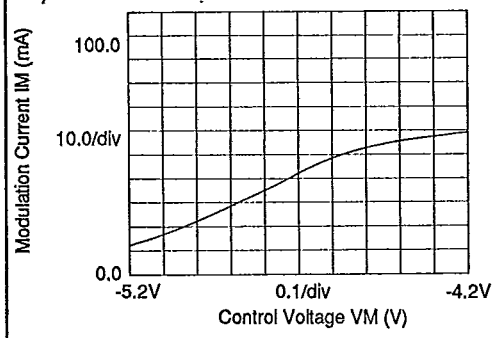
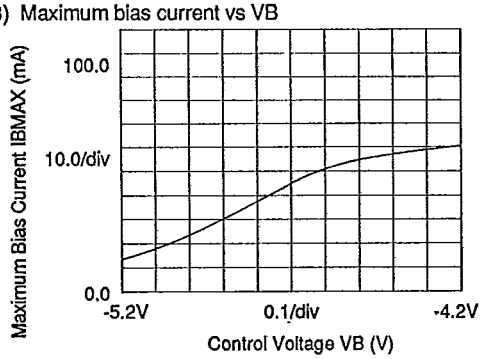
2) Modulation current vs VM



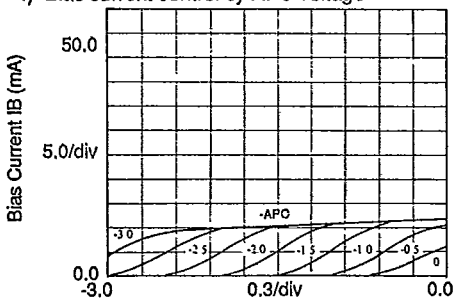
Input is set to "on" (-IN = -1.8V, +IN = -0.8V)
Bias current is cut by APC signal (+APC = -2.0V, -APC = 0.0V)

3) Maximum bias current vs VB

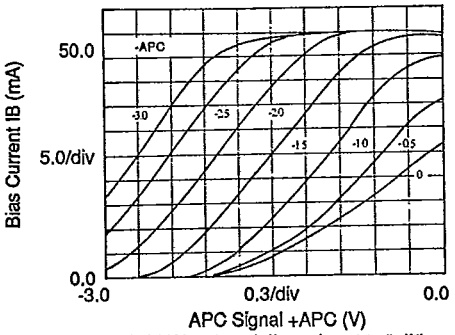


Input is set to "off" (-IN = -0.8V, +IN = -1.8V)
Bias Current is set to max. (+APC = 0.0V, -APC = -2.0V)

4) Bias current control by APC voltage



IBMAX = 10 mA (Input is set to "off")



IBMAX = 50 mA (Input is set to "off")

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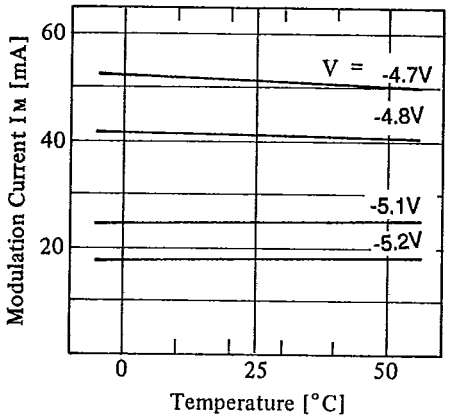
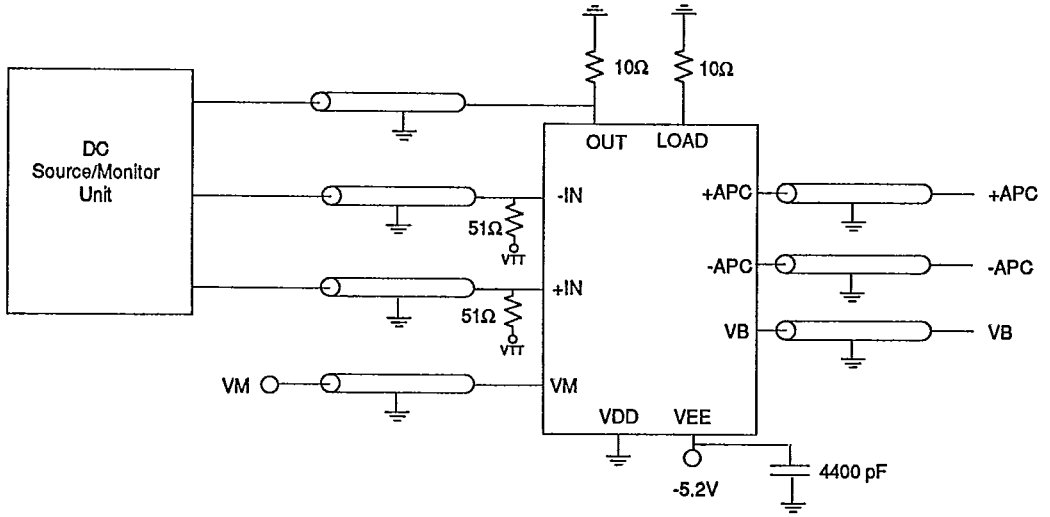
TYPICAL DC CHARACTERISTICS (Cont.)

5) Dependence of Modulation Current on the Ambient Temperature



Input is set to "on" (-IN = -1.8V, +IN = -0.8V)
Bias current is cut by APC signal
(+APC = -2.0V, -APC = 0.0V)

6) Measurement Block Diagram



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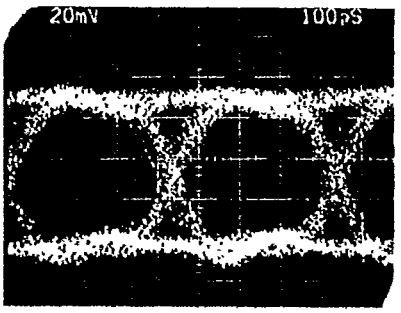
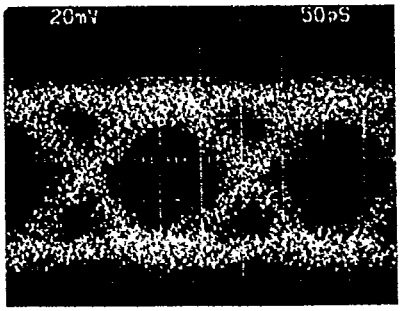
PSEUDO-RANDOM DATA RESPONSE OF ELECTRICAL OUTPUT

1) Eye Diagram (25Ω Load): 16G075-3L1

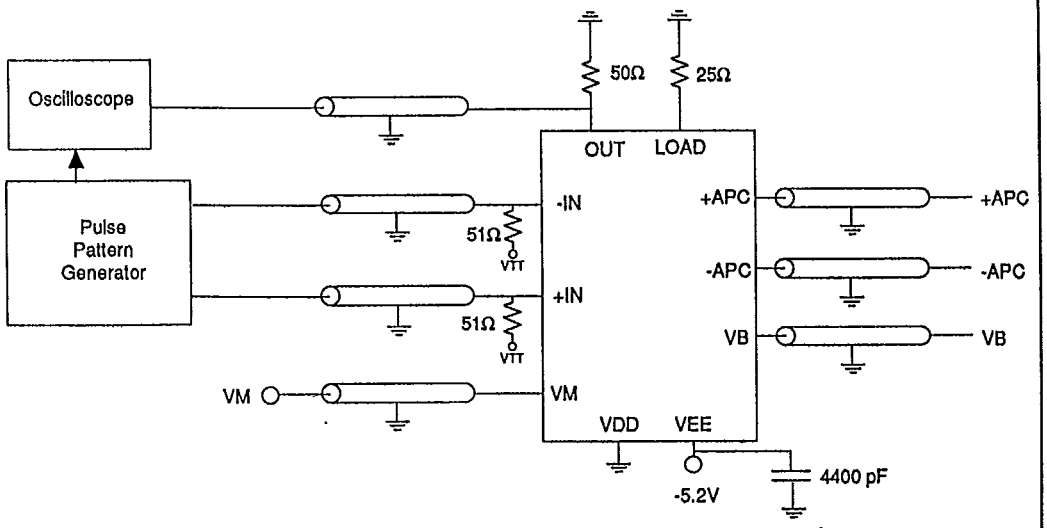


a) Response to 2.5Gbps NRZ single mode input
(+IN = -1.3V, -IN = 1.0Vp-p)



b) Response to 5.0Gbps NRZ single mode input
(+IN = -1.3V, -IN = 1.0Vp-p)

2) Measurement Block Diagram



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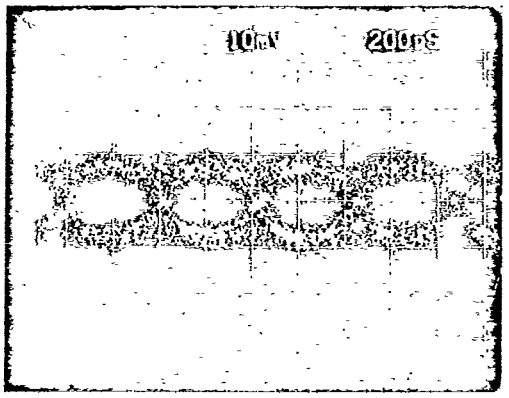
GigaBit Logic **16G075**

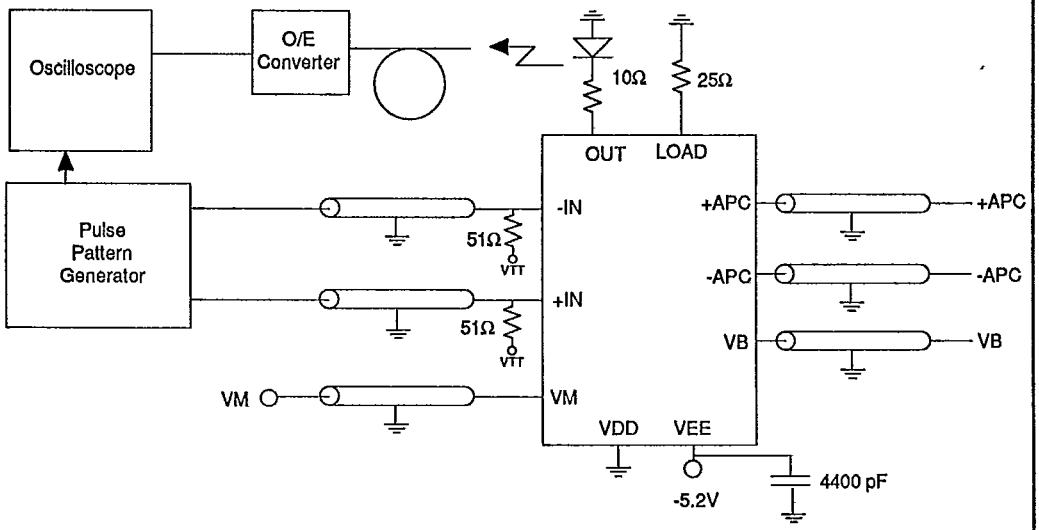
PSEUDO -RANDOM DATA RESPONSE OF OPTICAL OUTPUT

1) Eye Diagram (2.4 Gbps NRZ)



IC: 16G075-3L1
Laser Diode: MITSUBISHI FU-63SDF

2) Measurement Block Diagram



NOTE: The 10Ω and 25Ω resistors in series with OUT and LOAD respectively are damping resistors. Their values are selected to minimize ringing caused by the impedance mismatch to the laser diode. These values may change depending upon the type of laser diode used.

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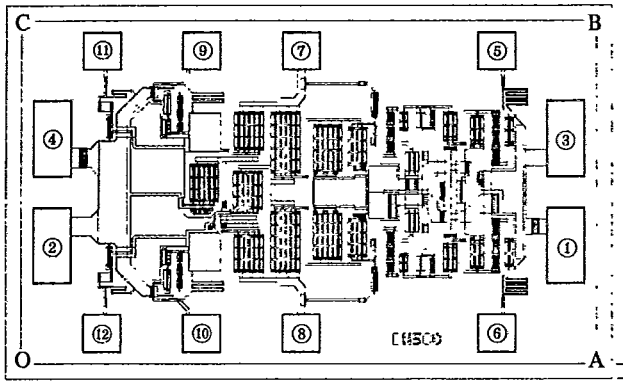
DIE PAD ASSIGNMENTS (16G075-NX)

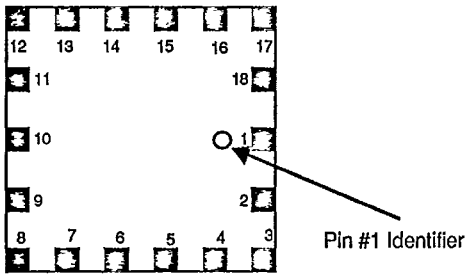


Thickness 450 µm

The point O designates the origin of the drawing.

	Pad	Center Position (µm)		Pad	Center Position (µm)
1	VDD1	(1420, 310)	7	OUT	(730, 820)
2	VDD2	(80, 590)	8	LOAD	(730, 80)
3	VEE1	(1420, 590)	9	+APC	(470, 820)
4	VEE2	(80, 310)	10	-APC	(470, 80)
5	-IN	(1240, 820)	11	VB	(210, 820)
6	+IN	(1240, 80)	12	VM	(210, 80)
A		(1500, 0)			
B		(1500, 900)	Pad Size 1 ~ 4: 100 µm x 200 µm 5 ~ 12: 100 µm sq.		
C		(0, 900)			

PIN ASSIGNMENTS (BOTTOM VIEW)



Pin	Connection	Pin	Connection
1	OUT	10	LOAD
2	NC	11	NC
3	+APC	12	+IN
4	VB	13	VDD1
5	VEE2	14	NC
6	VDD2	15	NC
7	VM	16	VEE1
8	-APC	17	-IN
9	NC	18	GND

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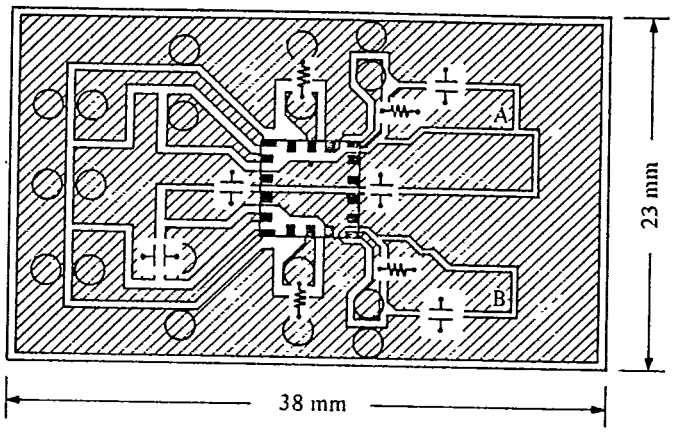
USER'S GUIDE FOR EVALUATION BOARD

1) Board Layout



The open circles indicate soldering positions for coaxial cables.
Islands A and B are termination resistors bias points. When driven from PicoLogic, they should be connected to -2V. Otherwise, they may be connected to ground.

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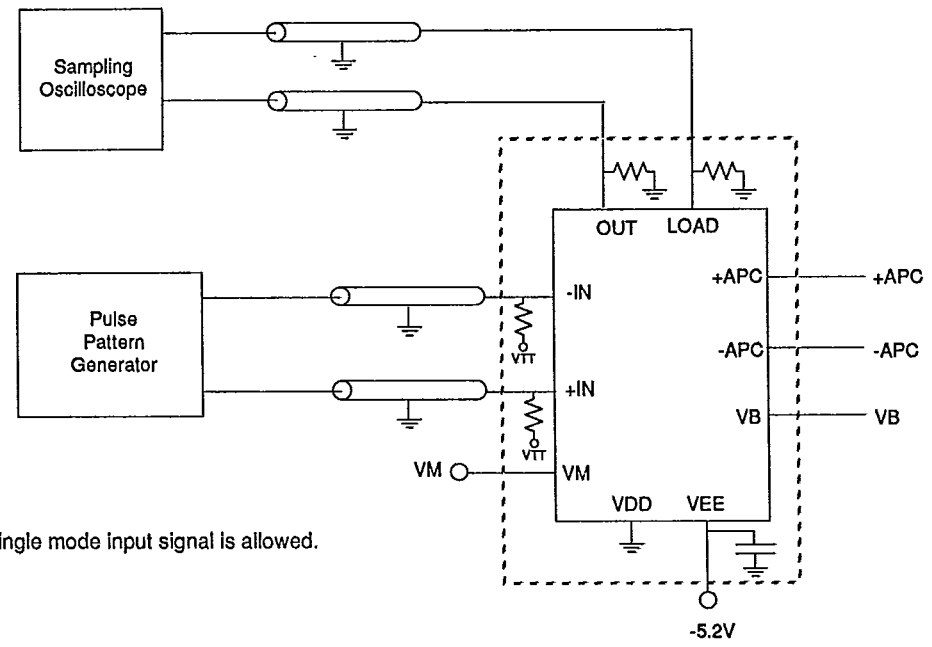
USER'S GUIDE FOR EVALUATION BOARD (Cont.)

2) Measurement Block Diagram

R: 51Ω
C: 4400pF



Single mode input signal is allowed.

PRECAUTIONS

Owing to their small dimensions, the GaAs FETs from which the 16G075 is designed can be damaged or destroyed if subjected to large transient voltages.

Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static electricity charged operators or ungrounded equipment. To prevent damage to devices from transient breakdown:

- DC ground all equipment and operators.
- Avoid excessive voltage transients when turning power supplies on.

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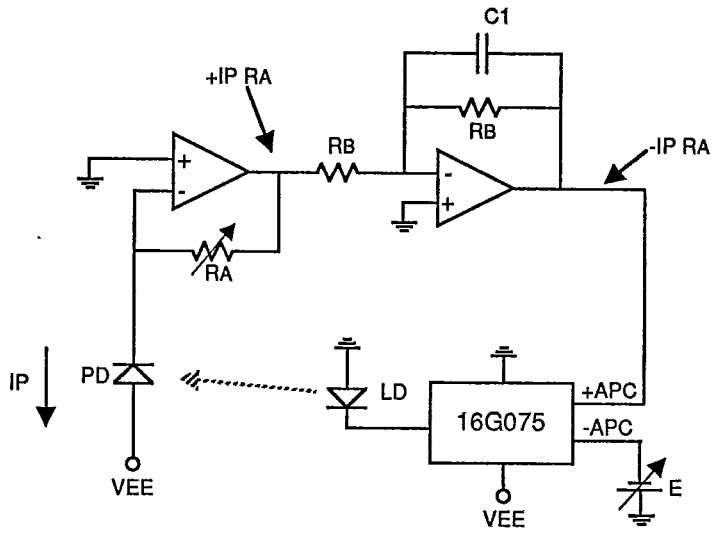
AUTOMATIC POWER CONTROL (APC) CIRCUIT DESIGN EXAMPLE



• EQUATIONS:

$$E(-APC) = -\frac{LRA}{Cm}$$

Where:

L = Light Power (W)
Cm = Monitor Efficiency = $\frac{L}{IP}$ (light power / monitor current) (W/A)
RA = Load Resistance
E = Reference Voltage

• EXAMPLE:

IC: LM324
RA: 4.5KΩ
RB: 100KΩ
C1: 0.1μF
VEE = -5.2V

L = 1 mW
Cm = 3.3 W/A

∴ E(-APC) = -1.35V

T-90-20

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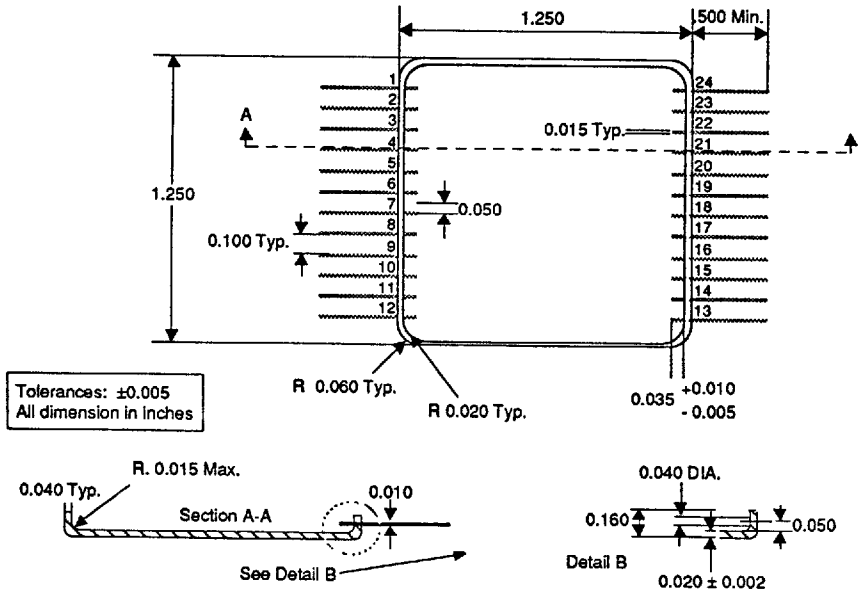
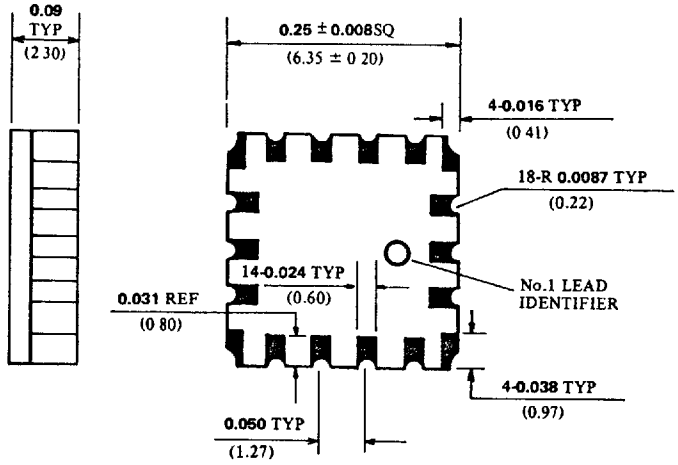
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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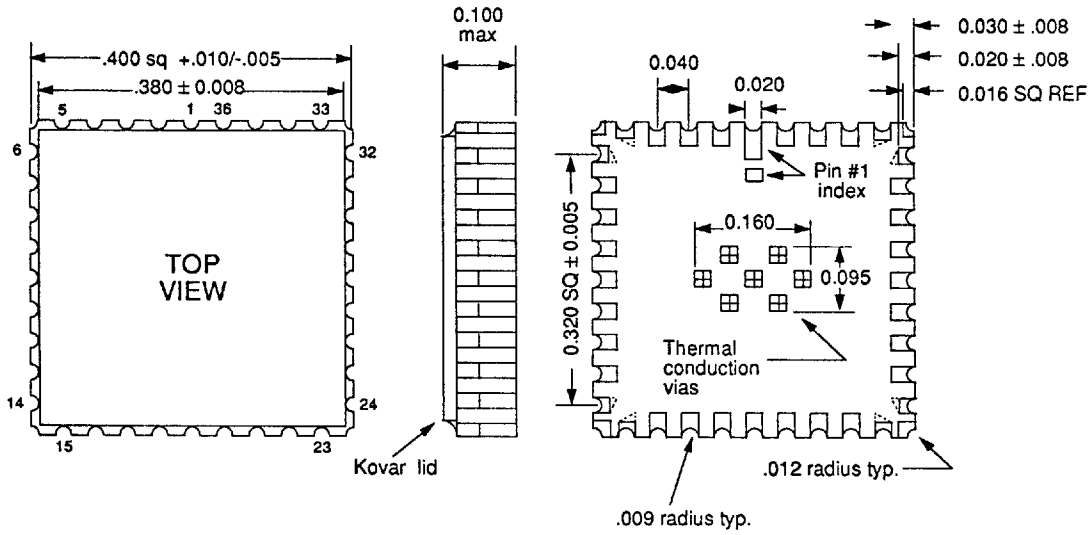
GigaBit Logic

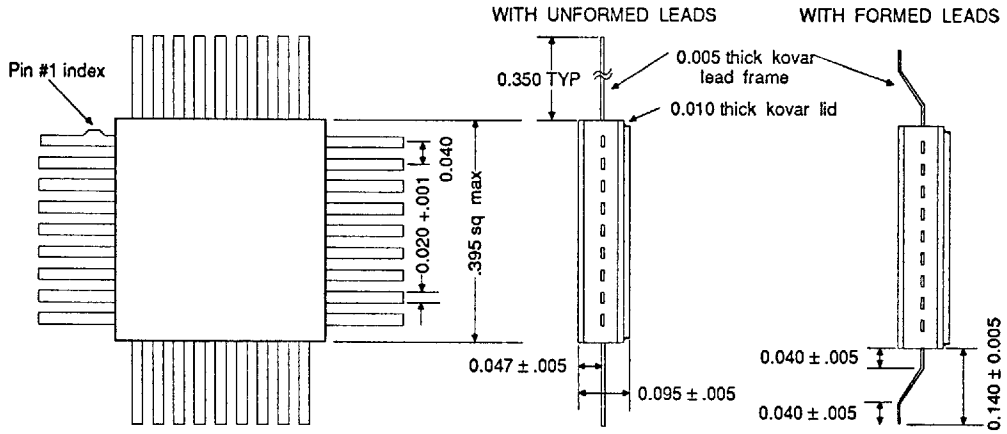
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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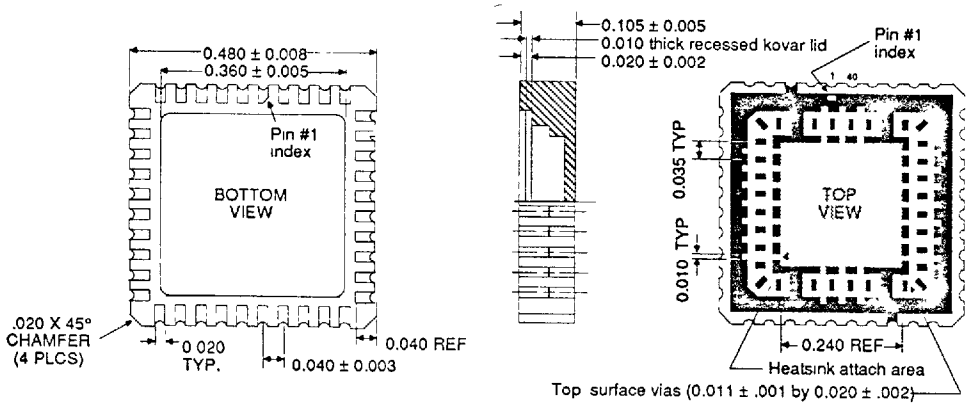
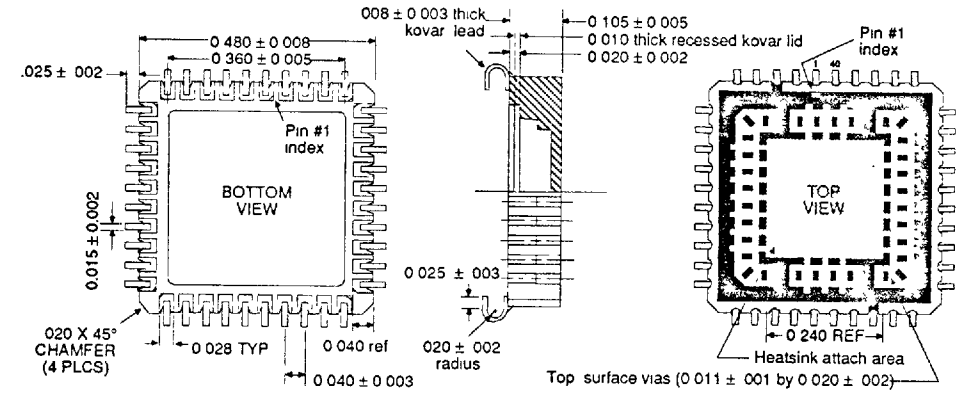
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

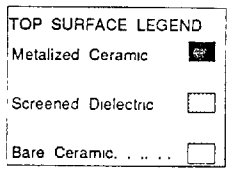


40 PIN LEADED CHIP CARRIER
TYPE C

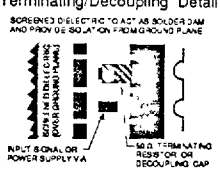


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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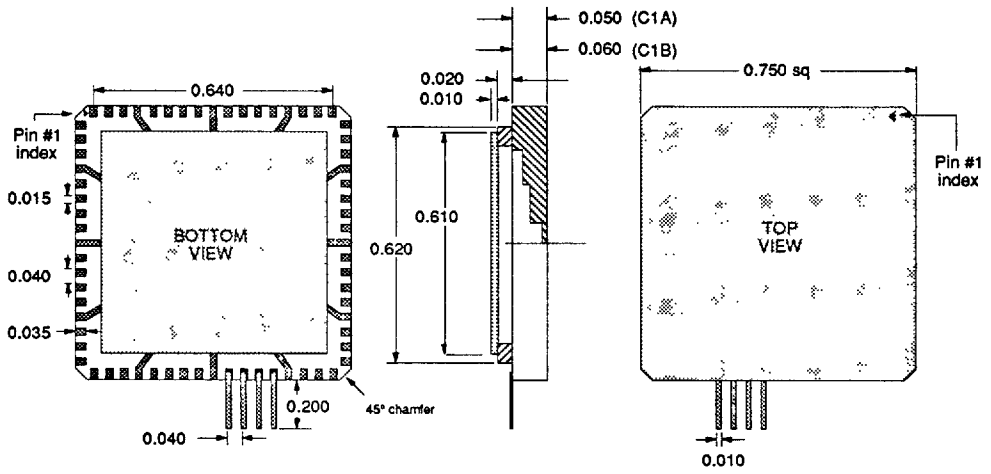
GigaBit Logic

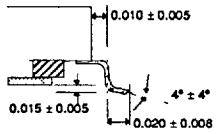
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3