General Description

BW2017X is a Phase-Locked Loop (PLL) frequency synthesizer implemented in 0.35um CMOS technology.
The PLL provides frequency multiplication capability.
The output clock frequency Fout is related to the reference input clock frequency Fin by the following equation:

$$Fout = \frac{M \times Fin}{P \times S}$$

where

Fout : output clock frequency.
Fin : reference input clock frequency.
M, P and S : values of programmable dividers.

BW2017X consists of a phase and frequency detector(PFD), a charge pump, an external loop filter, a voltage controlled oscillator(VCO), a 4bit pre-divider P, an 8bit main divider M and a 2bit post scaler S, and a lock detector as shown in Figure1

Features

- 0.35um CMOS technology
- 3.3V Single power supply
- Output frequency range: 3 ~ 25MHz
- Cycle Jitter: ±300ps
- Duty ratio: 40% ~ 60%
- Frequency change by programmable divider
- Power down mode

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

FUNCTIONAL BLOCK DIAGRAM

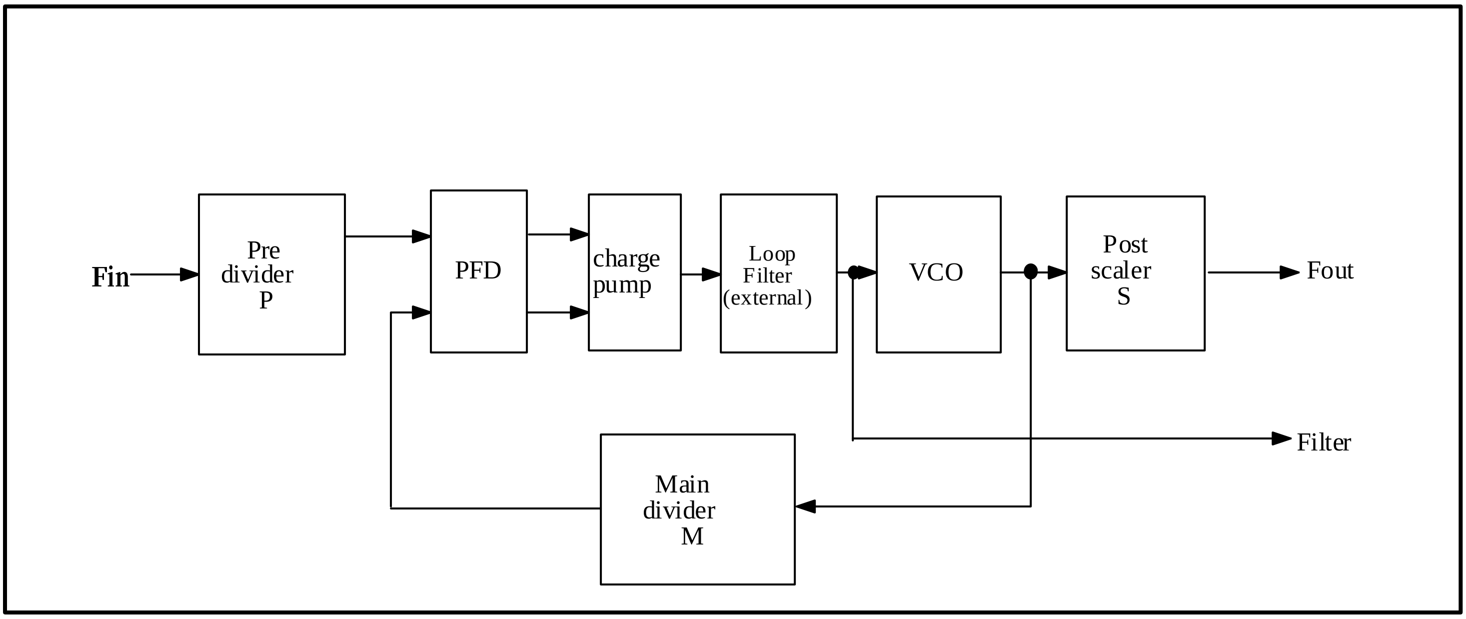


Figure 1. BW2017X Block Diagram

CORE PIN DESCRIPTIONS

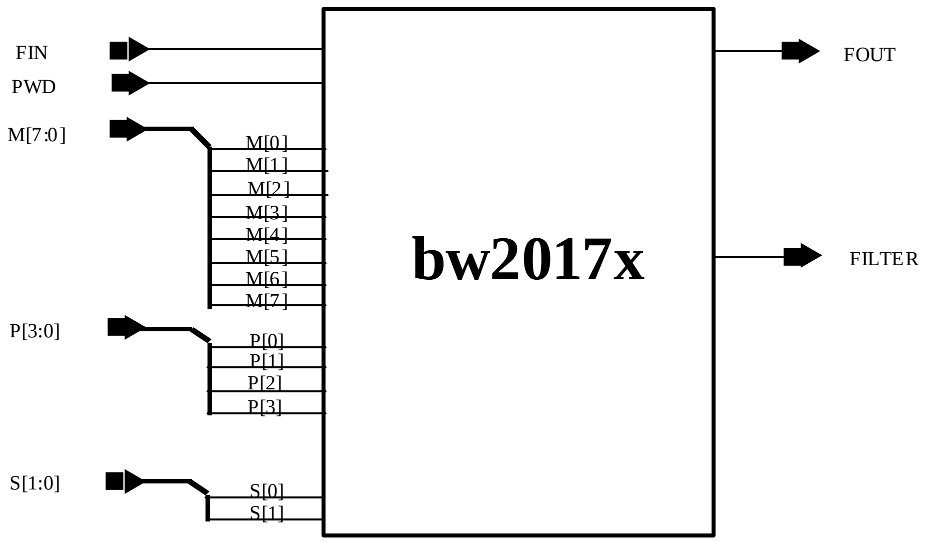
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VDD	DP	vddd	Digital power supply
VSS	DG	vssd	Digital ground
VDDA	AP	vdda	Analog power supply
VSSA	AG	vssa	Analog ground
VBB	AB/DB	vbba	Analog / Digital Sub Bias
FIN	DI	picc_bb	PLL clock input
FOUT	DO	pot12_bb	3 ~ 25MHz clock output
FILTER	DO	poar50_bb	-Charge pump output is connected to loop filter. -A capacitor is connected between the pin and analog ground.
PWD	DI	picc_bb	FSPLL clock power down. -PWD is active HIGH. -If NOT used, tie it to VSSD.
P[3:0]	DI	picc_bb	The values for 4bit programmable pre-divider.
M[7:0]	DI	picc_bb	The values for 8bit programmable main divider.
S[1:0]	DI	picc_bb	The values for 2bit programmable post scaler.

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- AB : Analog Sub Bias
- DP : Digital Power
- DG : Digital Ground
- DB : Digital Sub Vias

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	Symbol	Value	Unit	Applicable pin
Supply Voltage	VDD VDDA	-0.3 to 3.8	V	VDD,VSS VDDA,VSSA,VBB
Voltage on any digital pin	Vin	VSS-0.3 to VDD+0.3	V	P[3:0],M[7:0],S[1:0] PWD
Storage Temperature	Tstg	-45 to 125	℃	-

NOTE:
1. ABSOLUTE MAXIMUM RATINGS specify the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

Recommended Operating Conditions

	Symbol	Min	Typ	Max	Unit
Supply Voltage Differential	VDD - VDDA	-0.1		0.1	V
External Loop Filter Capacitance	L_F		940		pF
Operating Temperature	Topr	0		70	℃

NOTE:
1. It is strongly recommended that all the supply pins (VDDA, VDD) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

	Symbol	**Min**	**Typ**	**Max**	**Unit**
Operating Voltage	VDD,VDDA	3.15	3.3	3.45	V
Digital Input Voltage High	V_{IH}	2.0			V
Digital Input Voltage Low	V_{IL}			0.8	V
Dynamic Current (CORE Level without I/O Cell)	Idd			2	mA
Power Down Current	Ipd			50	uA

AC ELECTRICAL CHARACTERISTICS

	Symbol	Min	Typ	Max	Unit
Input Frequency	F_{IN}		4		MHz
Output Clock Frequency	F_{OUT}	3		25	MHz
Input Clock Duty Cycle	T_{ID}	40		60	%
Output Clock Duty Cycle (at 25MHz)	T_{OD}	40		60	%
Input Glitch Pulse Width	T_{IGP}	1			ns
Lock Time	T_{LT}			300	us
Cycle to Cycle Jitter	T_{JCC}	-300		+300	ps

FUNCTIONAL DESCRIPTION

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

. The voltage-controlled oscillator to generate the output frequency
. The pre-divider P divides the reference frequency by P.
. The main divider M divides the VCO output frequency by M.
. The post scaler S divides the VCO output frequency by S.
. The phase and frequency detector (PFD) detects the phase and frequency difference between the reference input and VCO output (after M division) and controls the charge pump current.
. The loop filter removes high frequency components in VCO control voltage and does smooth and correct control of VCO.
. The M, P, and S values can be programmed by 14bit digital data from the external source. Thus the PLL can be locked onto the desired frequency.

$$Fout = \frac{M \times Fin}{P \times S}$$

If Fin = 4MHz, and M=m+8 , P=p+2, S=2^s

Digital data format:

Main Divider	**Pre Divider**	**Post Scaler**
M7,M6,M5,M4,M3,M2,M1,M0	P3,P2,P1,P0	S1,S0

NOTE:
. S1 - S0 : Output Frequency Scaler
. M7 - M0 : VCO Frequency Divider
. P3 - P0 : Reference Frequency Input Divider

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

CORE EVALUATION GUIDE

For an embedded PLL, we must consider test circuit for the embedded core in multiple applications. Hence the following requirements should be satisfied.

- FOUT pin must be bypassed for external test.
- For the PLL test (below two examples),
  it is needed to control the dividers - M[7:0],P[3:0] and S[1:0] -that generate multiple frequencies.
  Example #1. Registers can be used for easy control of divider values.
  Example #2. N sample bits of 14-bit divider pins can be bypassed for test using MUX.

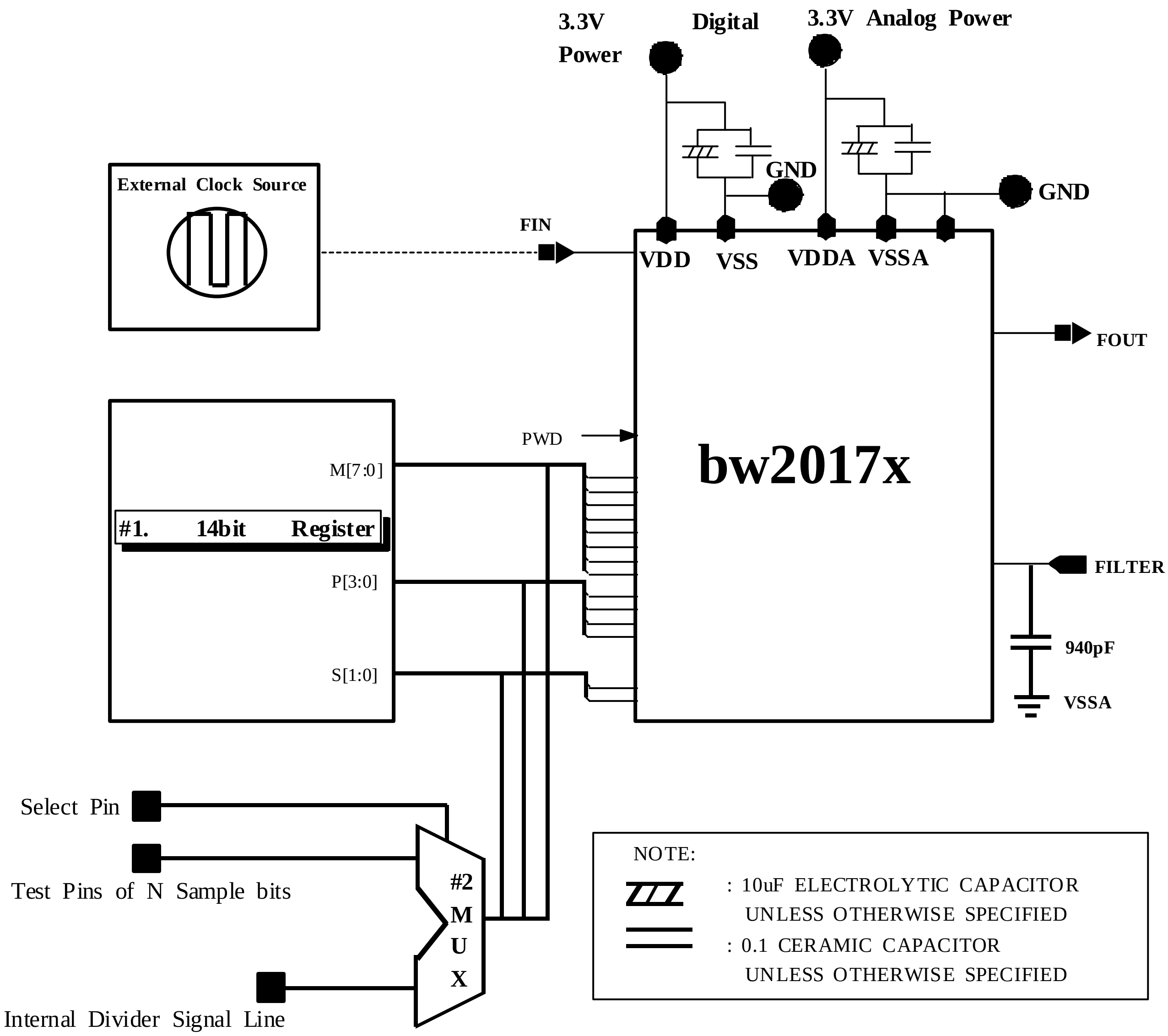


Fig.3 BW2017X Core Test Scheme

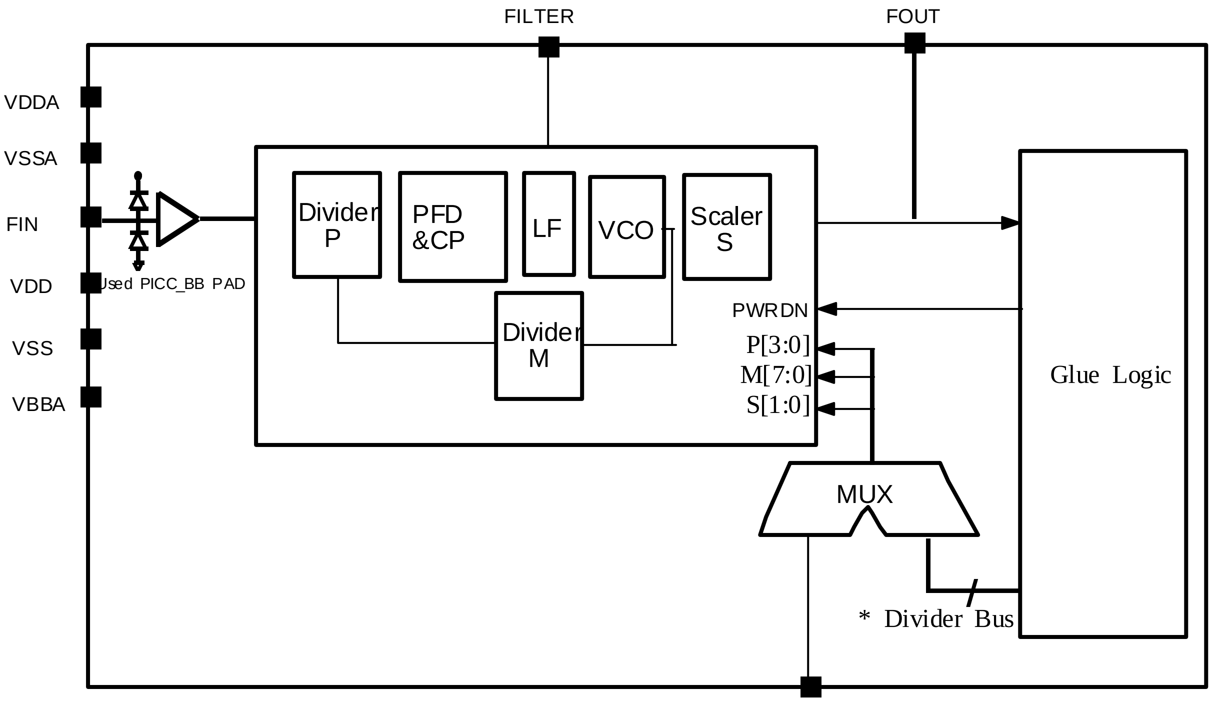
CORE LAYOUT GUIDE

- The digital power(VDD,VSS) and the analog power(VDDA,VSSA) must be dedicated only to PLL and be seperated. If the dedicated VDD and VSS is not available, that of the least power consuming block is shared with the PLL.
- The POA pad is used as a FILTER pad that contains ESD protection diodes without any resistors and buffers.
- The FOUT and FILTER pins must be placed far from the internal signals in order to prevent them from overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- The PLL core must be shielded by guard ring.
- For the FOUT, you can use a custom drive buffer or POT12 buffer considering the drive current.

WITHOUT XTAL-DRIVER USERS GUIDE

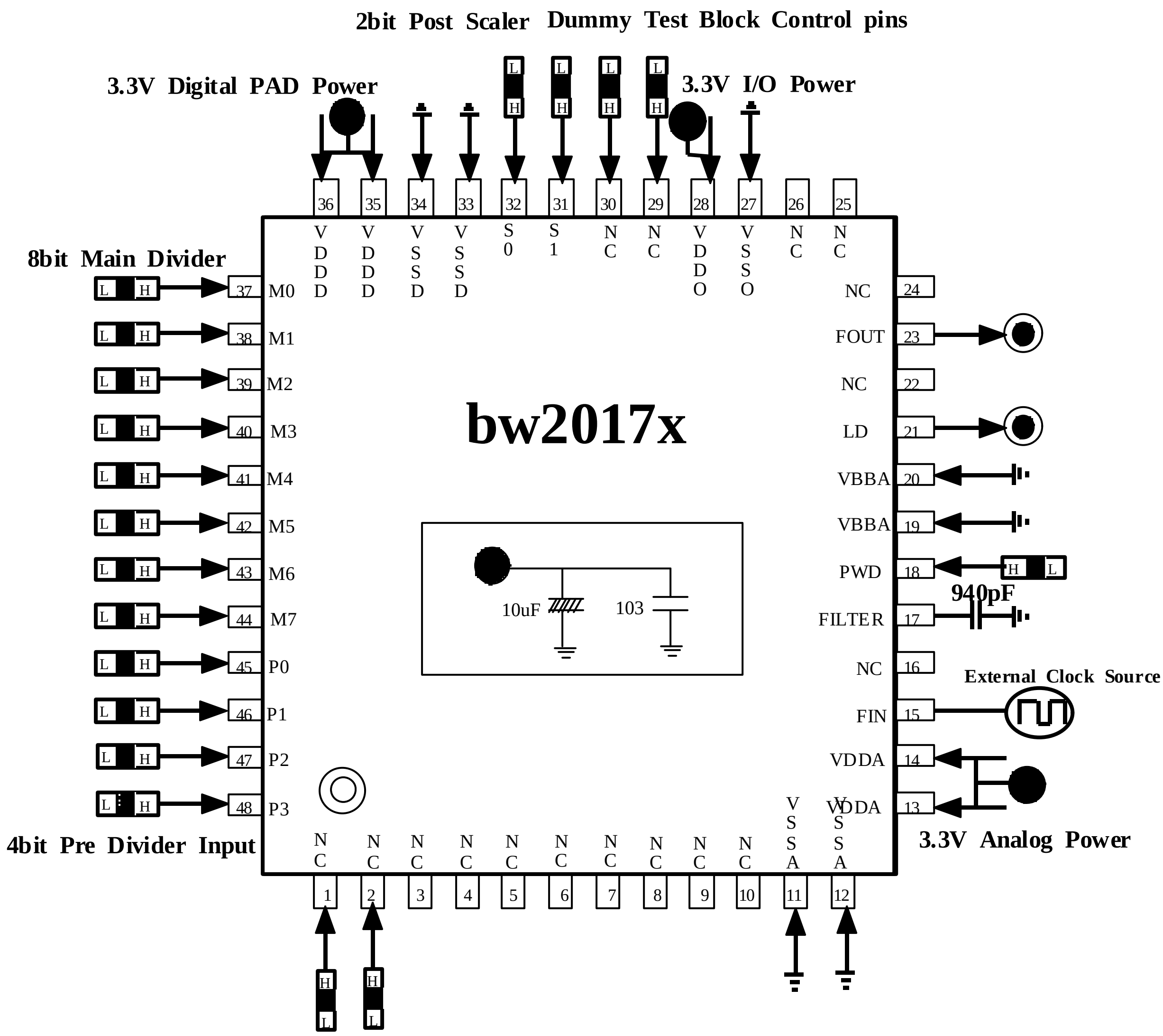
- There are two crystal driver cell (XTAL-OSC and PSOSCM2) options for the BW2017X PLL core.
  1. If the crystal component not used , an external clock source is applied to the FIN
     *Please contact an SEC application engineer when using a crystal.
  2. If the crystal component not used , an external clock I/O Buffer offered from Samsung's STD90 library is recommanded for use
  - When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
  * Without Xtal-driver : FIN,FILTER,FOUT,VDDA,VSSA,VDD and VSS.

Figure2. The example of PLL block without crystal component (Normal Case)



* Optional Test Pins

PACKAGE CONFIGURATION



NOTES
* NC is Noconnection pin
* LD is test pin of SEC

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
VDDD	35,36	DP	Digital power supply
VSSD	33,34	DG	Digital ground
PWD	18	DI	FSPLL clock power down -PWRDN is High, PLL do not operating under this condition. - If isn't used this pin, tied to VSS.
P[0]~P[3]	45~48	DI	Pre-Divider Input(LSB)
VDDA	13,14	AP	Analog power supply
VSSA	11,12	AG	Analog ground
VBBA	19,20	AB/DB	Analog / Digtal Sub Bias Power
FIN	15	AI	Crystal input or external F_{REF} input
FOUT	22	DO	3MHZ~25MHz clock output
FILTER	17	AO	Pump out is connected to the FILTER. A 940pF Capcitor is connected between the pin and analog pin
S[0]~S[1]	31,32	DI	Post scaler input
M[0]~M[7]	37~44	DI	8bit main divider input
VDDO	28	PP	I/O PAD Power
VSSO	27	PG	I/O PAD Ground

NOTES

1. I/O TYPE PP and PG denote PAD power and PAD ground respectively.

PLL Components

Figure 1 is a block diagram of the components of PLL: phase and frequency detector(PFD), charge pump, voltage controlled oscillator, and loop filter.
In SEC technology, the loop filter is implemented as external components close to chip.

Phase and Frequency Detector : The PFD monitors the phase and frequency difference between the Fref and Fvco, and generates control signals when it detects difference between the two.
If the Fref frequency is higher than the Fvco frequency, its falling edge occurs before(lead) the falling edge of the Fvco output. When this occurs the PFD signals the VCO to increase the frequency of the on-chip clock. If the falling edge of the Fref occurs after(lag) the falling edge of the Fvco output, the detector signals the VCO to decrease on-chip clock frequency. Figure3 illustrates the lead and lag conditions. If the frequencies of the Fref and Fvco are the same, the PFD does not generate control signals, so the frequencies remain constant.

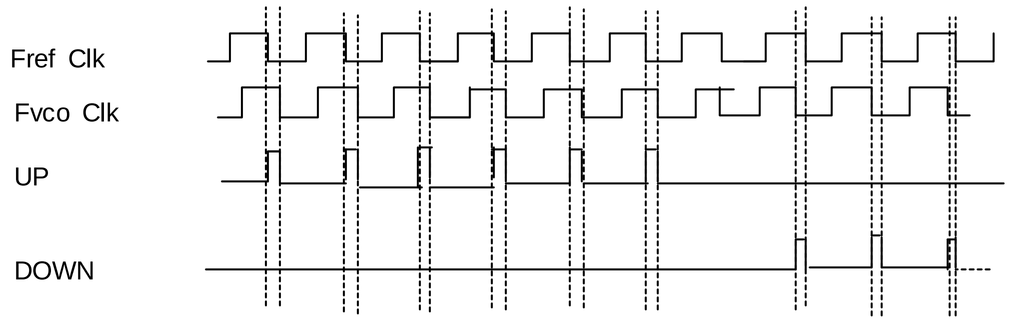


Figure3. Lead and Lag Clocking Relationships

Charge Pump : The charge pump converts a PFD control signal to electrical charge in voltage across the external filter that drives the VCO. As the VCO control voltage changes, the VCO frequency decreases or increases. If the control voltage remains constant, the frequency of the oscillator remains constant.

Loop Filter : The control signal that the PFD generates for the charge pump may generate large excursions(ripples) each time the VCO output is compared to the system clock. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. the filter is typically a two-pole RC lead-lag filter consisting of a resistor and two capacitors.

Voltage Controlled Oscillator(VCO) : The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease as a function of variations in voltage. When the VCO output matches the system clock in frequency and phase, the PFD stops sending a control signal to the charge pump, which in turn stabilizes the voltage applied to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock

Frequency Synthesis

Frequency synthesis uses the system clock as reference frequency to generate higher or lower frequencies for internal logic. For high speed applications in high-end designs, transmission line effects cause problems because of parasitics and impedance mismatch among various on-board components. These problems can be eliminated by isolating high frequency inside the chip. On-chip clocks faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider M is placed between the PFD and VCO as illustrated in Figure 1. The VCO frequency runs at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuation reduces the problem of interfacing to the system clock on a board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system.

Design Considerations

The following design considerations apply :

* Phase tolerance and jitter are independent of the PLL frequency.
* Jitter is affected by the noise frequency in the power(VDD,VSS,VDDA, and VSSA) . It increases when the noise level increases.
* A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL and ECL may degrade the tolerances.
* The use of two or more PLLs requires special design considerations. Please contact your application engineer for the detail.
* The following apply to the noise level, which can be minimized by selecting good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER(VDD,VSS, VDDA, and VSSA) connections to the PLL core. Seperate the traces from the chips' VDD/VSS/VDDA/VSSA supplies.
  - Use proper VDD/VSS/VDDA/VSSA decoupling method.
  - Use good power and ground sources on the board.
  - Use bulk power VBB to minimize substrate noise.
* The PLL core should be placed as close as possible to the dedicated loop filter and analog **Power and ground pins.**
* It is not desirable to put it close to the noise-generating signals such as data buses and high-current outputs near the PLL I/O cells.
* Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.

PLL Specifications

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
Supply Voltage					
Output frequency range					
Input frequency range					
Cycle to Cycle Jitter					
Lock time					
Dynamic current					
Stand by current					
Output clock duty ratio					
Long term jitter					
Output slew rate					

- Do you need XTAL driver buffer in PLL core?
  If you need it, what's the crystal frequency range? If not, What's the input frequency range when using a pre divider?

- Do you need the lock detector?
- Do you need the I/O cell of SEC?
- Do you need the external pin for PLL test?
- What's the main frequency & frequency range?
- How many FSPLLs do you need in your system?
- What's output loading?
- Could you illustrate external/internal pin configurations as required?

Specially requested function list :