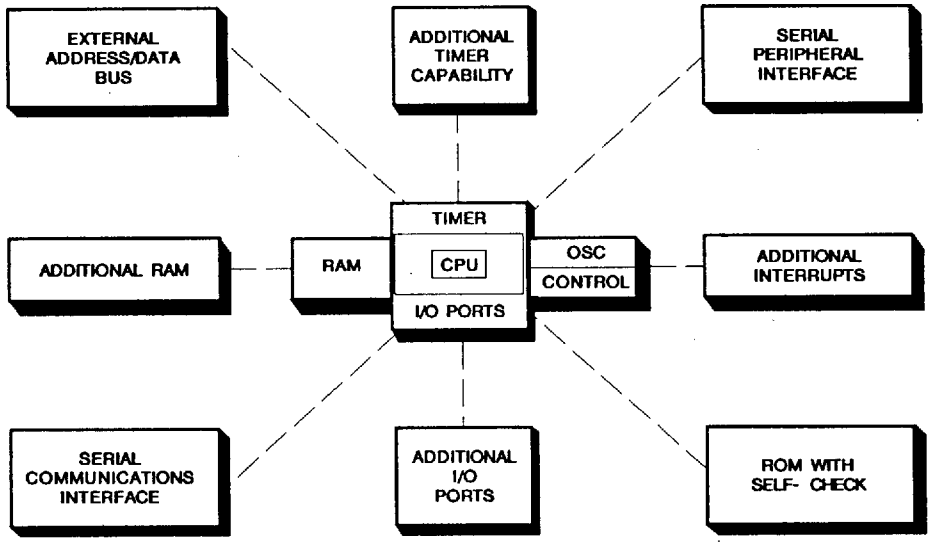
Standard Products

6805-Series Microcontrollers

All members of the Harris CDP6805 CMOS Family of MCUs are designed around a common core which consists of a CPU, timer, oscillator, control section (for interrupts and reset), bidirectional I/O lines, RAM, and ROM. This common core is expanded to provide versions of the CDP6805 with additional memory, I/O lines, interrupts, timer capability, and serial interfaces. This versatile common-core design offers five different CDP6805 CMOS Family micros that allow the user to choose the device best suited for a particular application.



CDP6805 CMOS FAMILY CORE ARCHITECTURE BLOCK DIAGRAM

General 6805 Family Features

Hardware

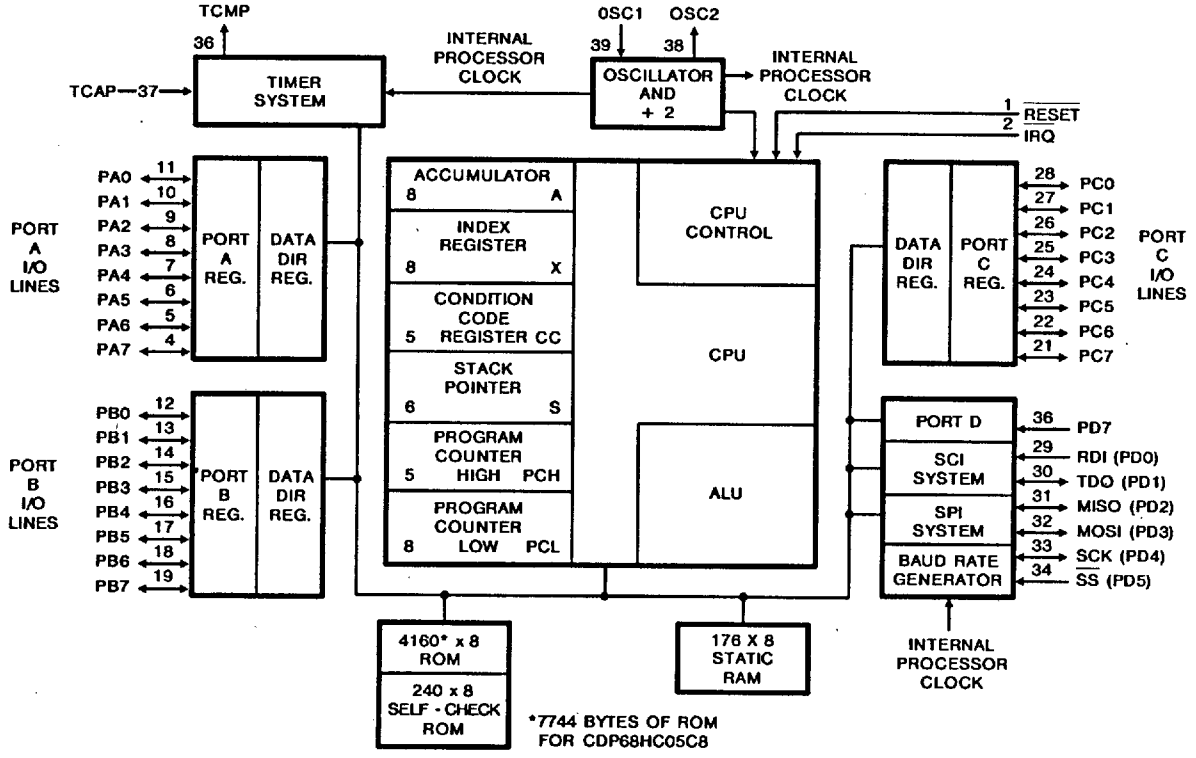
- 8-bit architecture
- Fully static operation
- Self-check mode
- Master Reset and Power-on Reset
- Single 3-6V power supply
- Power-saving Stop and Wait modes

Software

- Software compatible with entire 6805 family
- 61 instructions and 10 addressing modes
- Indexed addressing for tables
- True bit manipulation
- Memory-mapped I/O
- Efficient use of program space
- Versatile Interrupt handling
- 8 x 8 multiply instruction in C4, C8 and D2 versions.

Standard Products (Continued)

6805-Series Microcontrollers



MICROCOMPUTER BLOCK DIAGRAM (68HC05C4 VERSION SHOWN)

Comparison of CMOS CDP6805 Family Microcontrollers

Type	On-Chip RAM	On-Chip ROM	Max. Clock Freq. (MHz)	Instruction Time Min./Max. (µs)	Timer/ Counter Bits	Prescalers	Interrupts	I/O Lines	Serial Interface	Max. Operating Temp. Range (°C)	Package*
CDP6805F2 CDP6805F2C†	64	1089	4.0	2.0/10.00	8	Program	V	16	–	0 to 70	28D, 28E, 28Q
CDP6805G2 CDP6805G2C†	112	2106	4.0	2.0/10.00	8	Program	V	32	–	0 to 70	40D, 40E
CDP68C05D2○	96	2176	4.2	0.95/5.23	16	÷4	V	28	SPI	-40 to +125	40D, 40E, 44Q
CDP68C05C4○	176	4160	4.2	0.95/5.23	16	÷4	V	24	SPI/SCI	-40 to +125	40D, 40E, 44Q
CDP68C05C8○	176	7744	4.2	0.95/5.23	16	÷4	V	24	SPI/SCI	-40 to +125	40D, 40E, 44Q

V = Vectored address

† "C" version has -40°C to +85°C operating temperature range

○ Multiply instruction in the CDP68HC05C4, 68HC05C8 and 68HC05D2

* See interpretation guide and packaging section

Standard Products (Continued)

6805-Series Microcontrollers

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer Piggyback Emulators

The CDP68EM05C4 and CDP68EM05D2 are microcomputer emulator equivalents of the CDP68HC05C4 and CDP68HC05D2 CMOS microcomputers, respectively. Memory locations occupied by the on-chip ROM of the microcomputers are accessed as external locations with their emulator counterparts. The data bus, address bus, and control signals of the emulator devices are available externally to facilitate prototype development. The ceramic piggyback package of the emulator devices is designed to accept industry-standard, 28-pin EPROM memories (e.g., 27C64). This feature permits prototype development of systems for mask-programmed applications. The same microcomputer options for on-chip oscillator type, external interrupt sense, and crystal startup delay (D2 version only) are also available on the corresponding emulator devices. *

CDP68HC05C4 Features

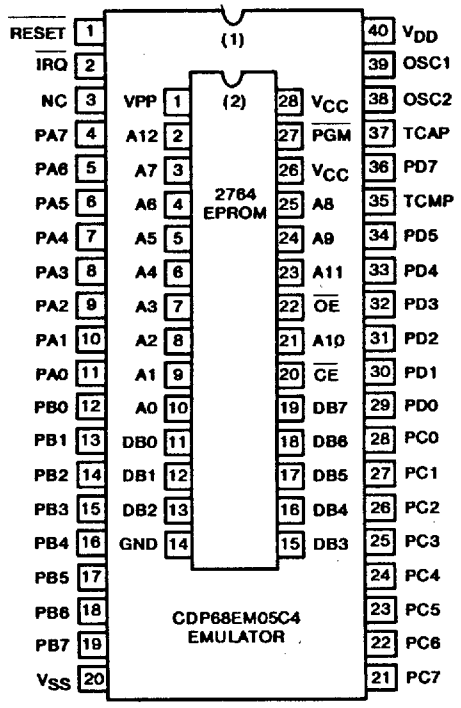
- All CDP68HC05C4 hardware and software features
- Un-multiplexed external address, data, and READ control lines
- Full 8K byte address space available (7984 bytes available externally)
- 176 bytes of on-chip RAM, no ROM
- Direct interface to industry-standard EPROMs
- 40-lead piggyback package (1) with 28-hole socket for 2764 EPROM (2)
- Also can be used for CDP68HC05C8 emulation

CDP68HC05D2 Features

- All CDP68HC05D2 hardware and software features
- Un-multiplexed external address, data, and READ control lines
- Full 8K byte address space available (8064 bytes available externally)
- 96 bytes of on-chip RAM, no ROM
- Direct interface to industry-standard EPROMs
- 40-lead piggyback package (1) with 28-hole socket for 2764 EPROM (2)

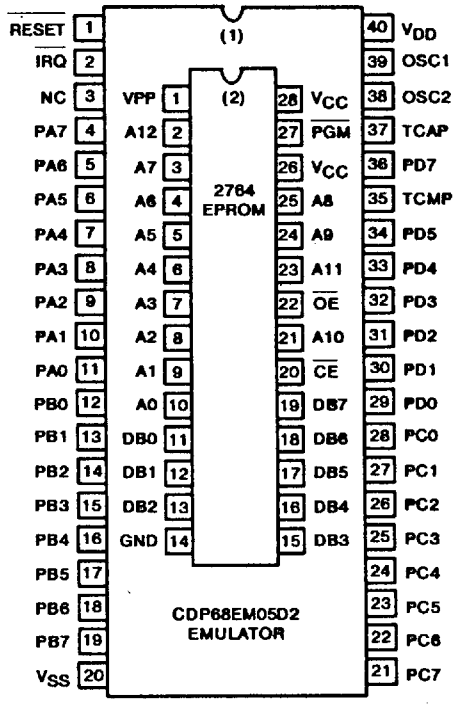
Terminal Assignment

40-LEAD PIGGYBACK
TOP VIEW



Terminal Assignment

40-LEAD PIGGYBACK
TOP VIEW



* Mask-Programming is not available thru Thomson Consumer Electronics