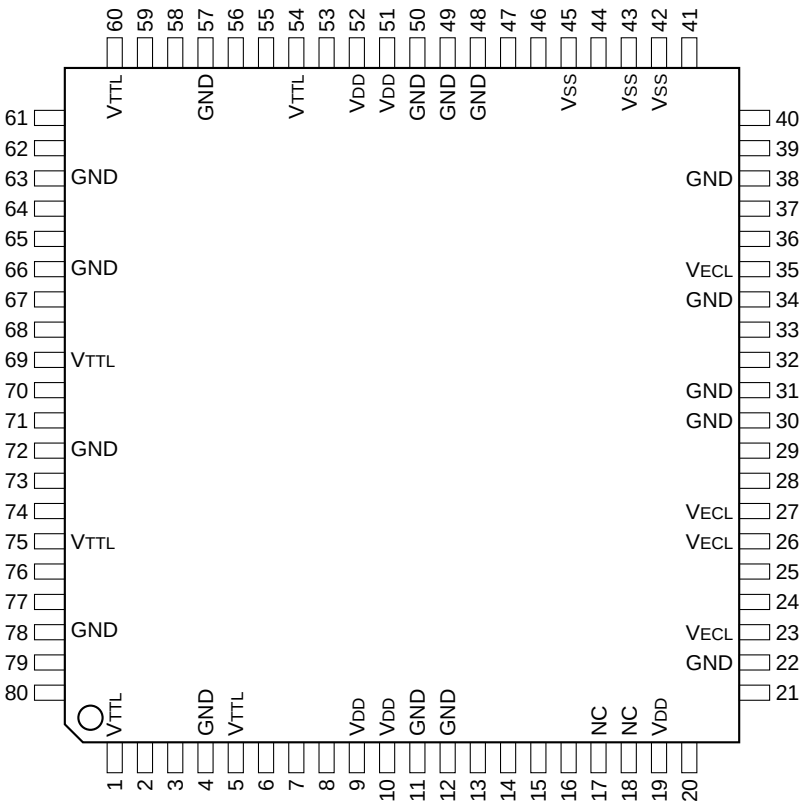
1.5 Gbps TRANSMITTER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VTTL	21	O	OPFDD	41	I	IB	61	I	ID04
2	I	ID18	22	—	GND	42	—	VSS	62	I	ID05
3	I	ID19	23	—	VECL	43	—	VSS	63	—	GND
4	—	GND	24	I	ICLK74N	44	O	OBM	64	I	ID06
5	—	VTTL	25	I	ICLK74	45	—	VSS	65	I	ID07
6	O	OCLK74T	26	—	VECL	46	O	OP	66	—	GND
7	I	XRST	27	—	VECL	47	O	OP	67	I	ID08
8	I	XTEST1	28	O	OCLK74EN	48	—	GND	68	I	ID09
9	—	VDD	29	O	OCLK74E	49	—	GND	69	—	VTTL
10	—	VDD	30	—	GND	50	—	GND	70	I	ID10
11	—	GND	31	—	GND	51	—	VDD	71	I	ID11
12	—	GND	32	I	TCLK148N	52	—	VDD	72	—	GND
13	I	ICNT0	33	I	TCLK148	53	I	ISD	73	I	ID12
14	I	ICNT1	34	—	GND	54	—	VTTL	74	I	ID13
15	I	ICNT2	35	—	VECL	55	I	ID00	75	—	VTTL
16	I	ICNT3	36	O	ODN	56	I	ID01	76	I	ID14
17	—	NC	37	O	OD	57	—	GND	77	I	ID15
18	—	NC	38	—	GND	58	I	ID02	78	—	GND
19	—	VDD	39	I	IREF	59	I	ID03	79	I	ID16
20	O	OPFDU	40	I	IP	60	—	VTTL	80	I	ID17

INPUTS

IB	:	LD DRIVER BIAS CURRENT CONTROL
ICLK74	:	PLL REFERENCE CLOCK (74.25 MHz)
ICLK74N	:	INVERTED PLL REFERENCE CLOCK (74.25 MHz)
ICNT0 - ICNT3	:	PARALLEL CLOCK DELAY CONTROL
ID00 - ID19	:	20 BITS PARALLEL SIGNAL
IP	:	LD DRIVER PEAK CURRENT CONTROL
IREF	:	LD DRIVER DUTY CONTROL
ISD	:	LD DRIVER OUTPUT CONTROL
TCLK148	:	EXTERNAL CLOCK (1.485 GHz)
TCLK148N	:	INVERTED EXTERNAL CLOCK (1.485 GHz)
XRST	:	RESET
XTEST1	:	SCRAMBLE/NRZ TO NRZI CONVERSION CONTROL

OUTPUTS

OBM	:	LD DRIVER BIAS CURRENT MONITOR
OCLK74E	:	74.25 MHz PARALLEL CLOCK (ECL LEVEL)
OCLK74EN	:	INVERTED 74.25 MHz PARALLEL CLOCK (ECL LEVEL)
OCLK74T	:	74.25 MHz PARALLEL CLOCK (LVTTL LEVEL)
OD	:	1.485 Gbps SERIAL DATA
ODN	:	INVERTED 1.485 Gbps SERIAL DATA
OP	:	LD DRIVER PEAK CURRENT
OPFDD	:	LOWER SIDE OF THE PHASE COMPARATOR (PFD)
OPFDU	:	UPPER SIDE OF THE PHASE COMPARATOR (PFD)