

EP600I

Classic EPLD

March 1995, ver. 2

Data Sheet Supplement

This data sheet supplement should be used together with the Classic Family Data Sheet and the Altera Device Package Outlines Data Sheet in the current data book.

Features

- Formerly Intel's 5C060 device
- High-performance, 16-macrocell Classic EPLD
 - Combinatorial speeds with $t_{PD} = 45$ ns
 - Counter frequencies up to 22.2 MHz
 - Pipelined data rates up to 26.3 MHz
- Pin-, function-, and programming file-compatible with Altera's EP610 EPLDs
- ☐ Programmable I/O architecture with up to 20 inputs or 16 outputs
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable plastic packages:
 - 24-pin dual in-line packages (CerDIP and PDIP)
 - 28-pin plastic J-lead chip carrier (PLCC)

www.DataSheet4U.com

Altera Corporation

Absolute Maximum Ratings

See Operating Requirements for Altera Devices in the current Altera Data Book.

Symbol	Parameter	Conditions	Min	Max	Unit
v _{cc}	Supply voltage	Note (1)	-2.0	7.0	V
V _t	DC input voltage	Notes (1), (2)	-0.5	V _{CC} + 0.5	V
T _{STG}	Storage temperature		-65	150	°C
T _{AMB}	Ambient temperature	Note (3)	-10	85	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage		4.75	5.25	V
Vi	input voltage		0	V _{cc}	V
٧o	Output voltage		0	V _{CC}	V
TA	Operating temperature	For commercial use	0	70	°C
TA	Operating temperature	For industrial use	-40	85	°C
T _C	Case temperature	For military use	-55	125	°C
t _R	Input rise time	Note (4)		500	ns
t _F	Input fall time	Note (4)		500	ns

DC Operating Conditions Note (5)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IH}	High-level input voltage	Note (6)	2.0		V _{CC} + 0.3	V
VIL	Low-level input voltage	Note (6)	-0.3		0.8	ν
V_{OH}	High-level output voltage	I _{OH} = -4 mA DC, V _{CC} = min	2.4			٧
VOL	Low-level output voltage	I _{OL} = 4 mA DC, V _{CC} = min			0.45	٧
I _I	Input leakage current	V _{CC} = max, GND < V _{IN} < V _{CC}	-10		10	μА
loz	Tri-state output off-state current	V _{CC} = max, GND < V _{OUT} < V _{CC}	-10		10	μА
I _{CC1}	V _{CC} supply current (non-turbo, standby)	$V_{CC} = max, V_{IN} = V_{CC} \text{ or GND},$ Note (7)		50	100	μА
I _{CC2}	V _{CC} supply current (non-turbo, active)	$V_{CC} = max$, $V_{IN} = V_{CC}$ or GND, no load, $f_{IN} = 1$ MHz, <i>Note (8)</i>		10	15	mA

Capacitance Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
CIN	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		20	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		20	pF
C _{CLK1}	CLK1 pin capacitance	V _{IN} = 0 V, f = 1.0 MHz		20	pF
C _{CLK2}	CLK2 pin capacitance	V _{IN} = 0 V, f = 1.0 MHz		50	pF

www.DataSheet4U.com

AC Operating Conditions Note (5)

External	ternal Timing Parameters			EP600I-45		01-55	Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
t _{PD1}	Input to non-registered output			43		53	25	ns
t _{PD2}	I/O input to non-registered output			45		55	25	ns
t _{PZX}	Input to output enable	Note (10)		45		55	25	пѕ
t _{PXZ}	Input to output disable	Note (10)		45		55	25	ns
t _{CLR}	Asynchronous output clear time			45		55	25	ns

Global (Clock Mode		EP60	01-45	EP600I-55		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
f _{MAX}	Maximum frequency	· · · · · · · · · · · · · · · · · · ·	26.3		23.3		0	MHz
t _{SU1}	Input setup time		36		41		25	ns
t _{SU2}	I/O setup time		38		43		25	ns
t _H	Input hold time		0		0		0	ns
t _{CH}	Clock high time		17.5		21.5		0	ns
t _{CL}	Clock low time		17.5		21.5		0	ns
tco	Clock to output delay			22		25	0	ns
t _{CNT}	Minimum clock period			45		55	25	ns
f _{CNT}	Internal maximum frequency		22.2		18.2		0	MHz

Array Cl	ock Mode		EP60	01-45	EP6001-55		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
f _{MAX}	Maximum frequency		28.6		23.3		0	MHz
t _{ASU1}	Input setup time		10		10		25	ns
t ASU2	I/O setup time		12		12		25	ns
t _{AH}	Input hold time		15		15		0	ns
t _{ACH}	Clock high time		17.5		21.5		25	ns
t _{ACL}	Clock low time		17.5		21.5		25	ns
t _{ACO}	Clock to output delay			50		58	25	ns
tACNT	Minimum clock period			45		55	25	ns
f _{ACNT}	Internal maximum frequency		22.2		18.2		0	MHz

www.DataSheet4U.com

Notes to tables:

(6)

- (1) Voltage is with respect to GND.
- (2) The minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to +7.0 V for periods less than 20 ns under no-load conditions.
- (3) This parameter is under bias. Extended temperature versions are also available.
- (4) For all Clocks: t_R and $t_F = 250$ ns (maximum).
- (5) Operating conditions: $T_A = 0^{\circ} \text{ C}$ to 70° C , $V_{CC} = 5.0 \text{ V} \pm 5\%$ for commercial use. $T_A = -40^{\circ} \text{ C}$ to 85° C , $V_{CC} = 5.0 \text{ V} \pm 10\%$ for industrial use. $T_C = -55^{\circ} \text{ C}$ to 125° C , $V_{CC} = 5.0 \text{ V} \pm 10\%$ for military use.
 - Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
- (7) When the Turbo Bit is not set (non-turbo mode), device enters standby mode approximately 100 ns after the last input transition.
- (8) Measured with a device programmed as a 16-bit counter.
- (9) When the Turbo Bit is not set (non-turbo mode), the non-turbo adder values must be added to the appropriate AC parameter to determine worst-case timing.
- (10) The t_{PZX} and t_{PXZ} parameters are measured at ± 0.5 V from steady state voltage as driven by the output load specification; t_{PZX} is measured with $C_L = 5$ pF.

Ordering Information

Package	Speed Grade	Product Grade (1)	Ordering Code
24-pin CerDIP	-45	Commercial	EP600IDC-45
24-pin CerDIP	-55	Commercial	EP600IDC-55
24-pin PDIP	-45	Commercial	EP600IPC-45
24-pin PDIP	-55	Commercial	EP6001PC-55
28-pin PLCC	-45	Commercial	EP600ILC-45
28-pin PLCC	-45	Industrial	EP6001LI-45
24-pin CerDIP	-55	MIL-STD-883B- Compliant, (2)	EP600IDM883B-55 5962-8686401LA

Notes:

- (1) Operating temperature: 0° C to 70° C for commercial use.
 - -40° C to 85° C for industrial use.
 - -55° C to 125° C for military use.
- (2) MIL-STD-883B-compliant product specifications are provided in this data sheet and in Military Product Drawings (MPDs). However, MPDs should be used to prepare Source Control Drawings (SCDs) and are available from Altera Marketing at (408) 894-7000. For more information on MPDs and SCDs, see the Military Products Data Sheet in the current Altera Data Book.



2610 Orchard Parkway San Jose, CA 95134-2020 (408) 894-7000 Applications Hotline: (800) 800-EPLD Marketing Information: (408) 894-7104 Literature Services: (408) 894-7144 Altera is a registered trademark of Altera Corporation. The following are trademarks of Altera Corporation Classic, EP600, EP6001. Altera acknowledges the trademarks of other organizations for their respective products or services mentioned in this document. Altera products marketed under trademarks are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

U.S. and European patents pending

Copyright © 1995 Altera Corporation