# 8 K × 8 Very Low Power CMOS SRAM

## Introduction

The HM 65664A is a very low power CMOS static RAM organized as 8192 × 8 bit. It is manufactured using the TEMIC high performance CMOS technology named super CMOS.

With this process, TEMIC is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as aerospace electronics or portable instruments and PC's.

Using an array or six transistors (6T) memory cells, the HM 65664A combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 25 ns over the full temperature range. The high stability of the 6T cell provides with excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.

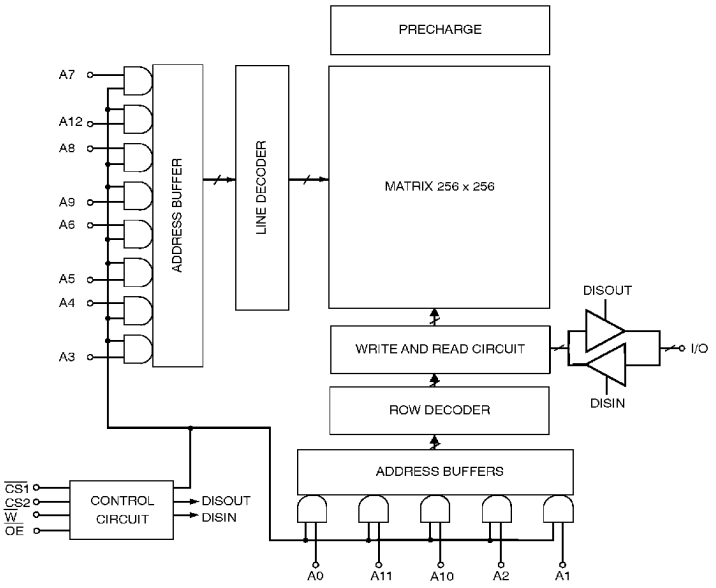
For military/space applications that demand superior levels of performance and reliability the HM 65664A is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

## Features

- Access Time
  Industrial/Commercial : 25/35/45/55 ns (max)
  Automotive/Military : 30/35/45/55 ns (max)
- Very Low Power Consumption
  Active : 175.0 mW (Typ)
  Standby : 0.5 µW (Typ)
  Data Retention : 0.4 µW (Typ)
- Wide Temperature Range : -55 To + 125°C
- 300 and 600 Mils Width Packages
- TTL Compatible Inputs and Outputs
- Asynchronous
- Single 5 Volt Supply
- Equal Cycle and Access Time
- Gated Inputs : No Pull-up/Down Resistors Are Required

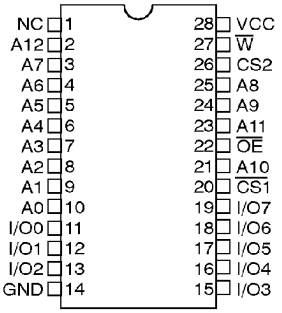
## Interface

### Block Diagram



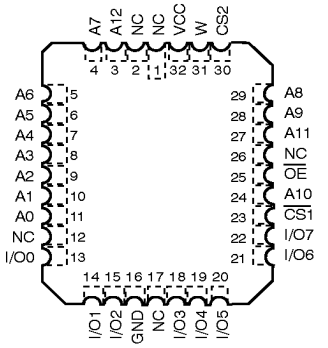
## Pin Configuration

Plastic 300 & 600 mils, 28 pins, DIL.
Ceramic 300 & 600 mils, 28 pins, DIL.
SOIC & SOJ 300 mils, 28 pins
SOIC 330 mils, 28 pins



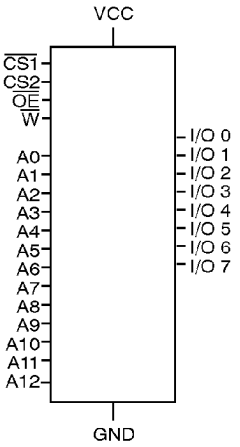

**Pinout DIL/SOJ 28 pins (top view)**

LCC, 32 pins.




**Pinout LCC 32 pins (top view)**

## Logic Symbol




## Pin Names

| | | | |
|---|---|---|---|
| A0–A12: Address inputs | | $\overline{CS1}$ | : Chip–select 1 |
| I/O0–I/O7 | : Input/Outputs | CS2 | : Chip–select 2 |
| VCC | : Power | $\overline{OE}$ | : Output Enable |
| GND | : Ground | $\overline{W}$ | : Write enable |

| $\overline{CS1}$ | CS2 | $\overline{OE}$ | $\overline{W}$ | DATA–IN | DATA–OUT | MODE |
|---|---|---|---|---|---|---|
| H | X | X | X | Z | Z | Deselect |
| L | H | L | H | Z | Valid | Read |
| L | H | X | L | Valid | Z | Write |
| L | H | H | H | Z | Z | Output disable |

L = low, H = high, X = H or L, Z = High impedance

# Electrical Characteristics

## Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . –0.5 V to +7.0 V
Input or Output voltage applied : . . . . (Gnd – 0.3 V) to (Vcc + 0.3 V)

Storage temperature : . . . . . –65°C to +150°C
Electro Static Discharge voltage > 2000 V
(MILSTD 883C method 3015.2)

## Operating Range

| | | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|---|
| Military | (– 2) | $V_{CC}$ ± 10 % | – 55°C to + 125°C |
| Automotive | (– A) | $V_{CC}$ ± 10 % | – 40°C to + ??? |
| Industrial | (– 9) | $V_{CC}$ ± 10 % | – 40°C to + 85°C |
| Commercial | (– 5) | $V_{CC}$ ± 10 % | 0°C to + 70°C |

## Recommended DC Operating Conditions

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL (1) | Input low voltage | – 0.3 | 0.0 | 0.8 | V |
| VIH | Input high voltage | 2.2 | – | Vcc + 0.3 V | V |

**Note :** 1. VIL min = –0.3 V or –1.0 V pulse width 50 ns.

## Capacitance

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Cin (2) | Input capacitance | – | – | 8 | pF |
| Cout (2) | Output capacitance | – | – | 8 | pF |

**Note :** 2. TA = 25°C, f = 1 MHz, VCC = 5.0 V, these parameters are not tested.

## DC Parameters

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| IIX (3) | Input leakage current | – 1.0 | – | 1.0 | µA |
| IOZ (3) | Output leakage current | – 1.0 | – | 1.0 | µA |
| VOL (4) | Output low voltage | – | – | 0.4 | V |
| VOH (4) | Output high voltage | 2.4 | – | – | V |

**Note :** 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc, output disabled, $\overline{CS}_1 \geq 2.2$ V or $\overline{CS}_2 \leq 0.8$ V.
4. Vcc min, IOL = 4.0 mA, IOH = –1.0 mA.

## Consumption for Commercial Specification (–5)

| SYMBOL | PARAMETER | 65664A U–5 | 65664A T–5 | 65664A G–5 | 65664A Q–5 | 65664A B–5 | 65664A S–5 | 65664A –5 | 65664A C–5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 10 | 15 | 10 | 15 | 10 | 15 | 10 | 15 | mA | max |
| ICCSB1 (6) | Standby supply current | 1 | 75 | 1 | 75 | 1 | 75 | 1 | 75 | µA | max |
| ICCOP (8) | Operating supply current | 70 | 80 | 65 | 75 | 65 | 75 | 65 | 75 | mA | max |

**Notes :** 5. $\overline{CS}1 \geq$ VIH and CS2 ≤ VIL.
6. $\overline{CS1} \geq$ Vcc – 0.3 V and CS2 ≤ 0.3 V, Iout = 0 mA.
7. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

## Consumption for Industrial Specification (–9)

| SYMBOL | PARAMETER | 65664A U–9 | 65664A T–9 | 65664A G–9 | 65664A Q–9 | 65664A B–9 | 65664A S–9 | 65664A –9 | 65664A C–9 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 15 | 20 | 15 | 20 | 15 | 20 | 15 | 20 | mA | max |
| ICCSB1 (6) | Standby supply current | 5 | 100 | 5 | 100 | 5 | 100 | 5 | 100 | µA | max |
| ICCOP (8) | Operating supply current | 75 | 100 | 75 | 100 | 75 | 100 | 75 | 100 | mA | max |

## Consumption for Automotive (–A) and Military (–2) Specifications

| SYMBOL | PARAMETER | 65664A G–2 | 65664A Q–2 | 65664A B–2 | 65664A S–2 | 65664A –2 | 65664A C–2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| ICCSB (5) | Standby supply current | 15 | 20 | 15 | 20 | 15 | 20 | mA | max |
| ICCSB1 (6) | Standby supply current | 50 | 500 | 50 | 500 | 50 | 500 | µA | max |
| IC-COP(7) | Operating supply current | 75 | 100 | 75 | 100 | 75 | 100 | mA | max |

**Notes :** 5. $\overline{CS1} \geq$ VIH and CS2 ≤ VIL.
6. $\overline{CS1} \geq$ Vcc – 0.3 V and CS2 ≤ 0.3 V, Iout = 0 mA.
7. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.

## AC Parameters

## AC Conditions

Input pulse levels : . . . . . Gnd to 3.0 V
Input rise : . . . . . 5 ns
Input timing reference levels : . . . . . 1.5 V
Output load : . . . . . 1 TTL gate + 30 pF

## AC Test Loads and Waveforms

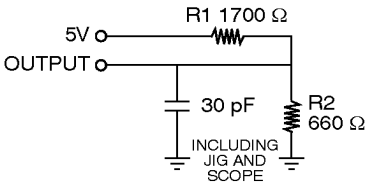



**Figure 1 a**

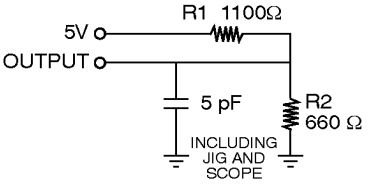



**Figure 1 b**

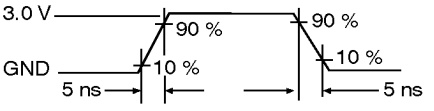
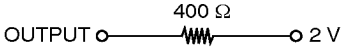



**Figure 2**

Equivalent to : THEVENIN EQUIVALENT

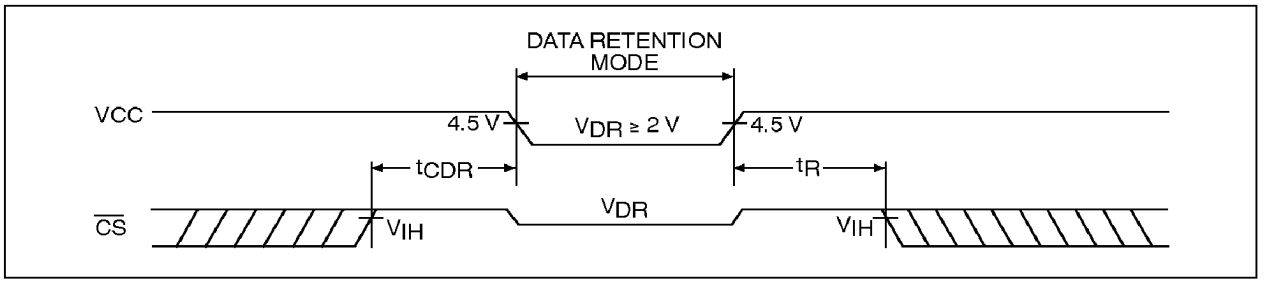


## Data Retention Mode

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc -0.2 V
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
2. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc -0.3 V and 70 % of Vcc during the power up and power down transitions
3. The RAM can begin operation > 45 ns after Vcc reaches the minimum operating voltage (4.5 V).

## Timing




## Data Retention Characteristics

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL (9) | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| VCCDR | Vcc for data retention | 2.0 | – | – | V |
| TCDR | Chip deselect to data retention time | 0.0 | – | – | ns |
| TR | Operation recovery time | TAVAV (10) | – | – | ns |
| ICCDR1(11) | Data retention current | | | | |
| | @2.0 V : HM-65664AB/G/U-5 | – | 0.1 | 0.5 | µA |
| | HM-65664AB/G/U-9 | – | 0.1 | 3.0 | µA |
| | HM-65664AB/G-2/-A | – | 0.1 | 20.0 | µA |
| | HM-65664AS/C/Q/T-5 | – | 0.1 | 30.0 | µA |
| | HM-65664AS/C/Q/T-9 | – | 0.1 | 30.0 | µA |
| | HM-65664AS/C/Q-2/-A | – | 0.1 | 200.0 | µA |
| ICCDR2(11) | Data retention current | | | | |
| | @2.0 V : HM-65664AB/G/U-5 | – | 0.3 | 1.0 | µA |
| | HM-65664AB/G/U-9 | – | 0.3 | 5.0 | µA |
| | HM-65664AB/G-2/-A | – | 0.3 | 30.0 | µA |
| | HM-65664AS/C/Q/T-5 | – | 0.3 | 50.0 | µA |
| | HM-65664AS/C/Q/T-9 | – | 0.3 | 50.0 | µA |
| | HM-65664AS/C/Q-2/-A | – | 0.3 | 300.0 | µA |

**Notes :** 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

## Write Cycle : Commercial Specification

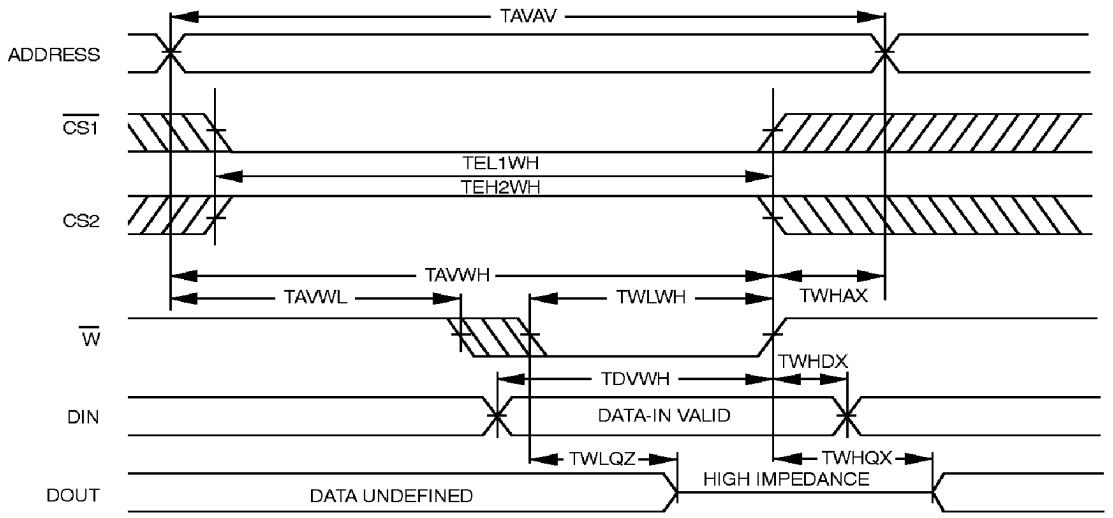
| SYMBOL | PARAMETER | 65664A U–5 | 65664A T–5 | 65664A G–5 | 65664A Q–5 | 65664A B–5 | 65664A S–5 | 65664A –5 | 65664A C–5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TAVWL | Address set–up time | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TDVWH | Data set–up time | 20 | 20 | 22 | 22 | 25 | 25 | 25 | 25 | ns | min |
| TEL1WH | $\overline{CS1}$ low to write end | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TEH2WH | CS2 low to write end | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TWLQZ (12) | Write low to high Z | 15 | 15 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |
| TWLWH | Write pulse width | 25 | 25 | 30 | 30 | 40 | 40 | 50 | 50 | ns | min |
| TWHAX | Address hold to end of write | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TWHDX | Data hold time | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | ns | min |
| TWHQX (12) | Write high to low Z | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |

## Write Cycle : Industrial, Automotive and Military Specifications

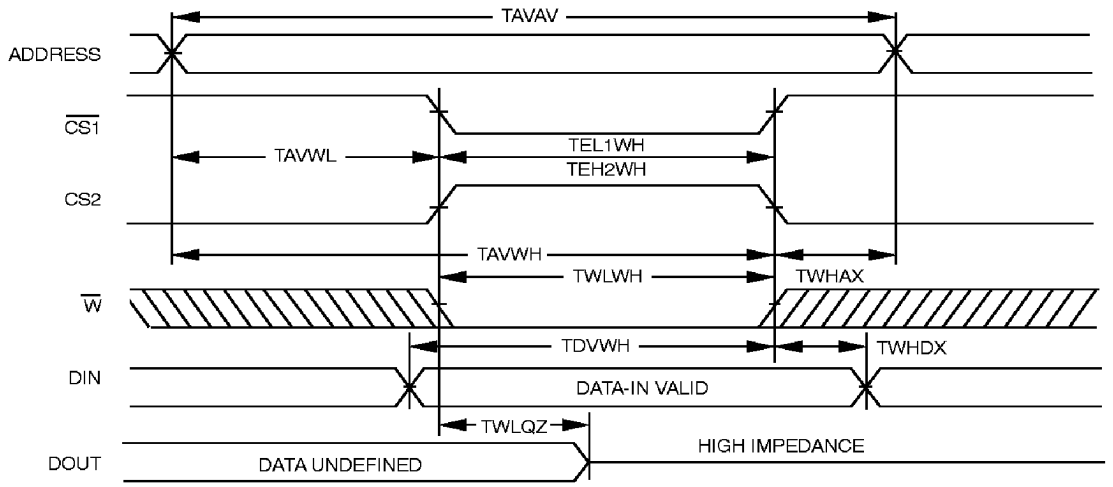
| SYMBOL | PARAMETER | 65664A U–9 | 65664A T–9 | 65664A G–9/–2 /–A | 65664A Q–9/–2 /–A | 65664A B–9/–2 /–A | 65664A S–9/–2 /–A | 65664A –9/–2 /–A | 65664A C–9/–2 /–A | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TAVWL | Address set–up time | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TDVWH | Data set–up time | 22 | 22 | 22 | 22 | 25 | 25 | 25 | 25 | ns | min |
| TEL1WH | $\overline{CS1}$ low to write end | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TEH2WH | CS2 low to write end | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TWLQZ (12) | Write low to high Z | 15 | 15 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |
| TWLWH | Write pulse width | 27 | 27 | 30 | 30 | 40 | 40 | 50 | 50 | ns | min |
| TWHAX | Address hold to end of write | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TWHDX | Data hold time | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | ns | min |
| TWHQX(12) | Write high to low Z | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | min |

**Note :** 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Write Cycle 1 $\overline{W}$ Controlled (note 13)




## Write Cycle 2 $\overline{CS}$ 1 Controlled (note 13)




**Note :** 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

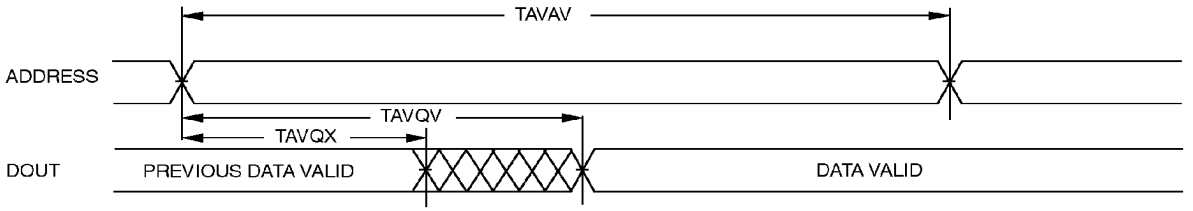
## Read Cycle : Commercial Specification

| SYMBOL | PARAMETER | 65664A U–5 | 65664A T–5 | 65664A G–5 | 65664A Q–5 | 65664A B–5 | 65664A S–5 | 65664A –5 | 65664A C–5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TAVQV | Address access time | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TAVQX | Address Valid to low Z | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | ns | min |
| TEL1QV | Chip–select 1 access time | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEH2QV | Chip–select 2 access time | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL1QX | $\overline{CS1}$ low to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEH2QX | CS2 to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEH1QZ | $\overline{CS1}$ high to high Z | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL2QZ | CS2 low to high Z | 25 | 25 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TGLQV | Output Enable access time | 12 | 12 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TGhQZ | $\overline{OE}$ high to high Z | 15 | 15 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |

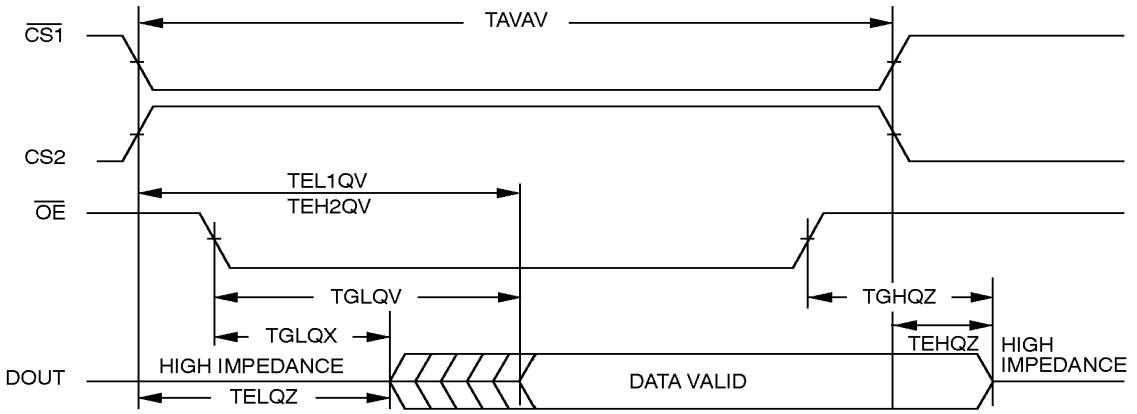
## Read Cycle : Industrial, Automotive and Military Specifications

| SYMBOL | PARAMETER | 65664A U–9 | 65664A T–9 | 65664A G–9/2/A | 65664A Q–9/2/A | 65664A B–9/2/A | 65664A S–9/2/A | 65664A –9/2/A | 65664A C–9/2/A | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | min |
| TAVQV | Address access time | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TAVQX | Address Valid to low Z | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | ns | min |
| TEL1QV | Chip–select 1 access time | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEH2QV | Chip–select 2 access time | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL1QX | $\overline{CS1}$ low to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEH2QX | CS2 to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEH1QZ | $\overline{CS1}$ high to high Z | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TEL2QZ | CS2 low to high Z | 30 | 30 | 35 | 35 | 45 | 45 | 55 | 55 | ns | max |
| TGLQV | Output Enable access time | 15 | 15 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 15 | 15 | 15 | 15 | 15 | 15 | 20 | 20 | ns | max |

## Read Cycle nb 1 (notes 16, 17)

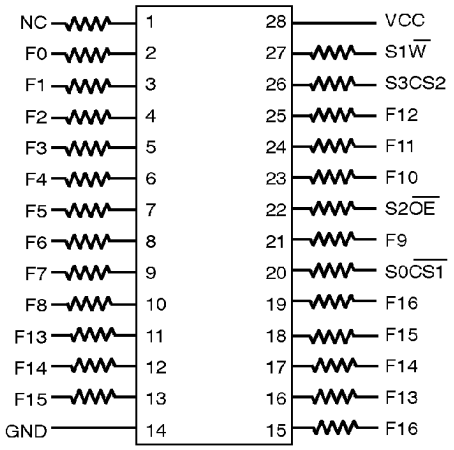


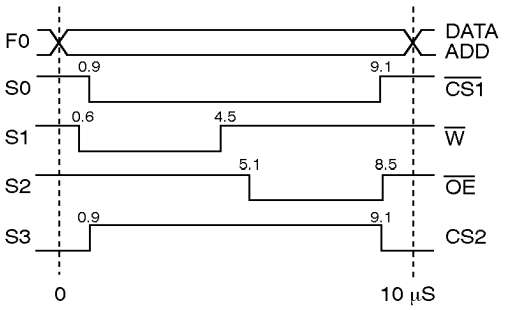

## Read Cycle nb 2 (notes 16, 18)




**Notes :** 16. $\overline{W}$ is high for read cycle.
17. Device is continuously selected, $\overline{CS1}$ & $\overline{OE}$ = VIL AND CS2 = VIH.
18. Address valid prior to or coincident with $\overline{CS}$ transition low.

## Burn-in Schematics




VCC = 5 V (–0, + 0.5)

R = 1 KΩ per pin

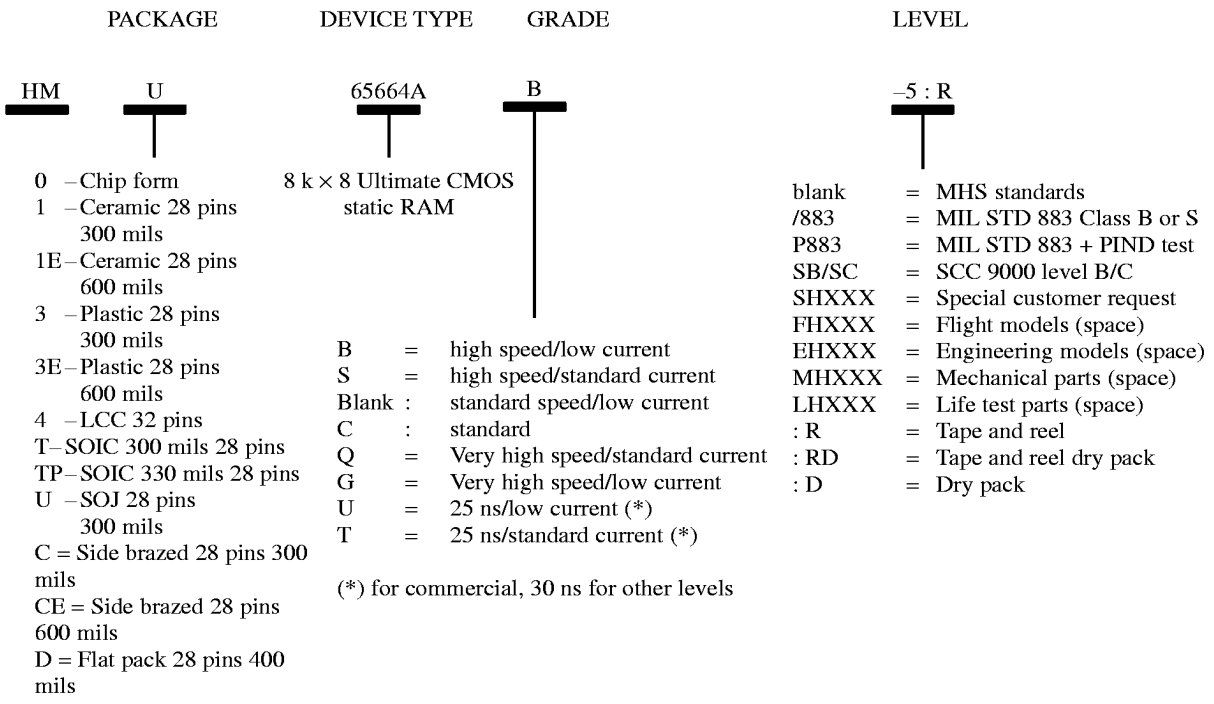
FO = 50 KHz ± 20%

Fn = 1/2 Fn – 1

SO to S3 : programmable signals for write/read cycles

NC : Not Connected

## Ordering Information




## Military and Space Versions

The following table gives package/consumption/access time/process flow available combinations

| Temp. range | Packages | Access Time (ns) Iccsb (µA) | | | | | | Std process 65664A | RT process 65664F | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | G 35 50 | Q 35 500 | B 45 50 | S 45 500 | 55 50 | C 55 500 | Mil flows | Mil flows | Space flows ( including SCC9301029) |
| M | 1 | ● | ● | ● | ● | ● | ● | ● | | |
| | 1E | ● | ● | ● | ● | ● | ● | ● | | |
| | 4 | ● | ● | ● | ● | ● | ● | ● | | |
| | D | X | X | X | X | X | X | X | | |
| | 0 | X | X | X | X | X | ● | ● | | |
| S | C | ● | | ● | | ● | | | ● | ● |
| | CE | ● | | ● | | ● | | | ● | ● |
| | 4 | ● | | ● | | ● | | | ● | ● |
| | D | X | | X | | X | | | X | X |
| | 0 | X | | X | X | X | ● | | ● | ● |

● = product in production

X = call sales office for availibility