MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

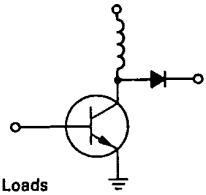
MJ13090 MJH13090
MJ13091 MJH13091

Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

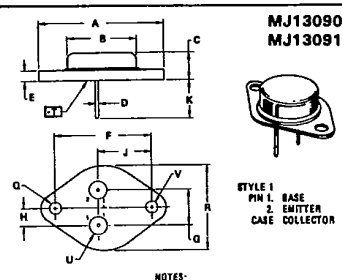


100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads — 150 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

15 AMPERE

NPN SILICON POWER TRANSISTORS

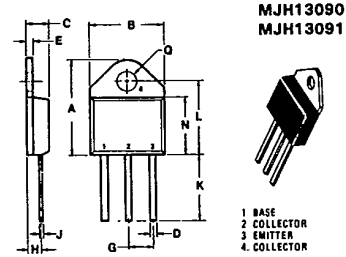
400 AND 450 VOLTS
125 and 175 WATTS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.57	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE D.
   ⌖ ⌀0.13 (0.005) M T V M
   FOR LEADS.
   ⌖ ⌀0.13 (0.005) M T V M Q M
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-05
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.85	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-01
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJ13090	MJ13091	MJH13090	MJH13091	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	450	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	650	750	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous — Peak (1)	I_C / I_{CM}	15 / 20				Adc
Base Current — Continous — Peak (1)	I_B / I_{BM}	5.0 / 10				Adc
Total Device Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 / 100 / 1.0		125 / 50 / 1.0		Watts / W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to 200		-55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds.	T_L	275	°C

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥10%.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0) MJ13090, MJH13090 MJ13091, MJH13091	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	— —	0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figures 12 and 13			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 14			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc	h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 15 Adc, I_B = 3.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	— — —	1.0 3.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	—	0.03	0.05	μs
Rise Time	t_r	—	0.13	0.50	
Storage Time	t_s	—	0.55	2.50	
Fall Time	t_f	—	0.10	0.50	
(V_{CC} = 250 Vdc, I_C = 10 Adc, I_{B1} = 1.25 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)					
Inductive Load, Clamped (Table 1)					
Storage Time	t_{sv}	—	0.80	3.00	μs
Crossover Time	t_c	—	0.175	0.40	
Fall Time	t_{fi}	—	0.15	0.30	
Storage Time	t_{sv}	—	0.50	—	
Crossover Time	t_c	—	0.15	—	
Fall Time	t_{fi}	—	0.10	—	
($I_{C(pk)}$ = 10 A, I_{B1} = 1.25 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V)	(T_J = 100°C)				
	(T_J = 25°C)				

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

*$\beta_f = \frac{I_C}{I_B}$

DC CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

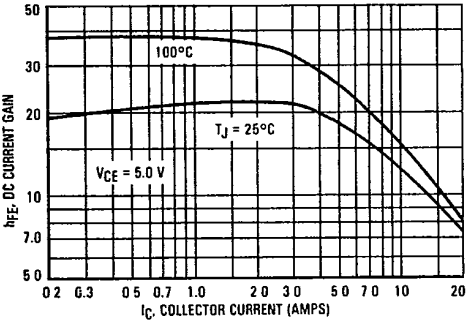


FIGURE 2 — COLLECTOR SATURATION REGION

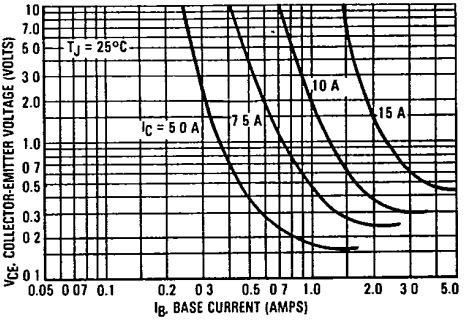


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

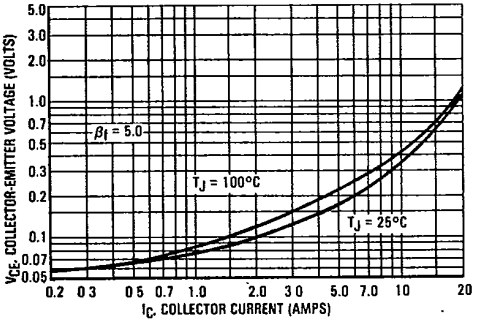


FIGURE 4 — BASE-EMITTER SATURATION VOLTAGE

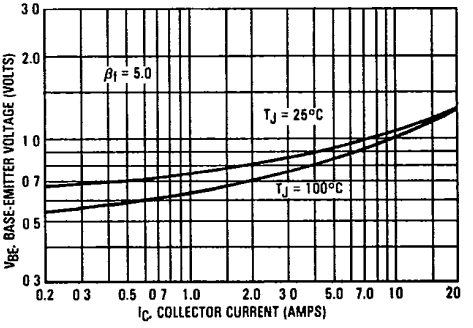


FIGURE 5 — COLLECTOR CUTOFF REGION

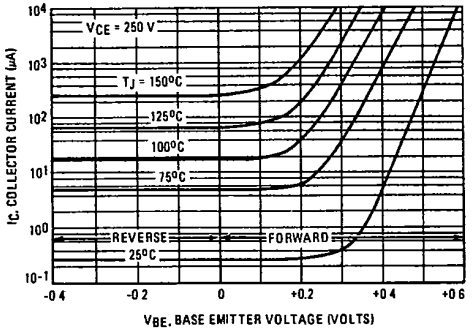


FIGURE 6 — CAPACITANCE

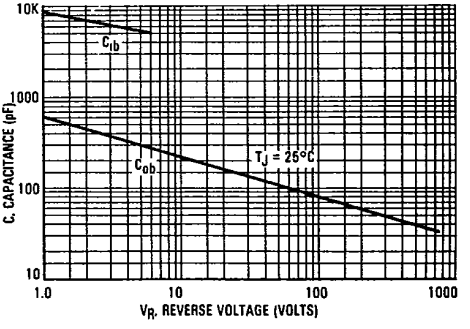


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V > 20 Ω; 0; 1; 2 PW Varied to Attain I_C = 100 mA	HP 214 or Equiv PG; 0; ≈ -35 V; 0.02 μF; 100; +V ≈ 11 V; 20; 2N6191; 10 μF; R_{B1}; A; R_{B2}; 0.02 μF; 10 μF; 2N5337; 50; 500; 100; -V Connect Point A to base of TUT Adjust -V to obtain desired $V_{BE(off)}$ at Point A Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$ R2 = ∞	TURN ON TIME 1; 2; I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_{B1} adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 30 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT; 1; Input; 1N4937 or Equivalent; R_{coil}; L_{coil}; See Above for Detailed Conditions; V_{clamp}; V_{CC}; 2; R_S = 0.1 Ω OUTPUT WAVEFORMS I_C; $I_{C(pk)}$; t_f Clamped; t_1; t_f; t; V_{CE}; V_{CE} or V_{clamp}; Time; t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1; TUT; 2; R_L; V_{CC}

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

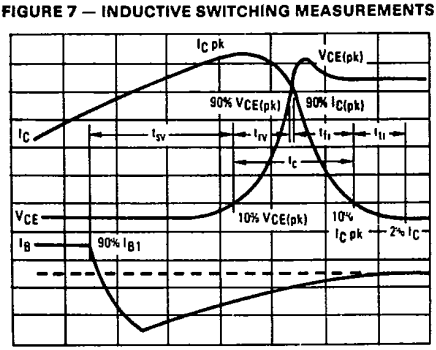
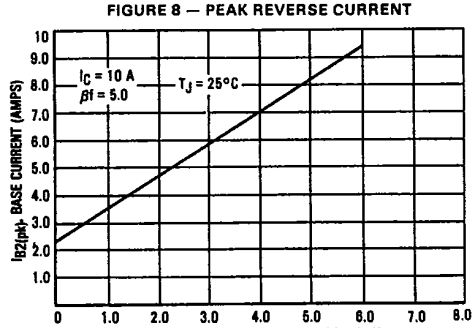


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10 % V_{clamp}
t_{rv} = Voltage Rise Time, 10—90% V_{clamp}
t_{fi} = Current Fall Time, 90—10% I_C
t_{ti} = Current Tail, 10—2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user-oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

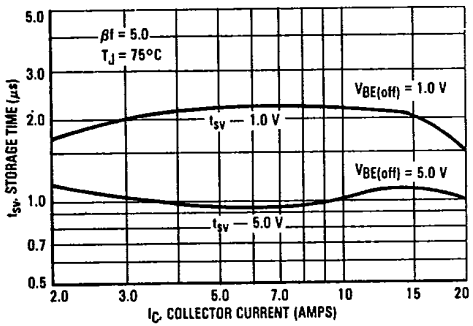


FIGURE 10 — CROSSOVER AND FALL TIMES

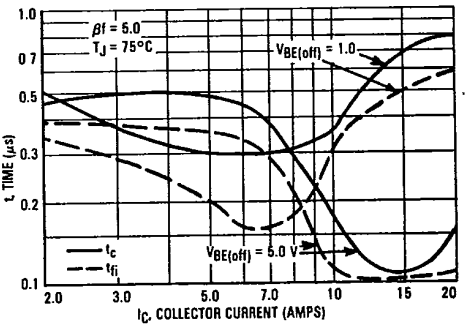
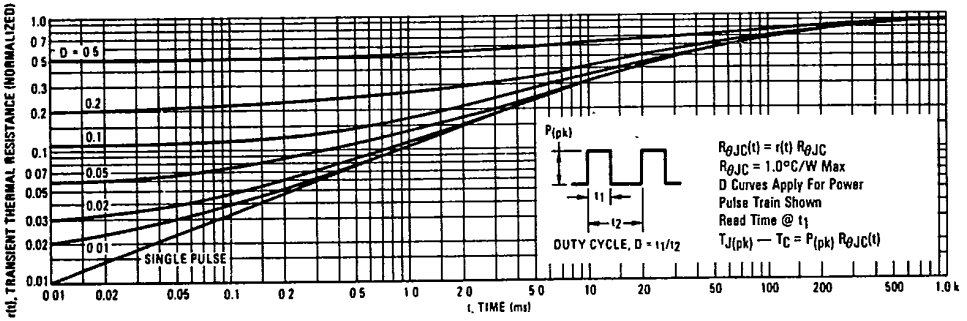


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — FORWARD BIAS SAFE OPERATING AREA
MJ13090 and MJ13091

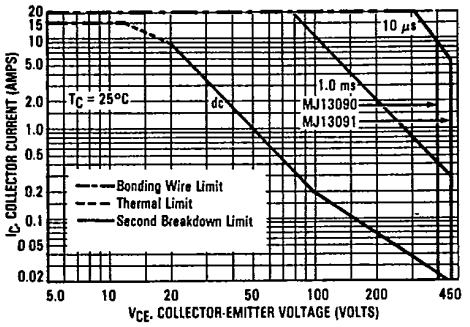
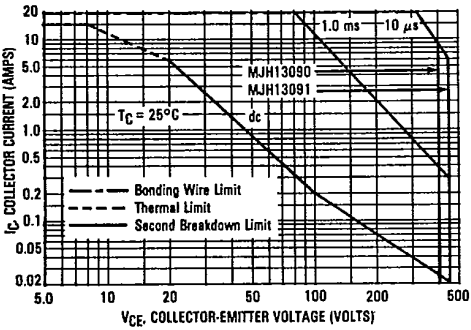


FIGURE 13 — FORWARD BIAS SAFE OPERATING AREA
MJH13090 and MJH13091



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 are based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 12 and 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse-biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives RBSOA characteristics.

FIGURE 14 — REVERSE BIAS SAFE OPERATING AREA

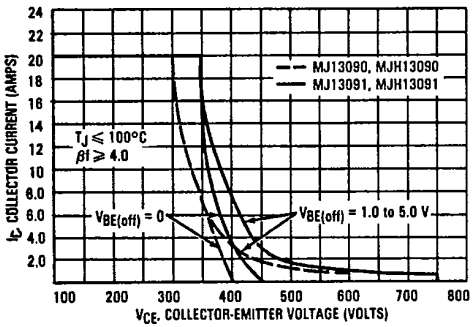


FIGURE 15 — POWER DERATING