SMCT TA20N20A10

Advanced Pulse Power Device

N-MOS VCS, ThinPak™

Preliminary Data Sheet

Description

This voltage controlled Solidtron (VCS) discharge switch utilizes an n-type MOS-Controlled Thyristor mounted on a ThinPak™, ceramic "chip-scale" hybrid.

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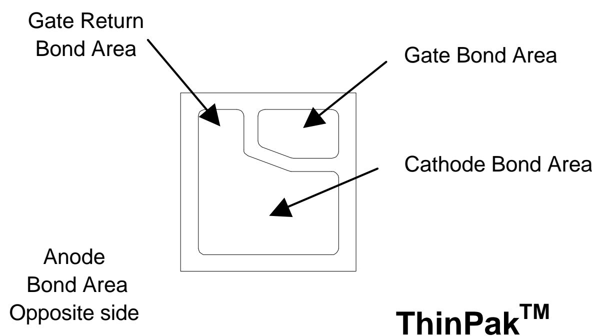
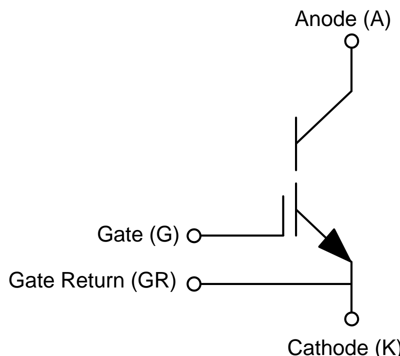
The VCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with extremely high dI/dt capability. This semiconductor is intended for the control of high power circuits with the use of very small amounts of input energy and is ideally suited for capacitor discharge applications.

The ThinPak™ Package is a perforated, metalized ceramic substrate attached to the silicon using 302°C solder. An epoxy underfill is applied to protect the high voltage termination from debris. All exterior metal surfaces are tinned with 63pb/37sn solder providing the user with a circuit ready part. It's small size and low profile make it extremely attractive to high dI/dt applications where stray series inductance must be kept to a minimum.

Package



Schematic Symbol



Features

- 2000V Peak Off-State Voltage
- 20A Continuous Rating
- 4kA Surge Current Capability
- High dI/dt Capability
- Low On-State Voltage
- MOS Gated Control
- Low Inductance Package

Absolute Maximum Ratings

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V_{DRM}	2000	V
Peak Reverse Voltage	V_{RRM}	-5	V
Off-State Rate of Change of Voltage Immunity	dv/dt	1000	V/uSec
Continuous Anode Current at 110°C	I_{A110}	20	A
Repetitive Peak Anode Current (Pulse Width=1uSec)	I_{ASM}	2000	A
Nonrepetitive Peak Anode Current (Pulse Width=250nSec)	I_{ASM}	4000	A
Rate of Change of Current	dI/dt	20	kA/uSec
Continuous Gate-Cathode Voltage	V_{GKS}	+/-20	V
Peak Gate-Cathode Voltage	V_{GKM}	+/-25	V
Minimum Negative Gate-Cathode Voltage Required for Garanteed Off-State	$V_{GK(OFF-MIN)}$	-5	V
Maximum Junction Temperature	T_{JM}	150	°C
Maximum Soldering Temperature (Installation)		260	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

Preliminary Data Sheet - Product Status : First Production : This data sheet contains preliminary data . Supplementary data will be published at a later date. Silicon Power reserves the right to make changes at any time without notice.

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SOLIDTRON™

SMCT TA20N20A10

Advanced Pulse Power Device

N-MOS VCS, ThinPak™

Preliminary Data Sheet

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Performance Characteristics	T_J=25°C unless otherwise specified			Measurements			
Parameters	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	$V_{(BR)}$	V_{GK}=-5, I_A=1mA		2000			V
Anode-Cathode Off-State Current	i_D	V_{GK}=-5V, V_{AK}=2000V	T_C=25°C		<10	100	uA
			T_C=150°C		250	1000	uA
Gate-Cathode Turn-On Threshold Voltage	$V_{GK(TH)}$	V_{AK}=V_{GK}, I_{AK}=1mA			0.7		V
Gate-Cathode Leakage Current	$I_{GK(lkg)}$	V_{GK}=+/-20V				500	nA
Anode-Cathode On-State Voltage	V_T	I_T=25A, V_{GK}=+5V	T_C=25°C		2.4	3.0	V
			T_C=150°C		3	3.5	V
Input Capacitance	C_{ISS}				5		nF
Turn-on Delay Time	$t_{D(ON)}$	0.2uF Capacitor Discharge			230	300	nS
Rate of Change of Current	dI/dt	T_J=25°C, V_{GK}= -5V to +5V			18		kA/uSec
Peak Anode Current	I_P	V_{AK}=1400V, RG=4.7Ω			2200		A
Discharge Event Energy	E_{DIS}	L_S= 15nH			196		mJ
Turn-on Delay Time	$t_{D(ON)}$	0.2uF Capacitor Discharge			180	250	nS
Rate of Change of Current	dI/dt	T_J=25°C, V_{GK}= -5V to +5V			28		kA/uSec
Peak Anode Current	I_P	V_{AK}=1800V, RG=4.7Ω			3300		A
Discharge Event Energy	E_{DIS}	L_S= 15nH			310		mJ
Junction to Case Thermal Resistance	$R_{\theta JC}$	Anode (bottom) side cooled (Note 1.)			0.09		°C/W
Junction to Case Thermal Resistance	$R_{\theta JC}$	Cathode-Gate (top) side cooled (Note 2.)			1.6		°C/W

Notes:

1. Case Exterior Assumed to be 0.002" of 63sn/37pb solder applied directly to Anode.
2. Case Exterior Assummed to be 0.002" of 63sn/37pb solder applied directly to cathode bond area of thinPak.

Typical Performance Curves (unless otherwise specified)

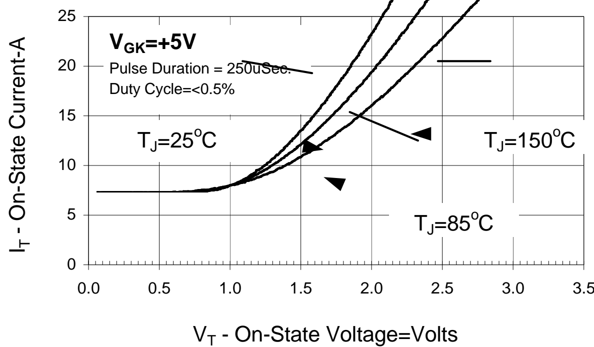

Figure 1. On-State Characteristics

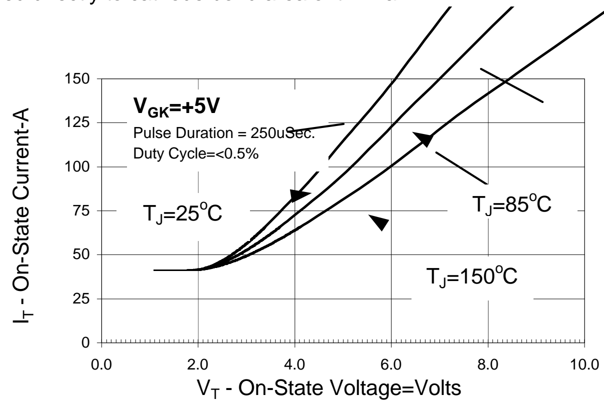

Figure 2. On-State Characteristics

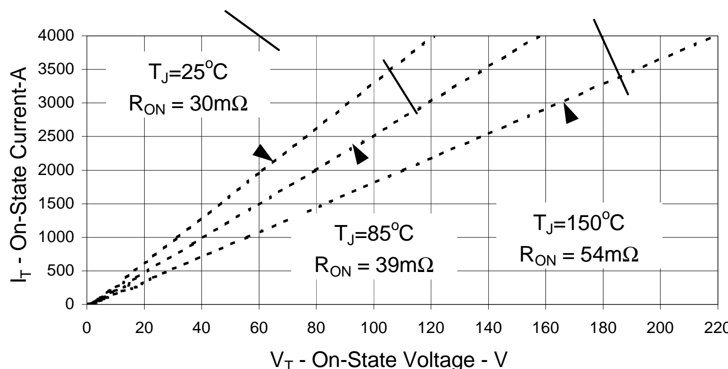

Figure 3. Predicted High Current On-State Characteristics

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Typical Performance Curves (Continued)

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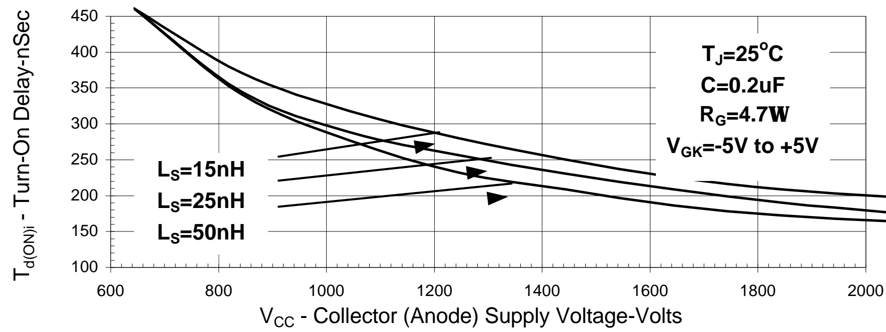

Figure 4. Turn-On Delay Characteristics with L_S = 15nH, 25nH and 50nH

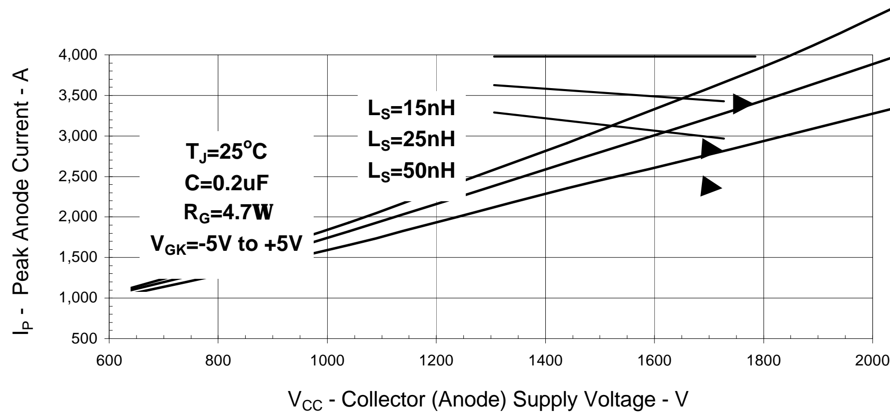

Figure 5. Peak Anode Current Vs. Anode Supply Voltage (See Figure 7.)

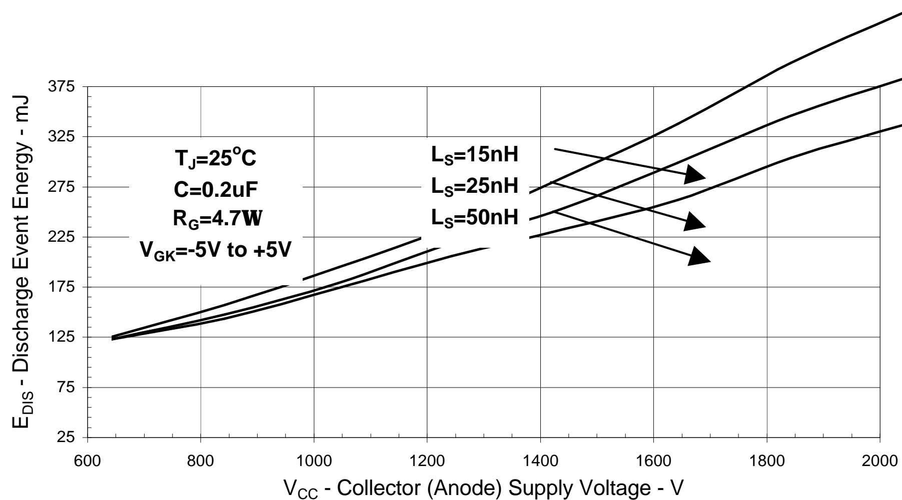

Figure 6. Discharge Energy Vs. Anode Supply Voltage (See Figure 7.)

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Typical Performance Curves (Continued)

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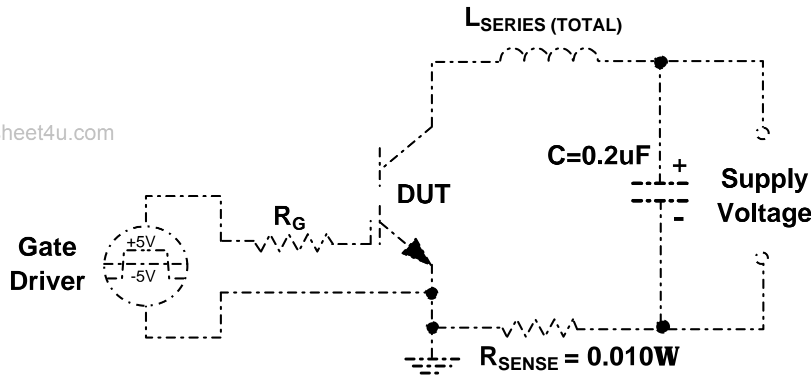
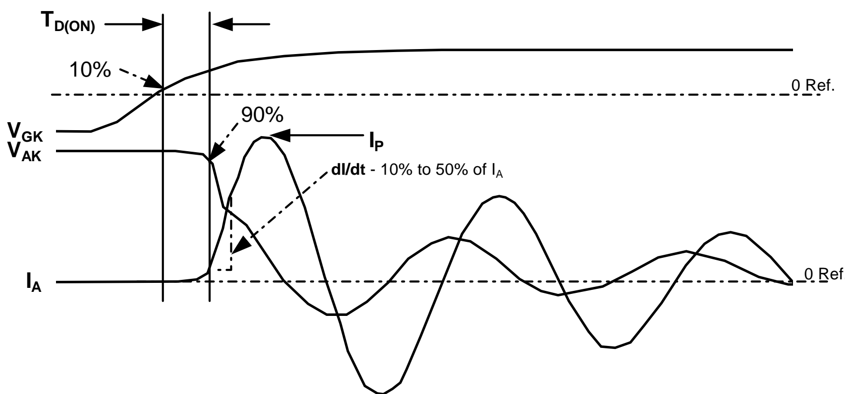


- $L_{SERIES(TOTAL)}$ is caculated using $1 / (f\ 2\pi)^2 C$ where f = frequency of I_A when using SMCT TA32N14A10 for circuit set up and calibration.
- R_{SENSE} is a calibrated Current Viewing Resistor (CVR)



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH) and a SMCTTA32N14A10 MCT. SMCT TA20N20A10 devices do not produce ringing waveforms
- V_{GK} is held positive until I_A oscillations have ended (I_A=0).

Figure 7. 0.2uF Pulsed Discharge Circuit and Waveforms

Application Notes

A1. Use of Gate Return Bond Area.

The VCS was designed for high di/dt applications. An independent cathode connection or "Gate Return Bond Area" was provided to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, (V=L*di/dt). It is therefore, critcal that the user utilize the Gate Return Bond Area as the point at which the gate driver reference (return) is attached to the VCS device.

Packaging and Handling

1. All metal surfaces are tinned using 63pb/37sn solder.
2. Installation reflow temperature should not exceed 260°C or internal package degradation may result.
3. Package may be cooled from either top or bottom.
4. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device

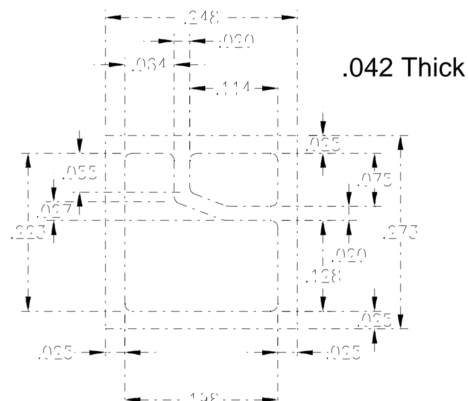


Figure 8. Package Dimensions

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