10.7Gb/s Linear Optical Modulator Driver TGA4819-EPU-SL

OC-192 Metro and Long Haul Applications
Surface Mount Package

Key Features and Performance

- Up to 10 V_{PP} Linear Output Voltage
- 20 dB Gain
- Internal DC Blocks
- Integrated Power Detector
- Single-ended Input / Output
- Small Form Factor
  - 11.4 x 8.9 x 2 mm
  - 0.450 x 0.350 x 0.080 inches

Primary Applications

- Mach-Zehnder Linear Modulator Driver for Metro and Long Haul.

Description

The TriQuint TGA4819-EPU-SL is part of a series of optical driver amplifiers suitable for a variety of driver applications.

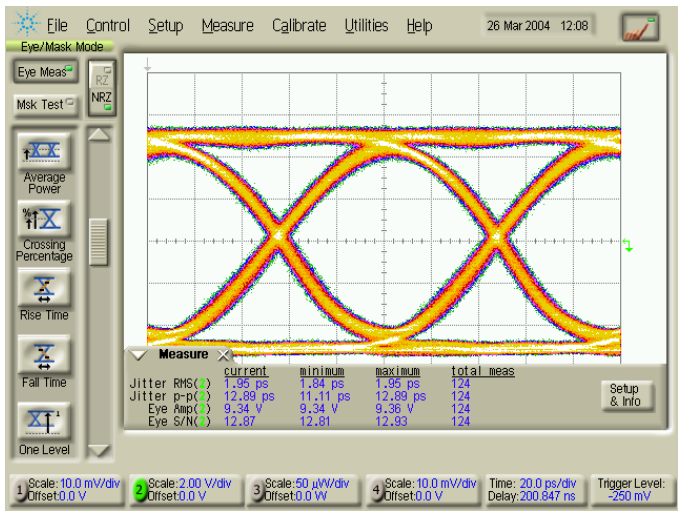
The TGA4819 is a medium power wideband AGC amplifier that typically provides 20dB small signal gain with 20dB AGC range.

The TGA4819 is an excellent choice for applications requiring high drive combined with high linearity. The TGA4819 has demonstrated capability to deliver 10Vpp while maintaining output harmonic levels near -30dBc for a 2GHz fundamental.

The TGA4819 requires a low frequency choke and control circuitry.

Preliminary Measured Performance

Bias Conditions: V_D = 8V, V_{CTRL} = +1V, I_D = 310mA
PRBS 2^{31}-1; 10.7Gbps; Vin = 1Vpp; CPC = 50%



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

TABLE I
MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V_D	Drain Voltage	9 V	1/ 2/
V_G	Gate Voltage Range	-3V to 0V	1/
V_{CTRL}	Control Voltage Range	-3V to V_D/2	1/
I_D	Drain Supply Current (Quiescent)	400 mA	1/ 2/
$\| I_G \|$	Gate Supply Current	5 mA	1/
P_{IN}	Input Continuous Wave Power	23 dBm	1/ 2/
V_{IN}	10.7Gb/s PRBS Input Voltage	4 V_{PP}	1/ 2/
P_D	Power Dissipation	3.1 W	1/ 2/ 3/
T_{CH}	Operating Channel Temperature	150 ^{0}C	4/
T_M	Mounting Temperature (10 Seconds)	230 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D at a package base temperature of 70◦C

3/ When operated at this bias condition with a baseplate temperature of 70◦C, the MTTF is reduced to 1.0E+6 hours

4/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	$R_{\Theta JC}$ (°C/W)	MTTF (hrs)
$R_{\Theta JC}$ Thermal Resistance (Channel to Backside of Package)	V_D = 8.1V I_D = 350mA P_{DISS} = 2.8W T_{BASE} = 70°C	142.8	25.7	1.9E6

Note: Thermal transfer is conducted through the bottom of the TGA4819-EPU-SL package into the motherboard. The motherboard must be designed to assure adequate thermal transfer to the base plate.

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TABLE III
RF CHARACTERIZATION TABLE
(T_A = 25°C, Nominal)
(V_D = 8V, V_{CTRL} = +1V, I_D = 310mA ±5%, V_G ≈ -0.3V)

Parameter	Test Conditions	Typ	Units	Notes
Small Signal Bandwidth		8	GHz	
Small Signal Gain	100 MHz – 4 GHz 6 GHz 10 GHz 14 GHz	20 19 17 12	dB	1/ 2/
Input Return Loss	100 MHz – 14 GHz	15	dB	1/ 2/
Output Return Loss	100 MHz – 14 GHz	13	dB	1/ 2/
Small Signal AGC Range	Midband	20	dB	
Output Power @ P_{1dB}	2 GHz	25.5	dBm	3/

Note: Table III Lists the RF Characteristics of typical devices as determined by fixtured measurements.

1/ Verified at package level RF test
2/ Package RF Test Bias: V_D = 8V, V_{CTRL} = +1V, adjust V_G to achieve I_D=310 mA
3/ Verified at die level on-wafer probe

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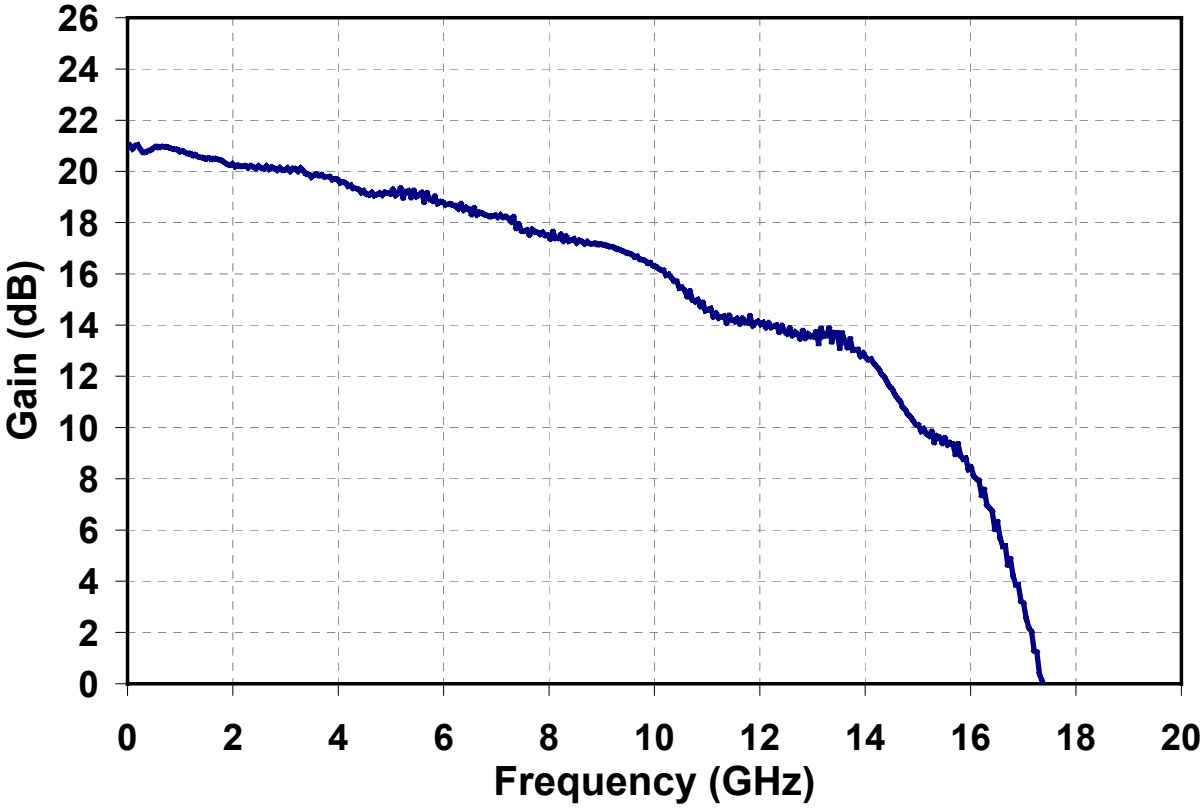
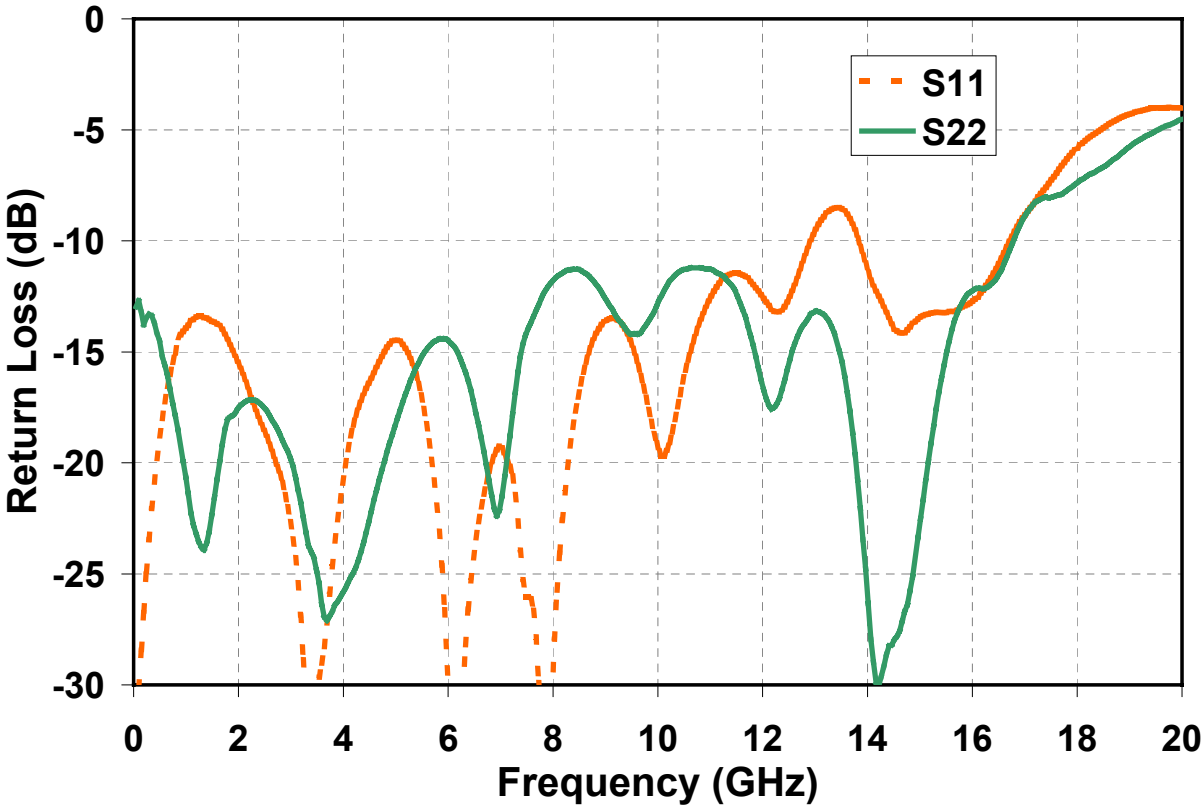
Measured Performance

V_D = 8V; V_{CTRL} = +1V; I_D = 310mA; $V_G \approx$ -0.3V





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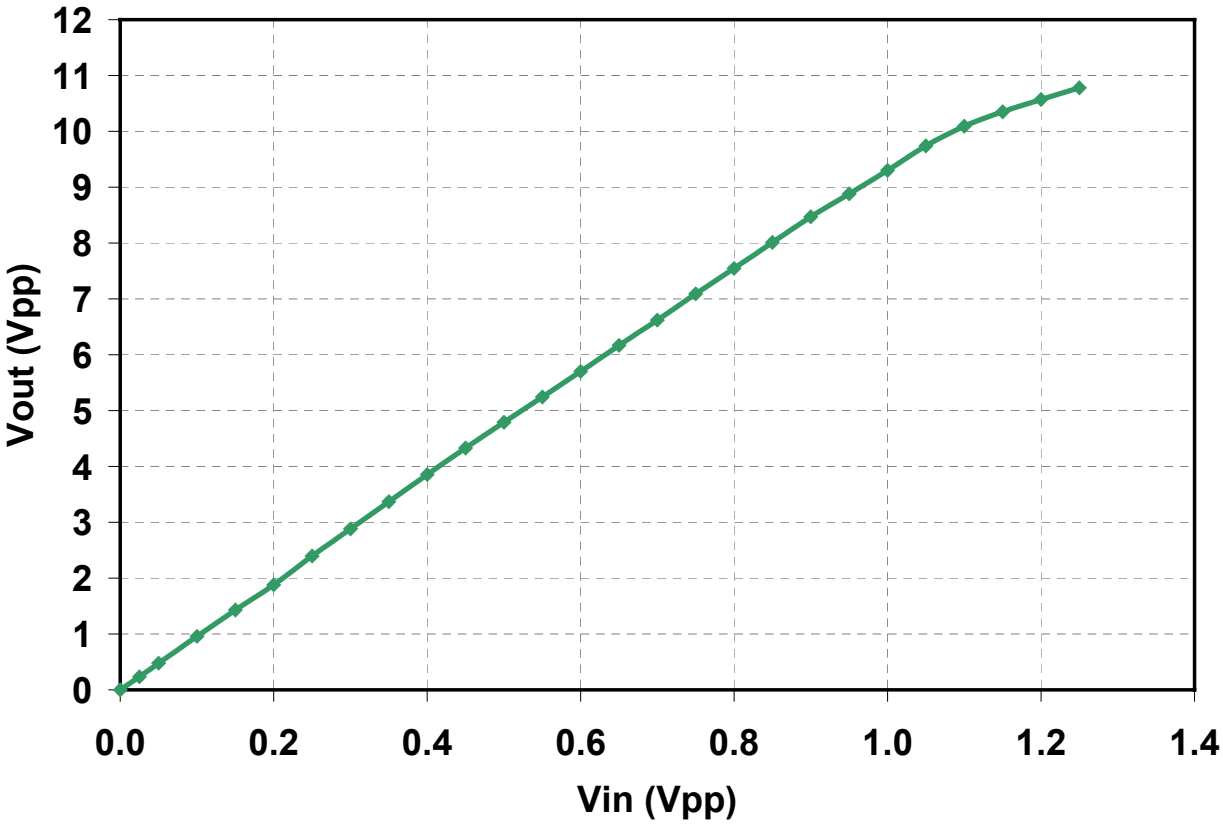

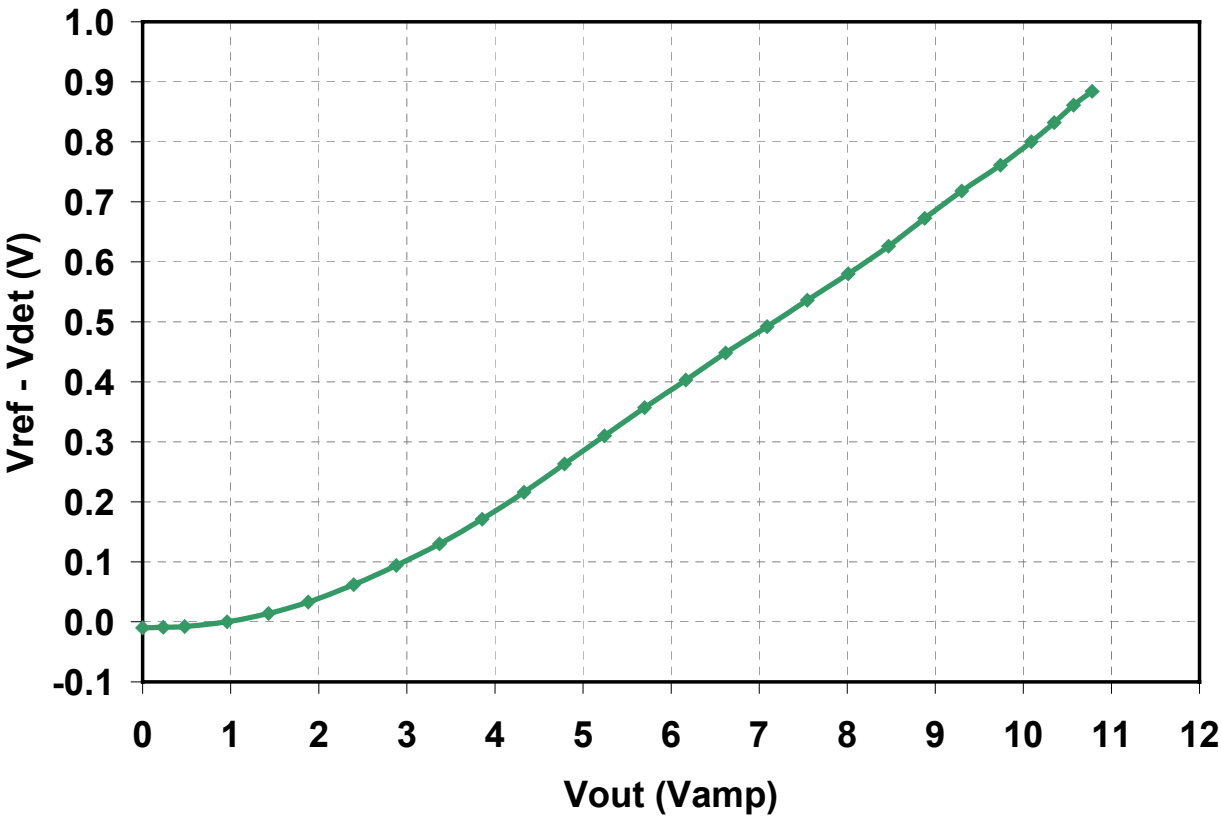

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Measured Performance

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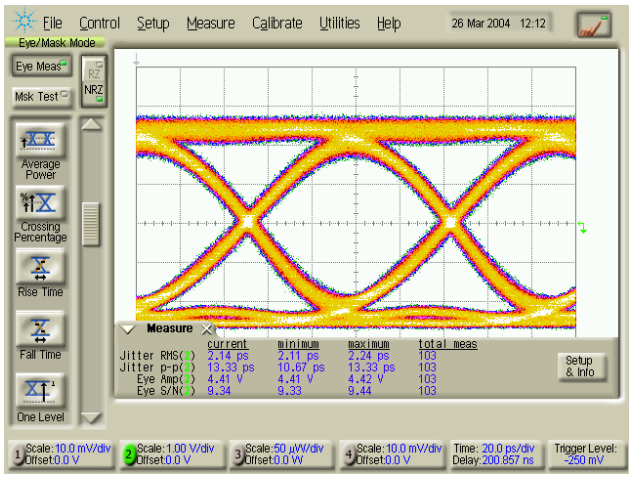
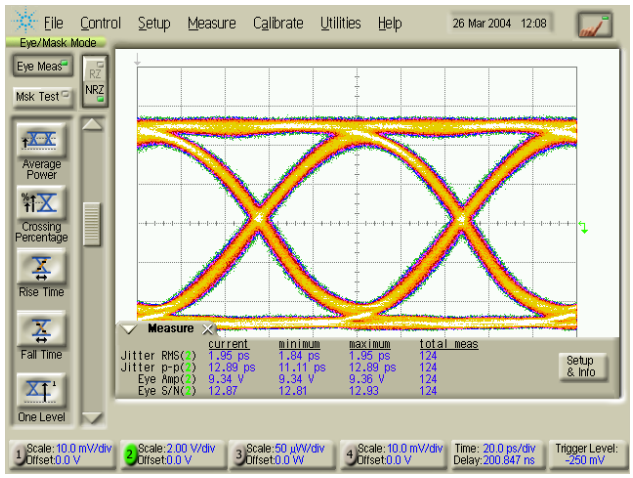
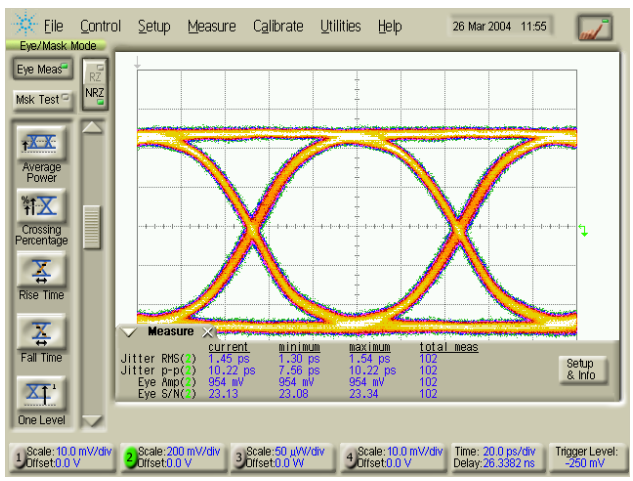
PRBS 2^{31}-1; 10.7Gbps; CPC = 50%



Vin = 500mV$_{PP}$



Vin = 1V$_{PP}$



Input Signal Vin = 1V$_{PP}$
Includes 8GHz Bessel Filter

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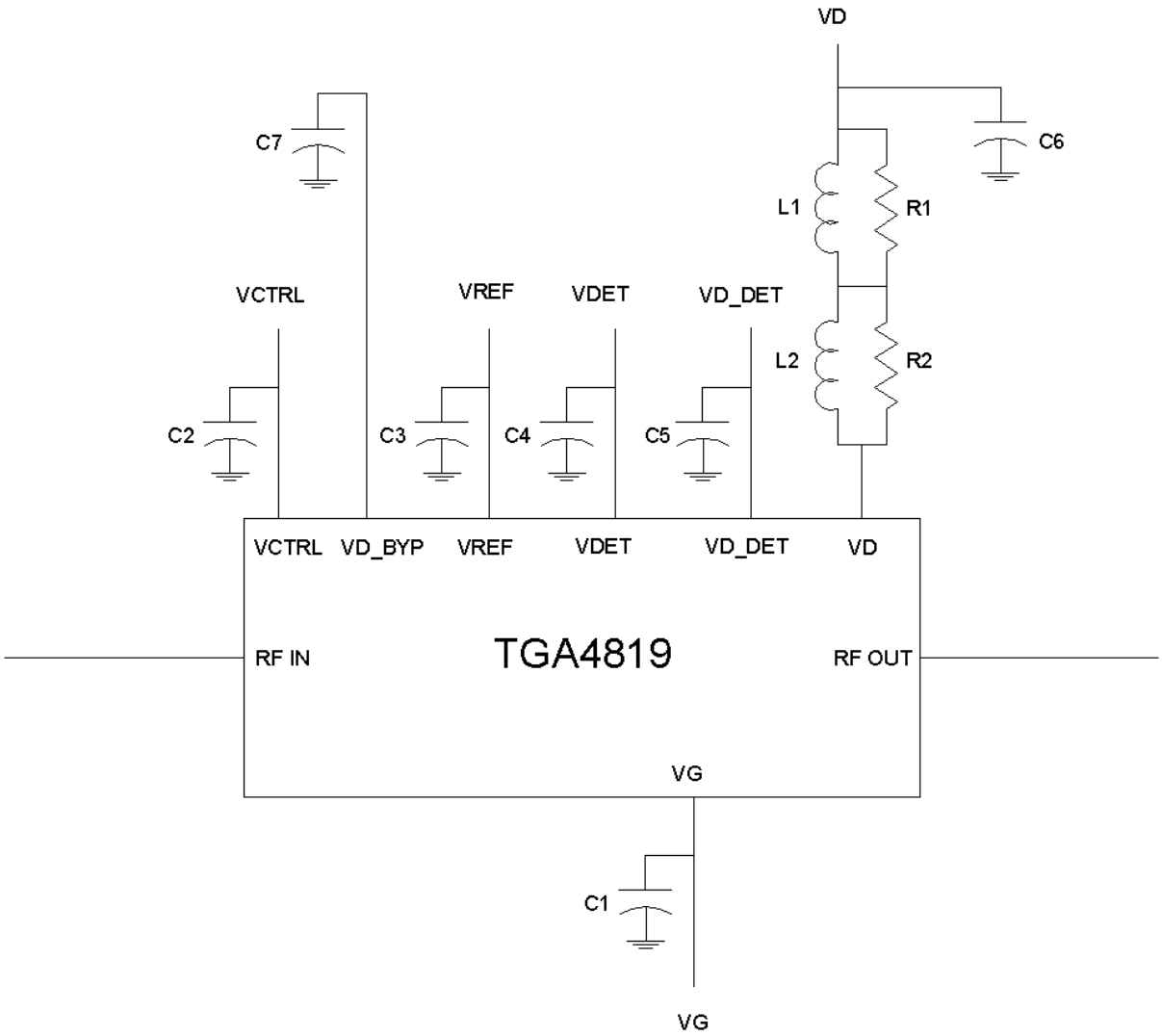
Application Circuit



Note:

1. C1 extend low frequency performance thru 30 KHz. For applications requiring low frequency performance thru 100 KHz, C1 may be omitted

2. C2 is a power supply decoupling capacitors and may be omitted when driven directly with an op-amp.

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Application Circuit
(Continued)

Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C7	10uF Capacitor MLC Ceramic	AVX	0802YC106KAT
C2, C3, C4, C5	0.01 uFCapacitor MLC Ceramic	AVX	0603YC103KAT
C6	10 uF Capacitor Tantalum	AVX	TAJA106K016R
L1	220 uH Inductor	Belfuse	S581-4000-14
L2	330 nH Inductor	Panasonic Coilcraft	ELJ-FAR33MF2 0603LS-331XJB
R1, R2	274 Ω Resistor	Panasonic	ERJ-2RKF2740X

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Laboratory - Bias ON/OFF Procedure
Vd=8V, CPC=50%

Bias ON

1. Disable the output of the PPG
2. Set V_D = 0V, V_{CTRL} = 0V & V_G = 0V
3. Set V_G = -1.5V
4. Increase V_D to 8V observing Id
   - Assure I_D = 0mA
5. Set V_{CTRL} = +1V
   - I_D should still be 0mA
6. Make V_G more positive until I_D = 310mA.

   V_G will be approximately -0.3V.
7. Enable the output of the PPG.
8. Output Swing Adjust: Adjust V_{CTRL} slightly positive to increase output swing or adjust V_{CTRL} slightly negative to decrease the output swing.
9. Crossover Adjust: Adjust V_G slightly positive to push the crossover down or adjust V_G slightly negative to push the crossover up.

Bias OFF

1. Disable the output of the PPG
2. Set V_{CTRL} = 0V
3. Set V_D = 0V
4. Set V_G = 0V

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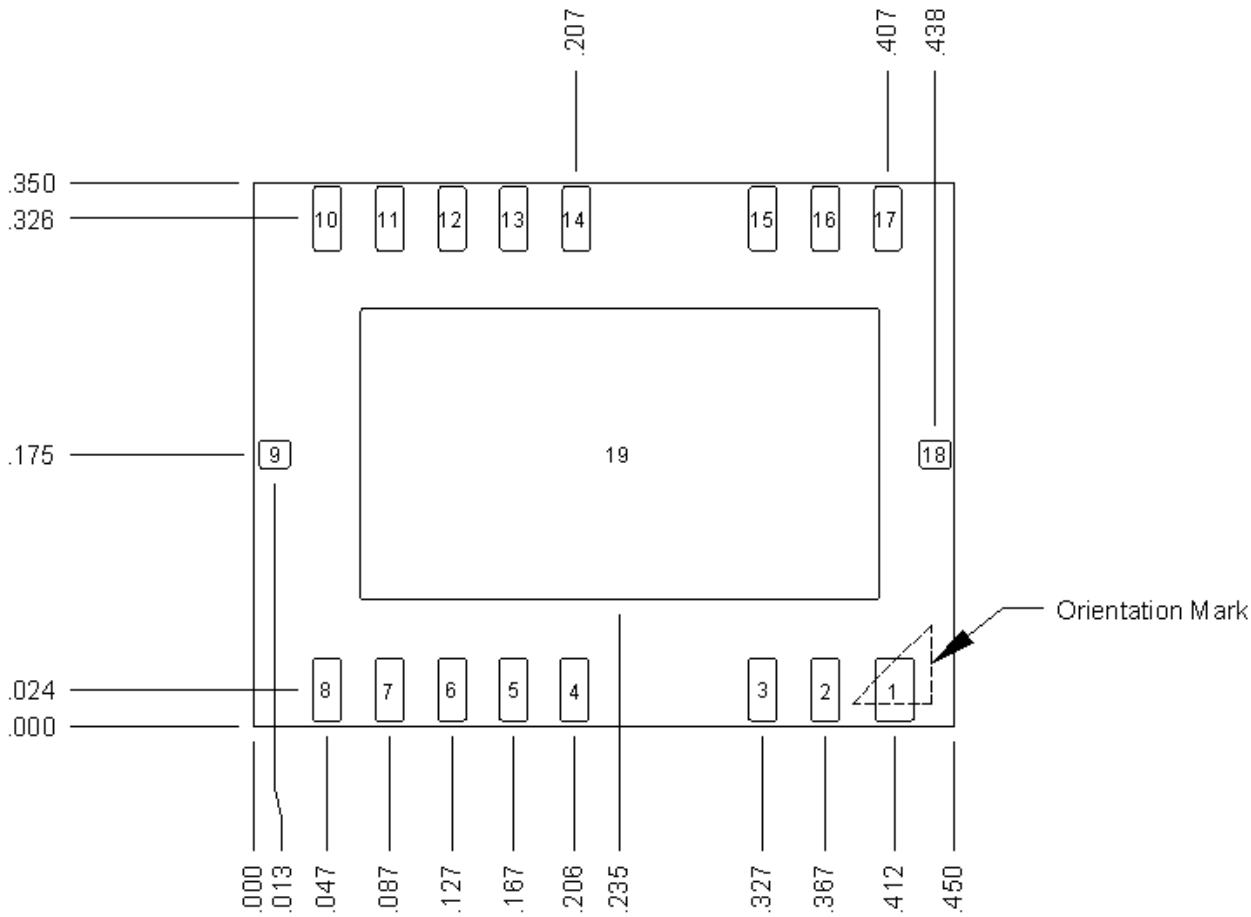
Mechanical Drawing



Bond Pad #1	N/C	0.025" x 0.041"	Bond Pad #11	N/C	0.018" x 0.041"
Bond Pad #2	N/C	0.018" x 0.041"	Bond Pad #12	VD	0.018" x 0.041"
Bond Pad #3	N/C	0.018" x 0.041"	Bond Pad #13	VD_DET	0.018" x 0.041"
Bond Pad #4	N/C	0.018" x 0.041"	Bond Pad #14	VDET	0.018" x 0.041"
Bond Pad #5	N/C	0.018" x 0.041"	Bond Pad #15	VREF	0.018" x 0.041"
Bond Pad #6	VG	0.018" x 0.041"	Bond Pad #16	VD_BYP	0.018" x 0.041"
Bond Pad #7	N/C	0.018" x 0.041"	Bond Pad #17	VCTRL	0.018" x 0.041"
Bond Pad #8	N/C	0.018" x 0.041"	Bond Pad #18	RF In	0.020" x 0.018"
Bond Pad #9	RF Out	0.020" x 0.018"	Bond Pad #19	GND	0.334" x 0.187"
Bond Pad #10	N/C	0.018" x 0.041"			

NOTE: Maximize number of vias on attachment area of PCB for Bond Pad #19. This is required electrical and thermal conduction

Dimensions: Inches

Tolerances: Length & Width: ±0.003"
Height: ±0.006"
Adjacent Pad to Pad Spacing: ±0.0002"
Pad Size: ±0.001"

Package Backside Material: Material: RO4003 (0.008" thk) w/ 0.5oz Cu (0.0007" thk)
Plating: 100 - 350µin Ni underplate w/ 5 - 10µin Au overplate

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Assembly of a TGA4819-EPU-SL Package onto a Motherboard

Manual Assembly for Prototypes

1. Clean the motherboard with Acetone and rinse with alcohol and DI water. Allow the motherboard to fully dry.

2. Using a standard SN63 solder paste, such as Kester SN63 R-560, dispense solder paste dots of 5 to 15 mil in diameter to the motherboard. Assure that there is a minimum of 5 mils and a maximum of 10 mils between the edge of each solder paste area and the closest edge of the ground pad.

3. Manually place a TGA4819-EPU-SL on the motherboard with correct orientation and good alignment. The alignment can be determined manually by centering the package on the motherboard. The RF traces (pin 1 and pin 10) are located along the center horizontal axis of the package.

4. Reflow the assembly on a hot plate with the surface temperature of the plate near 230 ^{o}C for 5 to 6 seconds.

5. Let the assembly completely cool down. *This package has little or no tendency to self- align during the reflow.*

6. Clean the assembly with acetone and rinse with alcohol and DI water.

High Volume Assembly of the Package

The TGA4819-EPU-SL is a standard surface mount component compatible with standard high volume assembly processes using standard SN63 solder paste, such as Kester R560. Refer to Kester R560 manufacture data sheet for recommended reflow profile, cleaning, and handling. Dispense solder paste using standard solder printing techniques such as stencil solder printing. Pick-and-place using a standard machine such as MRSI machine. Perform solder reflow using a Sikama Reflow System. Recommended solder stencil and motherboard interface layout are available upon request.

CAUTION: The TGA4819-EPU contains GaAs MMIC devices that are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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