

UNISONIC TECHNOLOGIES CO., LTD

L1913

Preliminary

CMOS IC

150mA LOW-DROPOUT LINEAR REGULATORS

DESCRIPTION

The UTC **L1913** is a low supply current, low dropout linear regulator. It is operating at 2.5V - 5.5V. The supply current is as low as 55μ A in the no–load condition. In the shutdown mode, the maximum supply current is less than 1μ A.

A built-in over-temperature protection circuit is designed to protect the device from being damaged by thermal overload. The over-current protection limit is set at 250mA (TYP.) and 150mA (MIN.).

The UTC **L1913** can be operated on the following two modes. When the SET pin is connected to ground, the output of **L1913** is a pre-set value and the external components are not needed to decide the output voltage. When an output other than the preset value is needed, two external resistors should be used as voltage dividers and then the output voltage is decided by the resistor ratio.

The UTC **L1913** is generally used in notebook computers, cellular phones, PDAs, digital still camera and video recorders and other hand-held devices.

4 5 1 2 3 5 0 7-25

FEATURES

- * Low No-Load Supply Current: 55µA
- * Guaranteed 150mA Output Current
- * Dropout Voltage is 70mV @ 50mA Load
- * OTP (Over-Temperature Protection) and Short-Circuit Protection
- * Two Modes Of Operation: Fixed Mode: 3.3V, 1.5V.
- Adjustable Mode: 1.25V 5.5V
- * Maximum Supply Current In Shutdown Mode is Less than $1\mu A$
- * Low Output Noise at 220µ VRMS
- * Stability with Lost Cost Ceramic Capacitors

ORDERING INFORMATION

Ordering Number	Package	Packing
L1913G-xx-AF5-R	SOT-25	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

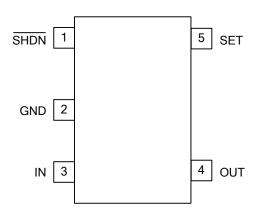
L1913 <u>G-xx-AF5-R</u>	(1) R: Tape Reel
(2)Package Type	(2) AF5: SOT-25
(3)Output Voltage Code	(3) xx: Refer to Marking Information
(4)Halogen Free	(4) G: Halogen Free

L1913

MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-25	15:1.5V 33:3.3V	$\begin{array}{c c} \hline 3 & 2 & 1 \\ \hline AQ \square G \\ \hline \hline 4 & 5 \\ \hline \end{array} \qquad \qquad$

■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	SHDN	Active-Low Shutdown Input. A logic low reduces the supply current to less than 1µA. Connect to IN for normal operation.
2	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
3	IN	Regulator Input. Supply voltage can range from +2.5V to +5.5V. Bypass with 1µF to GND
4	OUT	Regulator Output. Fixed or adjustable from 1.25V to +5.5V. Sources up to 150mA. Bypass with a 1µF, $<$ 0.2 Ω typical ESR capacitor to GND.
5	SET	Feedback Input for Setting the Output Voltage. Connect to GND to set the output voltage to the preset voltage. Connect to an external resistor divider for adjustable-output operation.



BLOCK DIAGRAM

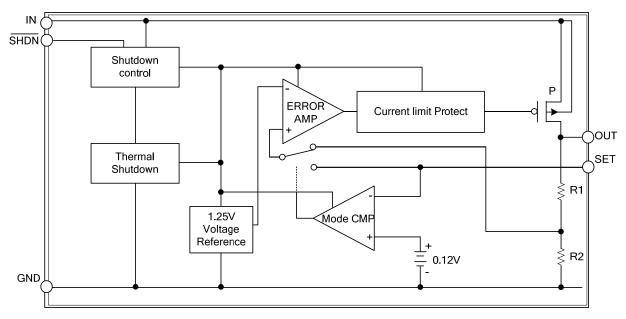


Figure 1. Functional Diagram



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Output Short-Circuit Duration		Infinite	
V _{IN} to GND		-0.3~7	V
SET to GND		-0.3~7	V
SHDN to GND		-0.3~7	V
SHDN to IN		-7~0.3	V
OUT to GND		-0.3~(V _{IN} +0.3)	V
Continuous Power Dissipation (T _A =25°C)	PD	520	mW
Junction Temperature	T_J	150	°C
Operating Temperature	T _{OPR}	-40~85	°C
Storage Temperature	T _{STG}	-65~160	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	240	°C/W

ELECTRICAL CHARACTERISTICS

(V_{IN} =+3.6V, $V_{SHDN} = V_{IN}$, $T_A = T_J = +25^{\circ}C$, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage (Note 2)	V _{IN}			2.5		5.5	V
Output Voltage Accuracy	V _{OUT}	Variation from specified V _{OUT} , I _{OUT} =1mA		-2		2	%
Adjustable Output Voltage Range (Note 3)	V _{OUT}			V_{SET}		5.5	V
Maximum Output Current				150			mA
Current Limit (Note 4)	I _{LIMIT}				250		mA
Ground Pin Current	lq	SET=GND	I _{LOAD} =0mA		55	120	μA
			I _{LOAD} =50mA		145		
		I _{OUT} =1mA			2		-
Dropout Voltage (Note 5)	VDROP	I _{OUT} =50mA			70		mV
		I _{OUT} =150mA			230	300	
	ΔV_{LNR}	SET=GND, $V_{IN}=V_{(STD)}+0.1V \sim 5.5V$, $I_{OUT}=1mA$			0.1	0.28	
Line Regulation		SET tide to OUT, V_{IN} =2.5V ~ 5.5V , I_{OUT} =1mA			0.08	0.4	
Load Regulation	ΔV_{LDR}	I _{OUT} = 0mA ~150mA	SET tide to OUT SET=GND		0.02	0.8 1.0	%/mA
Output Voltage Noise (10Hz~100kHZ)	en	V _{IN} =1.2V, I _{OUT} =150mA	C _{OUT} =1µF		220		μV _{RMS}
SHUTDOWN							
	V _{IH}	Regulator enabled Regulator shutdown		V _{IN} -0.7			
SHDN Input Threshold	VIL					0.4	V
SHDN Input Bias Current	ISHDN	$V_{\overline{SHDN}} = V_{IN}$	T _A = +25°C		0.003	0.1	μA
Shutdown Supply Current	I _{QSHDN}	V _{OUT} = 0V	T _A = +25°C		0.2	1	μA
SET INPUT		-	•				
	V_{SET}	V _{IN} = 2.5V ~ 5.5V,	T _A = +25°C	1.225	1.25	1.275	v
SET Reference Voltage (Note 3)		I _{OUT} = 1mA	$T_A = T_{MIN}$ to T_{MAX}		1.25		
SET Input Leakage Current (Note 3)	I _{SET}	V _{SET} = 1.3V	T _A = +25°C		5	30	nA



■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL PROTECTION						
Thermal Shutdown Temperature	T _{SHDN}			150		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}			15		°C

Notes: 1.Limits is 100% production tested at T_A = +25°C. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

2. Guaranteed by line regulation test.

3. Adjustable mode only.

4.Not tested. For design purposes, the current limit should be considered 150mA minimum to 420mA maximum.

5. The dropout voltage is defined as (V_{IN}-V_{OUT}) when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} +2V.



APPLICATION INFORMATION

The UTC **L1913** contains an error amplifier, 1.25V bandgap reference, PMOS output transistor, internal feedback voltage divider, mode comparator, shutdown logic, over current protection circuit, and over temperature protection circuit as shown in the block diagram.

The process of operation is like this: the mode comparator compares the voltage of SET pin with a pre-set voltage reference of 0.12 V. If the voltage of SET pin is smaller than 0.12 V, the internal feedback voltage divider's central tap is connected to the error amplifier's non-inverting input. Then, the error amplifier compares non-inverting input with the 1.25V bandgap voltage reference. If the feedback voltage is larger than the voltage reference 1.25V, the error amplifier's output becomes higher. This makes the PMOS output transistor's V_{GS} (gate-to-source voltage) smaller, in that condition, the current carrying capability of the PMOS output transistor is reduced, as a result the output voltage decreases until the feedback voltage becomes equal to 1.25V. Similarly, when the feedback voltage is less than 1.25V, the error amplifier causes the output PMOS to conductor more current to pull the feedback voltage up to 1.25V. Thus, through this feedback action, the error amplifier, output PMOS, and the voltage dividers effectively form a unity-gain amplifier with the feedback voltage force to be the same as the 1.25V bandgap reference.

The output voltage, V_{OUT} , can be calculated as follows:

$$V_{OUT}$$
 = 1.25 (1 + R1/R2). (1
Alternatively, the relationship between R1 and R2 is expressed in the following:

$$R1 = R2 (V_{OUT} / 1.25 - 1)$$

In order to reduce power dissipation and loop stability, it is recommended that R2 is 100K Ω . For UTC L1913 (pre-set V_{OUT} is 3.30V), R1 is 164K.

)

(2)

In Figure 2, the SET pin voltage will be larger than 120mV when external voltage divider functions in the operation. The non-inverting input of the amplifier will be connected to the external voltage divider. The conditions of equations 1 and 2 are still true since the operation of the feedback loop is the same. Equation 1 still presents the output voltage.

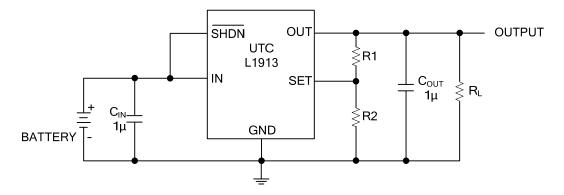


Figure 2. Adjustable Output Using External Feedback Resistors



APPLICATION INFORMATION (Cont.)

Over Current Protection

To monitor the output current, the UTC **L1913** applies a current mirror. A portion of the PMOS output transistor's current is mirrored to a resistor such that the voltage across this resistor is proportional to the output current. Once the output current exceeds limit threshold, UTC **L1913** would be protected with a limited output current. Further more, when the output is short to ground, the output current would be folded-back to a less limit.

Note: the input bypass capacitor of 1µF must be placed in the circuit in order to filter out the input voltage spike caused by the surge current due to the inductive effect of the package pin and the printed circuit board's routing wire. Otherwise, the actual voltage at the IN pin may exceed the absolute maximum rating.

Over Temperature Protection

Over-temperature protection circuit is designed to prevent this device from being damaged due to abnormal temperature during operation. It is used to turn off the output MOSFET if the temperature is higher than 150°C, the switch does not turn on until the temperature drops to 135°C.

Shutdown Mode

The UTC **L1913** enters shutdown mode if the SHDN pin is applied to a logic low voltage. Under the shutdown state, all the analog circuits are turned off completely, which reduces the current consumption to only the leakage current. The UTC **L1913** output pass transistor would get into high impedance level. There is an internal discharge path to help to shorten discharge delay time..

Operating Region and Power Dissipation

The UTC **L1913** is a linear regulator, so the power dissipation can be expressed by: $P = I_{OUT} (V_{IN} - V_{OUT})$. And the maximum power dissipation is calculated by:

$P_{D(MAX)} = (T_J - T_A)/\theta_{JA} = (150^{\circ}C - 25^{\circ}C)/240^{\circ}C/W = 520 \text{mW}$

(Where (T_J-T_A) is the temperature difference the die and the ambient air; θ_{JA} , is the thermal resistance of the chosen package to the ambient air.)

For surface mount device, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. The die attachment area of the UTC **L1913**'s lead frame is connected to pin 2, which is the GND pin. Therefore, the GND pin of UTC **L1913** can carry away the heat of the UTC **L1913** die very effectively. Connecting the GND pin to ground using a large ground plane near the GND pin can improve the power consumption.



APPLICATIONS INFORMATION

Capacitor Selection and Regulator Stability

A 1 μ F capacitor on the input and a 1 μ F capacitor on the output are recommended for most applications of the U TC **L1913**. To get a better supply-noise rejection and transient response, input capacitors with larger values and lower ESR are needed. A higher-value input capacitor (10 μ F) may be necessary if large, fast transients are anticipated and the device is located several inches from the power source.

Power-Supply Rejection and Operation from Sources Other than Batteries

The UTC **L1913** is particularly designed to deliver low dropout voltages and low quiescent currents in batterypowered systems. Power-supply rejection is 42dB at low frequencies. As the frequency increases above 20kHz, the output capacitor is the major contributor to the rejection of power-supply noise.

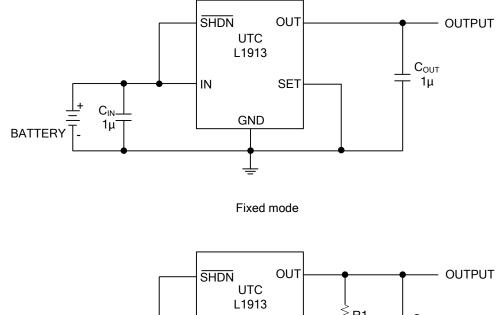
When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output capacitors, and using passive filtering techniques.

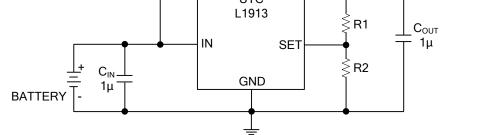
Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the UTC **L1913** use a P-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current.



TYPICAL APPLICATION CIRCUIT





Adjustable Mode

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