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SSI 32D539
Data Synchronizer & 1, 7 RLL ENDEC

Preliminary Data

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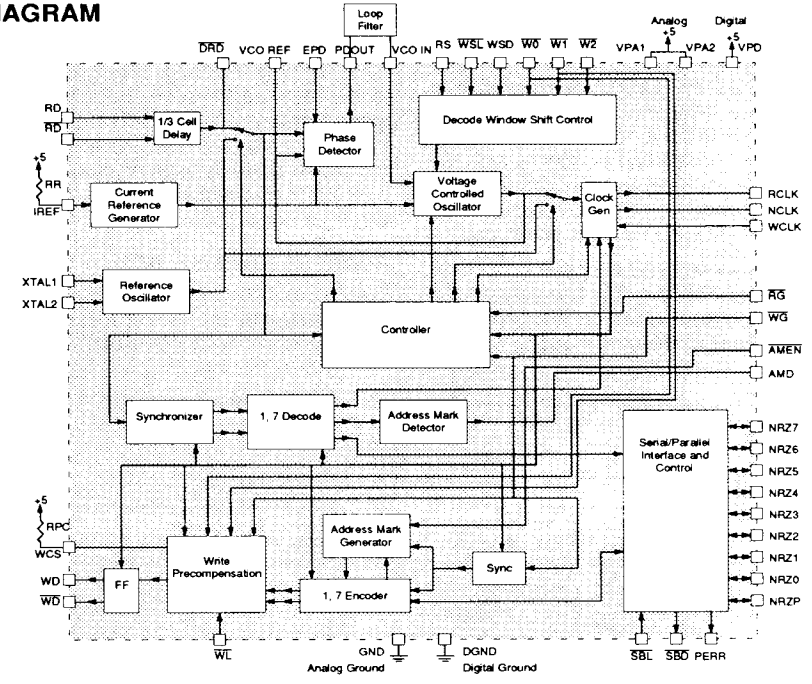
DESCRIPTION

The circuit is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **9-bit bi-directional data bus interface**
  - **8 data bits plus 1 parity bit**
  - **Parity generation during read operation**
  - **Parity checking during write operation**
- **Up to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Programmable Sync-Byte pattern detection**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

BLOCK DIAGRAM



OPERATION

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{185}{DR} - 1.7k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4660 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (read mode) selects the $\overline{RD}$ input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets

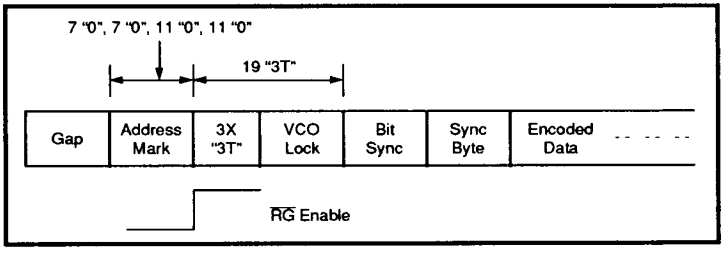


FIGURE 1: Disk Operation Lock Sequence in Read Mode Soft Sector Operation

of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMEN}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 $\overline{RD}$ bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts negative transitions of the incoming read data ($\overline{RD}$) looking for 3 consecutive 3T preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

BYTE SYNC AND NRZ OUT

As the data is decoded, it is compared to a Sync Byte that was loaded prior to the read operation. When a match is found, RCLK and NCLK are resynchronized to the correct byte boundary. NRZ data then appears at the byte output beginning with the sync byte. The $\overline{SBD}$ output is also set low at this time. It remains low until the end of the read operation. A parity bit (NRZP) is also generated for each output byte (even parity).

HARD SECTOR OPERATION

In hard sector operation AMD remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern. In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

NRZ data is clocked into the circuit, serialized and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

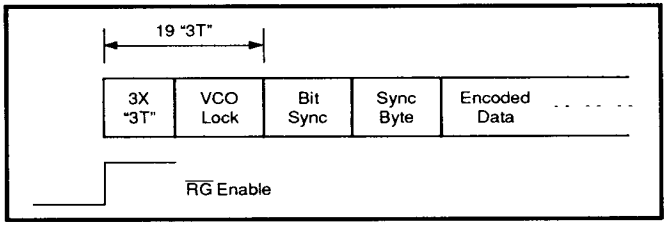


FIGURE 2: Disk Operation Lock Sequence in Read Mode Hard Sector Operation

WRITE MODE (Continued)

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from $\overline{RD}$ and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMEN}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ byte. The first non-zero NRZ byte input is assumed to be the sync byte. After a delay of 5 NRZ time periods, non-preamble data begins to toggle out WD. Finally, at the end of the write cycle, 2 bytes of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 2 NRZ time periods after $\overline{WG}$ goes high.

As each NRZ byte is input for encoding, its parity is checked against the parity bit (NRZP). If a parity error is detected the PERR output flag is set high. It remains high until WG goes high.

HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMEN}$ (address mark enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1, VPA2	I	5 volt analog power supply pins
VPD	I	5 volt digital power supply pin
AGND	O	Analog ground pin
DGND	O	Digital ground pin
$\overline{AMEN}$	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels.
EPD	I	ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to XTAL.) Pin EPD has an internal pull-up resistor. TTL input levels.
RD, $\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels.
$\overline{RG}$	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels.
$\overline{SBL}$	I	SYNC BYTE LATCH CONTROL: Used to latch the Sync Byte reference value into the internal Sync Byte comparator. During idle mode, the Sync Byte latch is transparent while $\overline{SBL}$ is high. An active low level latches the input Sync Byte. The Sync Byte latch is kept in a hold state during non-idle modes, independent of the state of the $\overline{SBL}$ control. Pin $\overline{SBL}$ has an internal pull-up resistor. TTL input levels.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
$\overline{W0}$, $\overline{W1}$, $\overline{W2}$	I	WRITE/WINDOW CONTROL BITS: In Write Mode, pins $\overline{W0}$ and $\overline{W1}$ control the magnitude of the write precompensation (see Table 4). In Read Mode, pins $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
$\overline{WL}$	I	WRITE PRECOMPENSATION LATCH CONTROL: Used to latch the write precompensation control bits $\overline{W0}$ and $\overline{W1}$ into the internal DAC. The latch is transparent while $\overline{WL}$ is high. An active low level latches the input control bits. Pin $\overline{WL}$ has an internal pull-up resistor. TTL input levels.
WCLK	I	WRITE CLOCK: Write mode byte clock. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels.
$\overline{WG}$	I	WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
$\overline{WSL}$	I	WINDOW SYMMETRY LATCH CONTROL: Used to latch the window symmetry control bits $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ and WSD into the internal DAC. The latch is transparent while $\overline{WSL}$ is high. An active low level latches the input control bits. Pin $\overline{WSL}$ has an internal pull-up resistor. TTL input levels.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is low or $\overline{AMEN}$ is high. When $\overline{AMEN}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMEN}$ resets pin $\overline{AMD}$. TTL output levels.
$\overline{DRD}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
NCLK	O	NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the RCLK frequency. TTL output levels.
PERR	O	PARITY ERROR FLAG: Active during write mode and during Sync Byte loading. When $\overline{WG}$ is low, the contents of the NRZ write data input register is examined and compared with the NRZP write data parity bit. Even parity is assumed. For example, PERR becomes active when NRZ7-0 and NRZP are all high. Parity checking is performed after each WCLK load operation. If the input data contains a parity error, or if the WCLK timing causes the input register to contain a parity error, an internal write parity error flag is set. If a parity error occurs during a write operation, the Write Data encoding will continue to function normally. This error flag is reset low when $\overline{WG}$ goes high. Independent of $\overline{WG}$, a separate circuit monitors the Sync Byte. Each time $\overline{SBL}$ transitions from high to low, the contents of the Sync Byte latch is compared with the NRZP data parity bit. If a parity error exists, an internal Sync Byte parity error flag is set. This flag is reset low when $\overline{SBL}$ goes high. The PERR output displays the write parity flag condition when $\overline{WG}$ is low. When $\overline{WG}$ is high, PERR outputs the state of the Sync Byte parity error flag. TTL output levels.

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
RCLK	O	READ CLOCK: A multiplexed byte clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RCLK initially remains synchronized to XTAL/12. When the Sync Byte is detected, RCLK is synchronized to the Read Data. When $\overline{RG}$ goes high, RCLK is synchronized back to the XTAL/12. TTL output levels.
$\overline{SBD}$	O	SYNC BYTE DETECT: A TTL output that transitions low upon detecting a Sync Byte. This transition is synchronized to the first NRZ byte out following the sync byte. Once it transitions, $\overline{SBD}$ remains low until $\overline{RG}$ is raised, when it is returned to a high state.
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
WD, $\overline{WD}$	O	WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RCLK and WCLK) to the XTAL reference clock. Differential +5 volts offset ECL (PECL) output levels.
NRZ0-7	I/O	NRZ DATA PORT: Read data output when $\overline{RG}$ is low, write data input when $\overline{WG}$ is low, and Sync Byte input when both $\overline{RG}$ and $\overline{WG}$ are high. TTL input and output levels.
NRZP	I/O	NRZ DATA PARITY BIT: Generated read data parity bit output when $\overline{RG}$ is low, write data parity bit input when $\overline{WG}$ is low, and Sync Byte parity bit input when both $\overline{RG}$ and $\overline{WG}$ are high. In read mode, even parity is generated. For example, when NRZ7-0 are all high, NRZP will be set low. TTL input and output levels.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin.
PD OUT	I/O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
RS	I	WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA.
VCO IN	I/O	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value.
XTAL1, 2	I	REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. If a crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. The crystal is connected between XTAL1 and XTAL2. If a crystal oscillator is not desired, XTAL1 may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal, with XTAL2 open.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75V < VPA/VPD < 5.25V, 0 °C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device

PARAMETER	RATING	UNIT
Supply Voltage, VPA1, VPA2, VPD	-0.3 to 6	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C
NRZ0 - NRZ7, RCLK, NCLK, WDT, $\overline{WDT}$, AMFND, SBFND, VCOREF, DRD Pins	-0.3 to (VPA/VPD+0.3), or +12	V mA
All other pins	-0.3 to (VPA/VPD+0.3)	V

POWER SUPPLY CURRENTS AND POWER

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
ICC (VPA, VPD) Supply Current	Outputs and test point pins open, Ta = 70 °C		200	230	mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 70 °C		1.0	1.2	W

DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs: $\overline{AMENB}$, EPD, NRZ0-NRZ7 (bid.), NRZP (bid.), $\overline{RG}$, $\overline{SBL}$, $\overline{W0}$, $\overline{W1}$, $\overline{W2}$, $\overline{WL}$, WCLK, $\overline{WG}$, WSD, $\overline{WSL}$ Pins

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Low Voltage (VIL)		-0.3		0.8	V
Input High Voltage (VIH)		2.0		VPD+0.3	V
Input Low Current	VIL = 0.4 V	0.0		-0.4	mA
Input High Current	VIH = 2.4 V			100	µA

Note: "bid." means bi-directional

TTL Compatible Outputs $\overline{AMD}$, NCLK, NRZ0-NRZ7 (bid.), NRZP (bid.), PERR, RCLK, $\overline{SBD}$ Pins

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Low Voltage	Iol = 4.0 mA			0.5	V
Output High Voltage	Ioh = -400 µA	2.4			V

Digital Differential Inputs: RD, $\overline{RD}$ Pins

Input Low Voltage (VIL)		VPA-2.2		VIH-0.5	V
Input High Voltage (VIH)		VIL+0.5		VPA-0.5	V
Differential Voltage	$\lvert V_{RD} - V_{\overline{RD}}\rvert$	0.5			V
Input Low Current	VIL = Min	-100			µA
Input High Current	VIH = Max			+100	µA

Digital Differential Outputs: WD, $\overline{WD}$ Pins

Output Low Voltage	Iol = TBD	VPD-2.1			V
Output High Voltage	Ioh = TBD			VPD-0.7	V
Differential Voltage	$\lvert V_{WD} - V_{\overline{WD}}\rvert$	0.5			V

Test Point Output Levels

Test Point Output High Level $\overline{DRD}$, VCO REF	262Ω to VPA, 402Ω to GND VPA = 5V		VPA -0.85		V
Test Point Output Low Level $\overline{DRD}$, VCO REF	262Ω to VPA, 402Ω to GND VPA = 5V		VPA -1.75		V

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Read Data Pulse Width (TPRD)		10		(2)TVCO -10	ns
Read Data Rise Time (TRRD)	20% to 80%, CL ≤ 10 pF			5	ns
Read Data Fall Time (TFRD)	80% to 20%, CL ≤ 10 pF			5	ns
Read Clock Rise Time (TRRC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
Read Clock Fall Time (TFRC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NCLK Rise Time (TRNC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
NCLK Fall Time (TFNC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NRZ (out) Set Up & Hold Time (TDS, TDH)		30			ns
$\overline{SBD}$ Set up & Hold Time (TSBS, TSBH)		30			ns

READ MODE (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
RCLK Pulse Width (TRD)	VCO re-sync	0.4 TORC		1.25 TORC	ns
	BYTE re-sync	0.4 TORC		1.6 TORC	ns
RCLK Duty Cycle		40		60**	%
NCLK Pulse Width (TQD)	Except during re-sync	(TORC/4)-5		(TORC/4)+5	ns
NCLK Pulse Width (TQD)	During re-sync	TORC/4-5		3TORC/4+5	ns
NCLK Skew (TQS)		-20		20	ns
RCLK Resync Period (Tdc2)		TORC		(2)TORC	ns
NCLK Resync Period (Tdc1)		TORC/2		TORC	ns
Decode Window Centering Accuracy				±0.75	ns
Decode Window		TVCO -0.75			ns

** Except during re-sync

WRITE MODE

Write Data Rise Time (TRWD)	20% to 80% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Fall Time (TFWD)	80% to 20% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Clock Rise Time (TRWC)	0.8V to 2.0V, CL ≤ 15 pF			10	ns
Write Data Clock Fall Time (TFWC)	2.0V to 0.8V, CL ≤ 15 pF			8	ns
NRZ Set Up Time (TSNRZ)		20			ns
NRZ Hold Time (THNRZ)		20			ns
Precompensation Time Shift Magnitude Accuracy (TPC)	TPCO = 0.22 (Rc + 0.53) Rc min=1 KΩ, Rc max=0.3TXTAL				
	$\overline{W0}$=1 $\overline{W1}$=1	-0.5		0.5	ns
	$\overline{W0}$=0 $\overline{W1}$=1	0.8 TPCO		1.2 TPCO	ns
	$\overline{W0}$=1 $\overline{W1}$=0	2 (0.8 TPCO)		2 (1.2 TPCO)	ns
	$\overline{W0}$=0 $\overline{W1}$=0	3 (0.8 TPCO)		3 (1.2 TPCO)	ns

DATA SYNCHRONIZATION

VCO Center Frequency Period (TVCO)	VCO IN=2.7V, VPA=VPD=5V TO=3.6 (RR+1.7), RR=(185/DR)-1.7K	0.8TO		1.2TO	ns
VCO Frequency Dynamic Range	1.0 V ≤ VCO IN ≤ VPA - 0.6V VPA=VPD = 5 V	± 25		± 45	%
VCO Control Gain (KVCO)	ωo = 2π/TVCO 1.0 V ≤ VCO IN ≤ VPA - 0.6V	0.14 ωo		0.26 ωo	rad/s V

DATA SYNCHRONIZATION (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Phase Detector Gain (KD)	VPA=VPD=5V Read: KD=750/(RR + 0.53) Non-Read: KD=375/(RR + 0.53)	0.83KD		1.17KD	µA/rad
KVCO x KD Product Accuracy		-28		+28	%
VCO Phase Restart Error	Referred to RRC	-1		+1	rad
1/3 Cell Delay	VCC = 5.0V TD=1.8 (RR + 1.7); RR = kΩ	0.8TD		1.2TD	ns

CONTROL TIMING

$\overline{W0}$, $\overline{W1}$, WSD Set Up and Hold Time (TSWC, THWC)		20			ns
$\overline{WL}$, $\overline{WSL}$ Pulse Width (TWL)		50			ns
Sync Byte NRZ Set Up and Hold Time (TSSB, THSB)		20			ns
$\overline{SBL}$ Pulse Width (TSB)		50			ns
Sync Byte Parity Error Output Delay (TDSE)		0		50	ns
Sync Byte Parity Error Reset Delay (TSER)		0		50	ns

MODE CONTROL

$\overline{WG}$	$\overline{RG}$	$\overline{AMENB}$	$\overline{SBL}$	Modes	
1	1	1	1	Idle (SB Enable)	Idle mode. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. SB latch transparent.
1	1	1	0	SB Load	SB latch in a hold state. Other conditions same as idle mode.
1	1	0	X	AM Search	Read mode Address Mark search. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ active.
1	0	1	X	Read Data	Read mode preamble search and data acquisition. VCO switched from XTAL to RD after preamble lock. Byte clock and 4-bit clock synchronized to RD after Sync Byte found. NRZ0-NRZ7 active. $\overline{SBD}$ active.
1	0	0	X	Undefined	Illegal state.
0	1	0	X	Write AM	Write mode Address Mark insertion. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high.
0	1	1	X	Write Data	Write mode preamble insertion and data write. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high.
0	0	1	X	Undefined	Illegal state.
0	0	0	X	Undefined	Illegal state.

WRITE PRECOMP CONTROL

$\overline{WL}$ - Write precomp latch control	$\overline{W1}$, $\overline{W0}$ - Write precomp magnitude control bits
0 → Write precomp control latches in hold state 1 → Write precomp control latches in transparent state	00 → 3x (maximum) shift 01 → 2x shift 10 → 1x shift 11 → No shift

WINDOW SHIFT CONTROL

$\overline{WSL}$ - Window shift latch control
0 → Window shift control latches in hold state
1 → Window shift control latches in transparent state

WSD - Window shift direction control
0 → Early window (+TS)
1 → Late window (-TS)

WINDOW SHIFT MAGNITUDE CONTROL BITS

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	TS0 (decode window %)
1	1	1	No shift
1	1	0	4% Minimum shift
1	0	1	8%
1	0	0	12%
0	1	1	15%
0	1	0	18%
0	0	1	20%
0	0	0	22% Maximum shift

Window shift with RRS used:	(2KΩ ≤ RRS ≤ 16 KΩ)
$TS = TSO\left(\frac{RRS}{RRS + 0.8}\right)$	TSO = Window shift set by $\overline{W0}$ - $\overline{W1}$ with no RRS

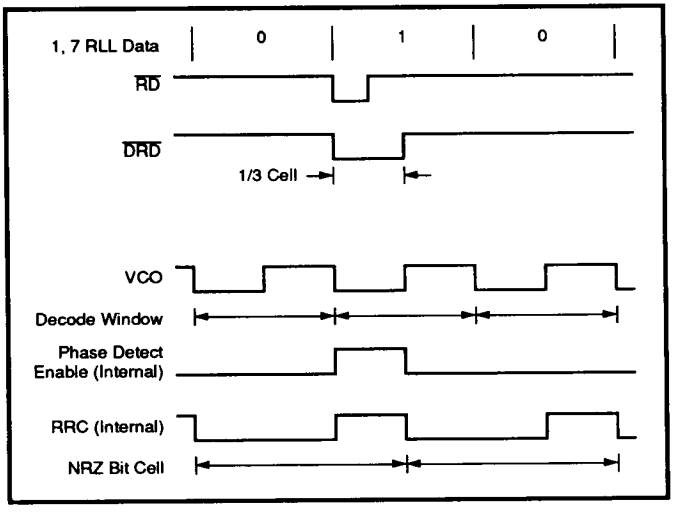


FIGURE 3: Data Synchronization Waveforms

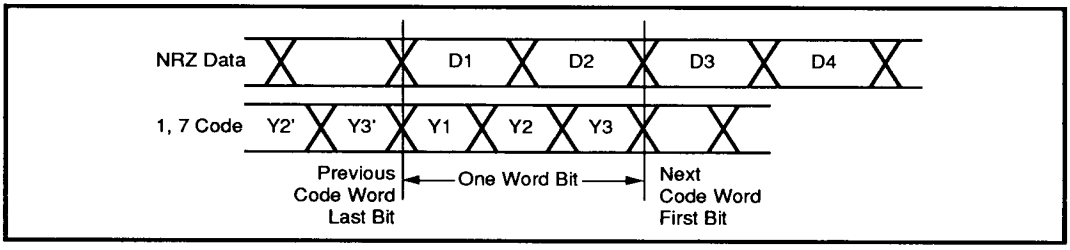


FIGURE 4: NRZ Data Word Comparison to 1, 7 Code Word Bit
(See Table 1 for Decode Scheme)

TABLE 1: 1, 7 RLL Code Set

Previous Code Word Last Bits		Data Bits Present		Data Bits Next		Code Bits		
X	0	1	0	0	X	1	0	1
X	0	1	0	1	X	0	1	0
X	0	1	1	0	0	0	1	0
X	0	1	1	*	*	1	0	0
1	0	0	0	0	X	0	0	1
1	0	0	0	1	X	0	0	0
0	0	0	1	0	X	0	0	1
0	0	0	1	1	X	0	0	0
X	1	0	0	0	X	0	0	1
X	1	0	0	1	X	0	1	0
X	1	0	1	0	0	0	1	0
X	1	0	1	*	*	0	0	0
Y2'	Y3	D1	D2	D3	D4	Y1	Y2	Y3

X = Don't Care;
* = Not All Zeros

TABLE 2: Clock Frequency

$\overline{WG}$	$\overline{RG}$	VCO REF	RCLK	DECCLK	ENCCLK	MODE
1	1	XTAL	XTAL/12	XTAL	XTAL	IDLE
1	0	RD	VCO/12	VCO	XTAL	READ
0	1	XTAL	XTAL/12	XTAL	XTAL	WRITE

Notes 1: Until the VCO locks to the new source, the VCO entries will be XTAL.
2: Until the VCO locks to the new source, the VCO/12 entries will be XTAL/12.
3: $\overline{WG}$ = $\overline{RG}$ = 0 is undefined.

TABLE 3: Write Precompensation Algorithm

Bit n-2	Bit n-1	Bit n	Bit n+1	Bit n+2	Compensation
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Notes Late: Bit n is time shifted (delayed) from its normal time position towards the Bit n+1 time position.
Early: Bit n is time shifted (advanced) from its normal time position towards the Bit n-1 time position.

TABLE 4: Write Precompensation Magnitude

$\overline{WC1}$	$\overline{WC0}$	Magnitude, TPC
0	0	3 (TPC0)
0	1	2 (TPC0)
1	0	TPC0
1	1	0

The normal magnitude TPC0 is externally set with a resistor on pin WCS.

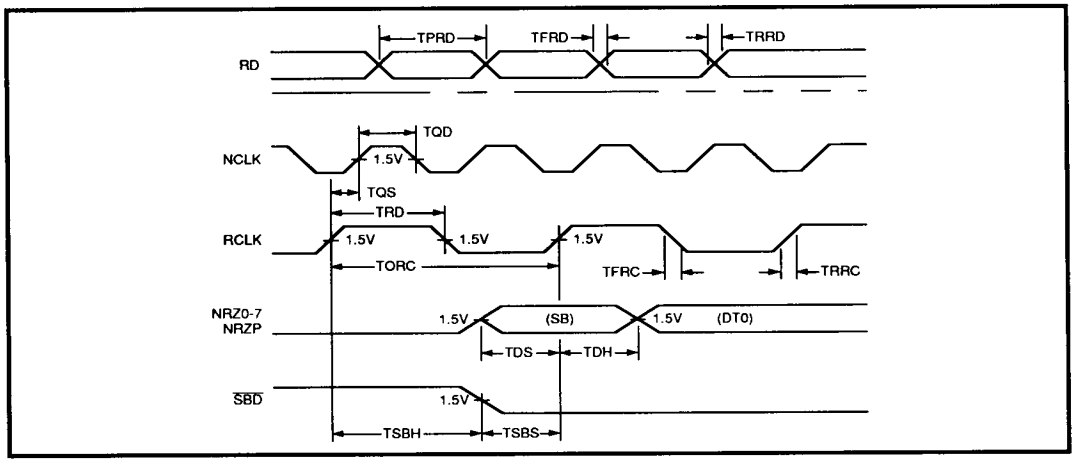


FIGURE 5: Read Timing

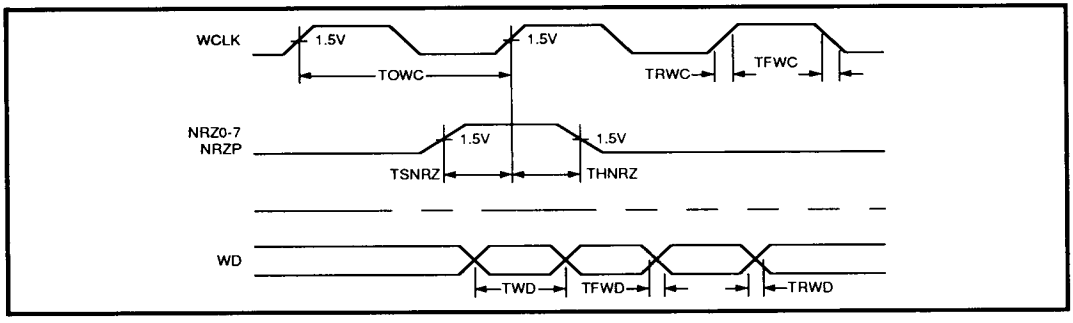


FIGURE 6: Write Timing

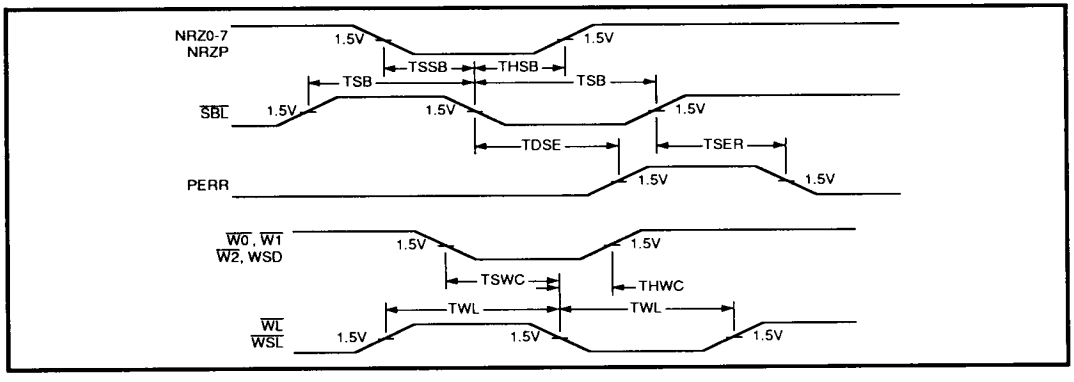


FIGURE 7: Control Timing

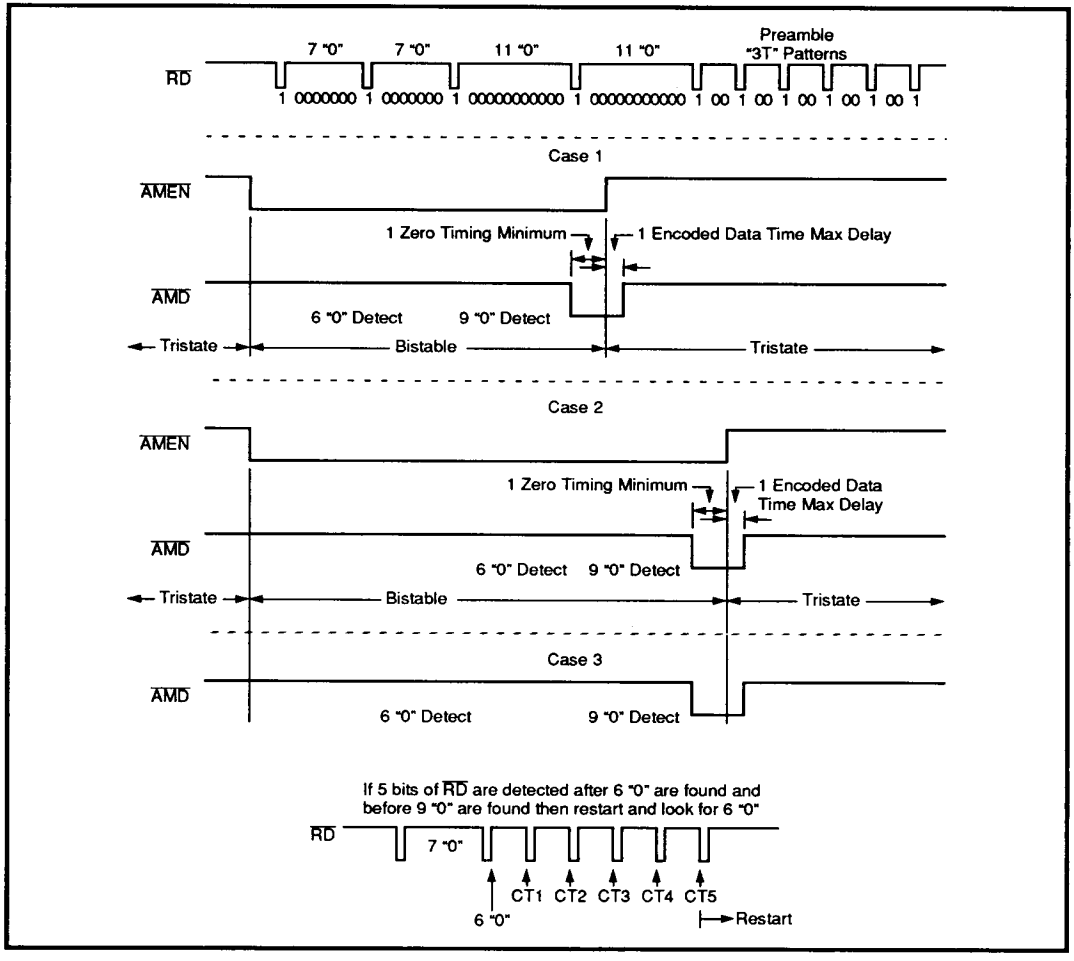


FIGURE 8: Address Mark Search

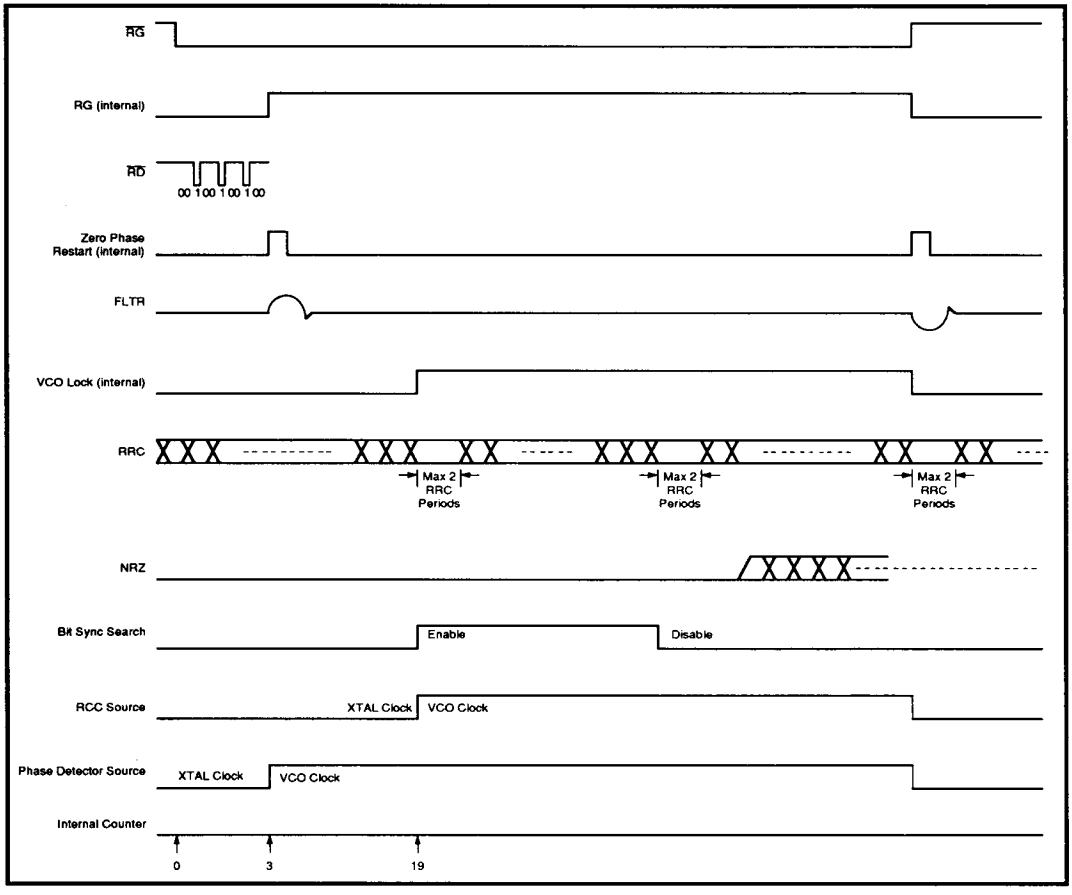


FIGURE 9: Read Mode Locking Sequence (Soft and Hard Sector)

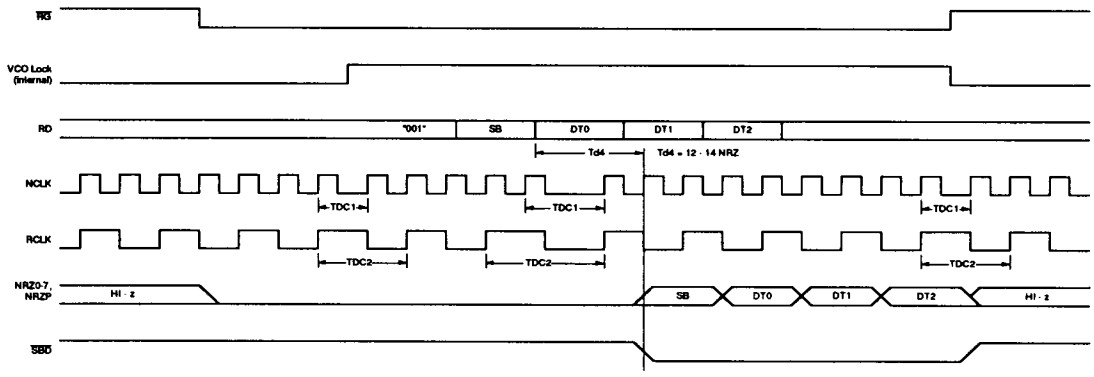


FIGURE 10: Read Mode NRZ Data Timing

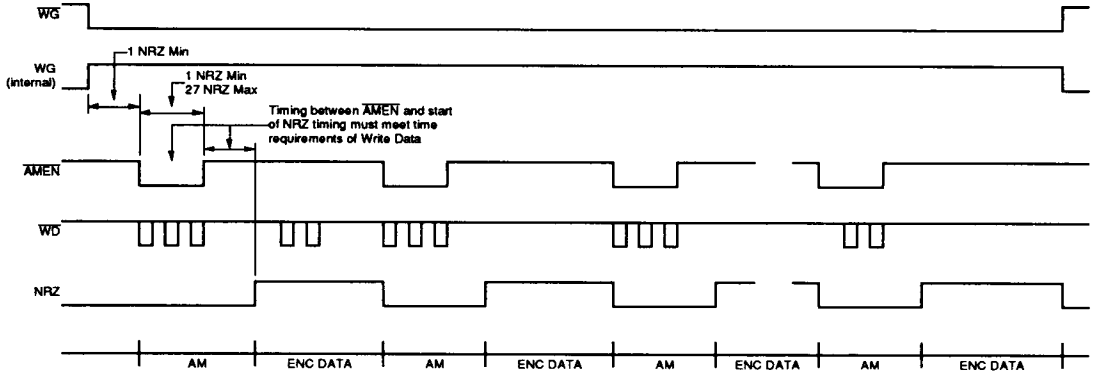


FIGURE 11: Multiple Address Mark Write

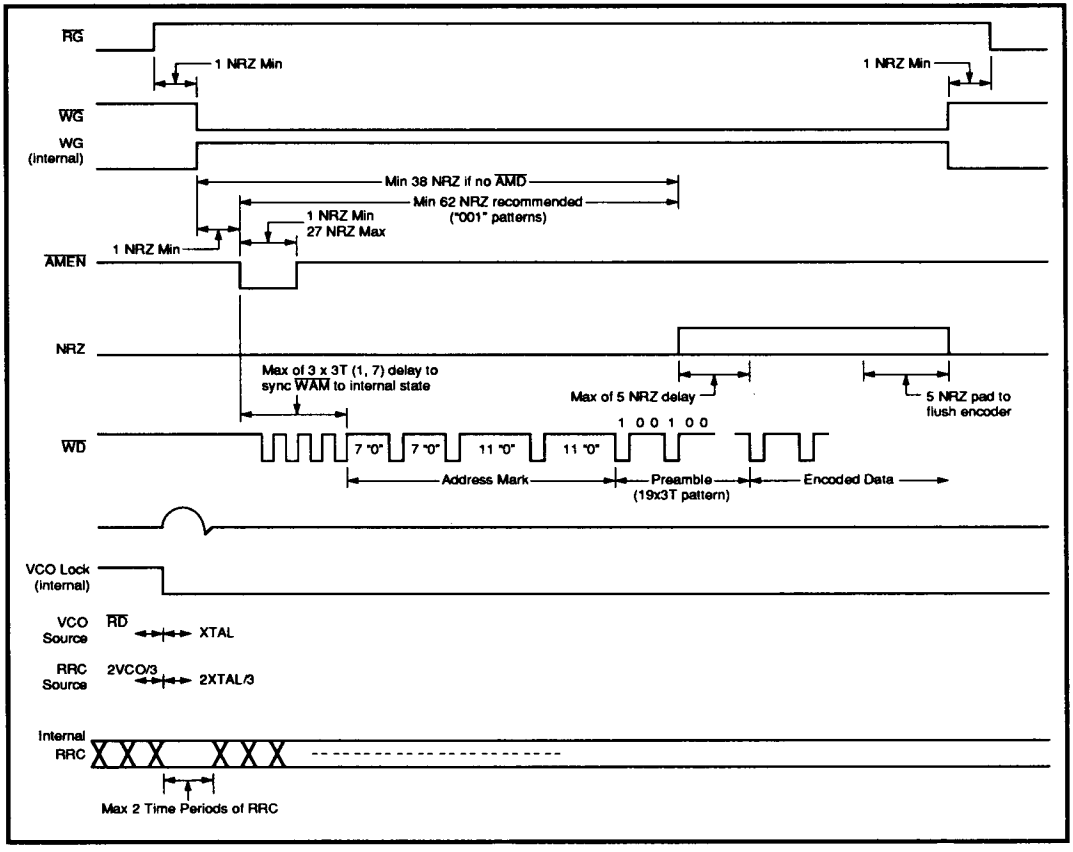


FIGURE 12: Write Data

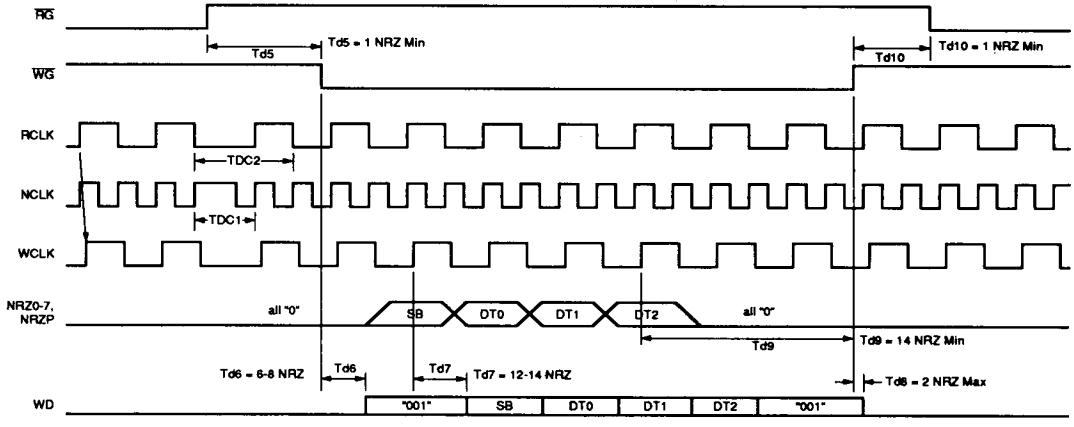


FIGURE 13: Write Mode NRZ Timing

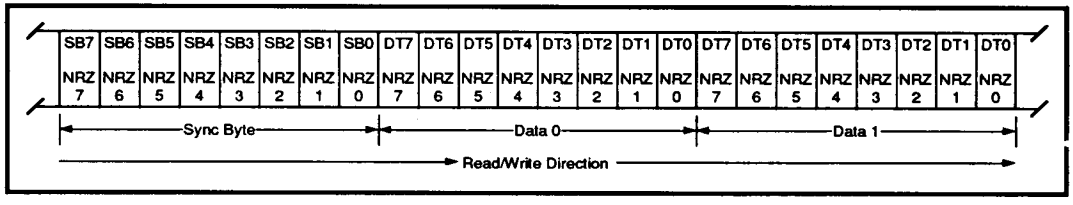
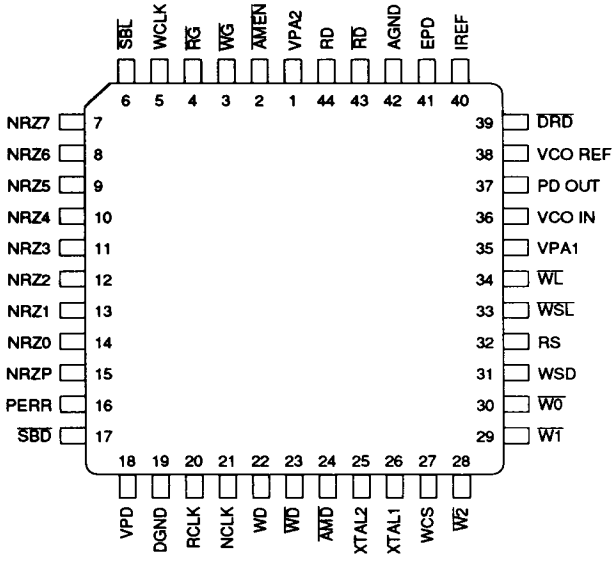


FIGURE 14: Parallel/Serial Conversion Format

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D539		
44-Pin PLCC	32D539-CH	32D539-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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