

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
 - 120 ns access time available
- CMOS Technology for low power consumption
 - 20 mA Active current
 - 100 μ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin Chip carrier (leadless or plastic)
 - 28-pin SOIC package
 - 28-pin TSOP package
 - Tape and reel
- Available for the following temperature ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C
 - Automotive: -40°C to +125°C

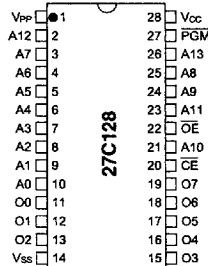
DESCRIPTION

The Microchip Technology Inc. 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements. A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

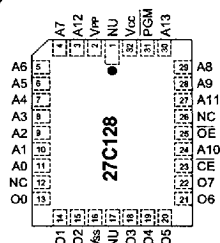
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PACKAGE TYPE

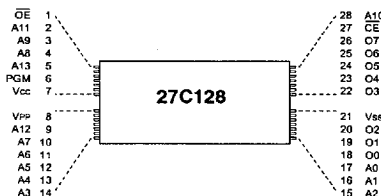
DIP/SOIC



PLCC/LCC



TSOP



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} -0.6V to +7.25VV_{PP} voltage w.r.t. V_{SS} during

programming -0.6V to +14V

Voltage on A9 w.r.t. V_{SS} -0.6V to +13.5VOutput voltage w.r.t. V_{SS} -0.6V to V_{CC} +1.0V

Storage temperature -65°C to +150°C

Ambient temp. with power applied -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
V _{PP}	Programming Voltage
O0 - O7	Data Output
V _{CC}	+5V Power Supply
V _{SS}	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V _{CC} = +5V (±10%) Commercial: T _{amb} = 0°C to +70°C Industrial: T _{amb} = -40°C to +85°C Extended (Automotive): T _{amb} = -40°C to +125°C							
Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V _{IH} V _{IL}	2.0 -0.5	V _{CC} +1 0.8	V V	
Input Leakage	all	—	I _{LI}	-10	10	μA	V _{IN} = 0 to V _{CC}
Output Voltages	all	Logic "1" Logic "0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400 μA I _{OL} = 2.1 mA
Output Leakage	all	—	I _{LO}	-10	10	μA	V _{OUT} = 0V to V _{CC}
Input Capacitance	all	—	C _{IN}	—	6	pF	V _{IN} = 0V; T _{amb} = 25°C; f = 1 MHz
Output Capacitance	all	—	C _{OUT}	—	12	pF	V _{OUT} = 0V; T _{amb} = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	I _{CC1} I _{CC2}	— —	20 25	mA mA	V _{CC} = 5.5V; V _{PP} = V _{CC} f = 1 MHz; $\overline{OE} = \overline{CE} = V_{IL}$; I _{OUT} = 0 mA; V _{IL} = -0.1 to 0.8V; V _{IH} = 2.0 to V _{CC} ; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	I _{CC} (s)	— — —	2 3 100	mA mA μA	$\overline{CE} = V_{CC} \pm 0.2V$
I _{PP} Read Current V _{PP} Read Voltage	all all	Read Mode Read Mode	I _{PP} V _{PP}	V _{CC} -0.7	100 V _{CC}	μA V	V _{PP} = 5.5V Note 2

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

Note 2: V_{CC} must be applied before V_{PP}, and be removed simultaneously or after V_{PP}.

AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$ $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial: $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ Extended (Automotive): $T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$													
Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t _{ACC}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t _{CE}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t _{OE}	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t _{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t _{OH}	0	—	0	—	0	—	0	—	0	—	ns	

Timing diagram for the 74VHC02 showing Address, $\overline{CE}$, $\overline{OE}$, and Outputs (O0 - O7) signals. The diagram illustrates the relationship between these signals during a memory access cycle.

- Address:** Valid throughout the cycle.
- $\overline{CE}$ (Chip Enable):** Active-low signal. It is active from $t_{CE(2)}$ after its falling edge until $t_{CE(1)}$ before its rising edge.
- $\overline{OE}$ (Output Enable):** Active-low signal. It is active from $t_{OE(2)}$ after its falling edge until $t_{OE(1)}$ before its rising edge.
- Outputs (O0 - O7):** The output is in High Z state when both $\overline{CE}$ and $\overline{OE}$ are inactive. The output is valid from t_{ACC} after the falling edge of $\overline{CE}$ until $t_{OFF(1,3)}$ after the rising edge of either $\overline{CE}$ or $\overline{OE}$. The output is in High Z state when both $\overline{CE}$ and $\overline{OE}$ are active.

Notes:

- (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
- (2) $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}
- (3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V						
Parameter	Status	Symbol	Min	Max.	Units	Conditions
Input Voltages	Logic"1" Logic"0"	V _{IH} V _{IL}	2.0 -0.1	V _{CC} +1 0.8	V V	
Input Leakage	—	I _{LI}	-10	10	μA	V _{IN} = 0V to V _{CC}
Output Voltages	Logic"1" Logic"0"	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400 μA I _{OL} = 2.1 mA
VCC Current, program & verify	—	I _{CC2}	—	20	mA	Note 1
VPP Current, program	—	I _{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V _H	11.5	12.5	V	

Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: $V_{IH}=2.4V$ and $V_{IL}=0.45V$; $V_{OH}=2.0V$; $V_{OL}=0.8V$ Ambient Temperature: $T_{amb}=25^{\circ}C \pm 5^{\circ}C$ $V_{CC}=6.5V \pm 0.25V$, $V_{PP} = V_H = 13.0V \pm 0.25V$				
Parameter	Symbol	Min	Max	Units	Remarks	
Address Set-Up Time	tAS	2	—	μs		
Data Set-Up Time	tDS	2	—	μs		
Data Hold Time	tDH	2	—	μs		
Address Hold Time	tAH	0	—	μs		
Float Delay (2)	tDF	0	130	ns		
VCC Set-Up Time	tVCS	2	—	μs		
Program Pulse Width (1)	tPW	95	105	μs	100 μs typical	
$\overline{CE}$ Set-Up Time	tCES	2	—	μs		
$\overline{OE}$ Set-Up Time	tOES	2	—	μs		
VPP Set-Up Time	tVPS	2	—	μs		
Data Valid from $\overline{OE}$	tOE	—	100	ns		

Note 1: For express algorithm, initial programming width tolerance is 100 μs ±5%.

Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)

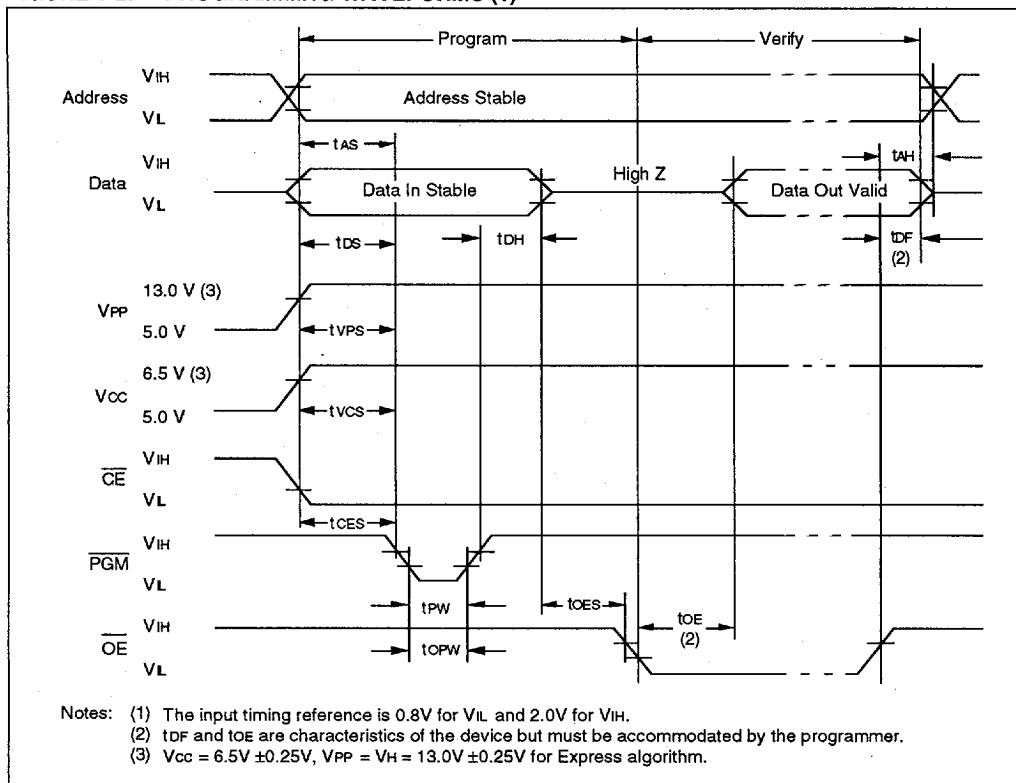


TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	DOUT
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	DIN
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_H	X	DOUT
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the $\overline{CE}$ pin is low to power up (enable) the chip
- the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 μ A.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 μ W/cm² for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

- Vcc is brought to the proper voltage,
- Vpp is brought to the proper V_H level,
- the $\overline{CE}$ pin is low,
- the $\overline{OE}$ pin is high, and
- the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- Vcc is at the proper level,
- Vpp is at the proper V_H level,
- the $\overline{CE}$ line is low,
- the $\overline{PGM}$ line is high, and
- the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

1.9 Identity Mode

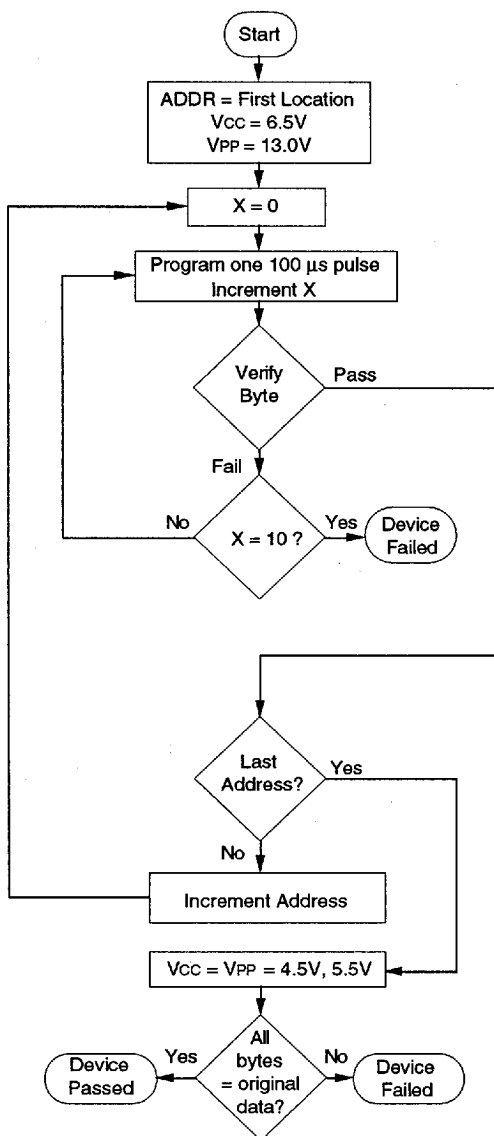
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin $\rightarrow$	Input	Output							
Identity $\downarrow$	A0	0	0	0	0	0	0	0	H
		7	6	5	4	3	2	1	e
Manufacturer Device Type*	V _{IL}	0	0	1	0	1	0	0	1
	V _H	1	0	0	0	0	0	1	83

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM

Conditions:
 $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$
 $V_{CC} = 6.5 \pm 0.25\text{V}$
 $V_{PP} = 13.0 \pm 0.25\text{V}$



27C128

27C128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C128	-	25	I	/P	
					Package:
					J CERDIP
					K Ceramic Leadless Chip Carrier
					L Plastic Leaded Chip Carrier
					P Plastic DIP
					SO Plastic SOIC
					TS Thin Small Outline Package (TSOP) 8X13.4mm
					Temperature
					- 0°C to +70°C
					Range:
					I -40°C to +85°C
					E -40°C to +125°C
					Access
					12 120 ns
					Time:
					15 150 ns
					17 170 ns
					20 200 ns
					25 250 ns
					Device:
					27C128 128K (16K x 8) CMOS EPROM