REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Editorial changes to table I 8/ and changes to case outlines X and Y. - tmh	99-11-24	Monica L. Poelking

REV																				
SHEET	55																			
REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV					A			A		A	A		A							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																		
	REV		A															
	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Thanh V. Nguyen

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
99-02-17

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, DIGITAL SIGNAL PROCESSOR, 32-BIT, MONOLITHIC SILICON

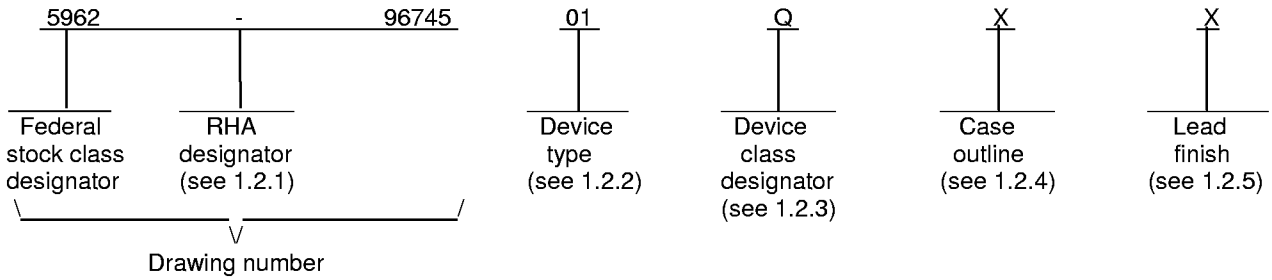
SIZE	CAGE CODE	
A	**67268**	**5962-96745**

SHEET 1 OF 55

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	21062	32-bit digital signal processor, 2 Mbit SRAM
02	21060	32-bit digital signal processor, 4 Mbit SRAM

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	240	Gull wing flatpack cavity down heat sink
Y	See figure 1	240	Gull wing flatpack cavity up heat sink
T	See figure 1	240	Flatpack with non-conductive tie-bar cavity down heat sink
U	See figure 1	240	Flatpack with non-conductive tie-bar cavity up heat sink

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.3 V dc to V_{DD} + 0.3 V dc
Output voltage range (V_{OUT})	-0.3 V dc to V_{DD} + 0.3 V dc
Load capacitance	200 pF
Lead temperature (soldering, 5 seconds)	+280°C
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	5 W
Thermal resistance junction-to-case (Θ_{JC}):	
Cases X,Y, T, and U	0.24°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.75 V dc to +5.25 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stress above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values are not available.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 132 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Theses devices shall be compliant to IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage 2/	V_{IH}	V_{DD} = max	1, 2, 3	All	2.0		V
High level input voltage 3/	V_{IHCR}	V_{DD} = max	1, 2, 3	All	2.2		
Low level input voltage 2/ 3/	V_{IL}	V_{DD} = min	1, 2, 3	All		0.8	
High level output voltage 4/ 5/	V_{OH}	V_{DD} = min, I_{OH} = -2.0 mA	1, 2, 3	All	4.1		
Low level output voltage 4/ 5/	V_{OL}	V_{DD} = min, I_{OL} = 4.0 mA	1, 2, 3	All		0.4	
High level input current 6/ 7/	I_{IH}	V_{DD} = max, $V_{IN} = V_{DD}$ = max	1, 2, 3	All		10	µA
Low level input current 6/	I_{IL}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		10	
Low level input current 7/	I_{ILP}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		150	
Three-state leakage current 8/ 9/ 10/ 11/	I_{OZH}	V_{DD} = max, $V_{IN} = V_{DD}$ = max	1, 2, 3	All		10	
Three-state leakage current 8/ 13/	I_{OZL}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		10	
Three-state leakage current 13/	I_{OZHP}	V_{DD} = max, $V_{IN} = V_{DD}$ = max	1, 2, 3	All		350	
Three-state leakage current 10/	I_{OZLC}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		1.5	mA
Three-state leakage current 12/	I_{OZLA}	V_{DD} = max, V_{IN} = 1.5 V	1, 2, 3	All		350	µA
Three-state leakage current 11/	I_{OZLAR}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		4.2	mA
Three-state leakage current 9/	I_{OZLS}	V_{DD} = max, V_{IN} = O V	1, 2, 3	All		150	µA
Supply current (internal) 14/	I_{DDIN}	t_{CK} = 25 ns, V_{DD} = max	1, 2, 3	All		730 15/	mA
Supply current (idle) 16/	I_{DDIDLE}	t_{CK} = 25 ns, V_{DD} = max	1, 2, 3	All		300	
Input capacitance 17/ 18/	C_{IN}	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V See 4.4.1c	4	All		4.7	pF
Functional test		See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKIN period	t_{CK}	See figure 4 18/	9, 10, 11	All	25	100	ns
CLKIN width low	t_{CKL}		9, 10, 11	All	7		
CLKIN width high	t_{CKH}		9, 10, 11	All	5		
CLKIN rise/fall (0.4 V-2.0 V)	t_{CKRF}		9, 10, 11	All		3	
$\overline{\text{RESET}}$ pulse width low 19/	t_{WRST}		9, 10, 11	All	$4t_{CK}$		
$\overline{\text{RESET}}$ setup before CLKIN high 20/	t_{SRST}		9, 10, 11	All	14+DT/2	t_{CK}	
$\overline{\text{IRQ2-0}}$ setup before CLKIN high 21/	t_{SIR}		9, 10, 11	All	18+3DT/4		
$\overline{\text{IRQ2-0}}$ hold before CLKIN high 21/	t_{HIR}		9, 10, 11	All		12+3DT/4	
$\overline{\text{IRQ2-0}}$ pulse width 22/	t_{IPW}		9, 10, 11	All	$2+t_{CK}$		
CLKIN high to TIMEXP	t_{DTEX}		9, 10, 11	All		15	
FLAG3-0_{IN} setup before CLKIN high 23/	t_{SFI}		9, 10, 11	All	8+5DT/16		
FLAG3-0_{IN} hold after CLKIN high 23/	t_{HFI}		9, 10, 11	All	0-5DT/16		
FLAG3-0_{IN} delay after $\overline{\text{RD}}$ / $\overline{\text{WR}}$ low 23/	t_{DWRFI}		9, 10, 11	All		5+7DT/16	
FLAG3-0_{IN} hold after $\overline{\text{RD}}$ / $\overline{\text{WR}}$ deasserted 23/	t_{HFIWR}		9, 10, 11	All	0		
FLAG3-0_{OUT} delay after CLKIN high	t_{DFO}		9, 10, 11	All		16	
FLAG3-0_{OUT} hold after CLKIN high	t_{HFO}		9, 10, 11	All	4		
CLKIN high to FLAG3-0_{OUT} enable	t_{DFOE}		9, 10, 11	All	3		
CLKIN high to FLAG3-0_{OUT} disable	t_{DFOD}		9, 10, 11	All		14	
Address, Selects delay to data valid 24/ 25/	t_{DAD}		9, 10, 11	All		18+DT+W	
$\overline{\text{RD}}$ low to data valid 24/	t_{DRLD}		9, 10, 11	All		12+5DT/8+W	
Data hold from Address, Selects 26/ 27/	t_{HAD}		9, 10, 11	All	0.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold from $\overline{RD}$ High 26/ 27/	t_{HDRH}	See figure 4 18/	9, 10, 11	All	2.0		ns
ACK delay from Address, Selects 25/ 28/	t_{DAAK}		9, 10, 11	All		14+7DT/8+W	
ACK delay from $\overline{RD}$ Low 28/	t_{DSAK}		9, 10, 11	All		8+DT/2+W	
Address, Selects setup before ADRCLK high	t_{DRHA}		9, 10, 11	All	0 + H		
Address, Selects to $\overline{RD}$ low 25/	t_{DARL}		9, 10, 11	All	2+3DT/8		
$\overline{RD}$ pulse width	t_{RW}		9, 10, 11	All	12.5+5DT/8+W		
$\overline{RD}$ high to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ low	t_{RWR}		9, 10, 11	All	8+3DT/8+HI		
Address, Selects setup before ADRCLK high 25/	t_{SADADC}		9, 10, 11	All	0+DT/4		
Address, selects to $\overline{WR}$ deasserted 25/	t_{DAWH}		9, 10, 11	All	17+15DT/16+W		
Address, selects to $\overline{WR}$ low 25/	t_{DAWL}		9, 10, 11	All	3+3DT/8		
$\overline{WR}$ pulse width	t_{WW}		9, 10, 11	All	12+9DT/16+W		
Data setup before $\overline{WR}$ high	t_{DDWH}		9, 10, 11	All	7+DT/2+W		
Address hold after $\overline{WR}$ deasserted	t_{DWHA}		9, 10, 11	All	0.5+DT/16+H		
Data disable after $\overline{WR}$ deasserted 27/	t_{DATRWH}		9, 10, 11	All	1+DT/16+H	6+DT/16+H	
$\overline{WR}$ high $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ low	t_{WWR}		9, 10, 11	All	8+7DT/16+H		
Data disable before $\overline{WR}$ or $\overline{RD}$ low	t_{DDWR}		9, 10, 11	All	5+3DT/8+I		
$\overline{WR}$ low to data enabled	t_{WDE}		9, 10, 11	All	-1+DT/16		
Data setup before CLKIN	t_{SSDATI}		9, 10, 11	All	3+DT/8		
Data hold after CLKIN	t_{HSDATI}		9, 10, 11	All	3.5-DT/8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ACK setup before CLKIN	t_{SACKC}	See figure 4 18/	9, 10, 11	All	6.5+DT/4		ns
ACK hold after CLKIN	t_{HACK}		9, 10, 11	All	-1-DT/4		
Address, $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ delay after CLKIN 25/	t_{DADRO}		9, 10, 11	All		7-DT/8	
Address, $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ hold after CLKIN	t_{HADRO}		9, 10, 11	All	-1-DT/8		
PAGE delay after CLKIN	t_{DPGC}		9, 10, 11	All	9 + DT/8	16+DT/8	
$\overline{RD}$ high delay after CLKIN	t_{DRDO}		9, 10, 11	All	-2-DT/8	4-DT/8	
$\overline{WR}$ high delay after CLKIN	t_{DWRO}		9, 10, 11	All	-3-3DT/16	4-3DT/16	
$\overline{RD}$ / $\overline{WR}$ low delay after CLKIN	t_{DRWL}		9, 10, 11	All	8+DT/4	12.5+DT/4	
Data delay after CLKIN	t_{SDDATO}		9, 10, 11	All		19.5+5DT/16	
Data disable after CLKIN 27/	t_{DATTR}		9, 10, 11	All	0-DT/8	7-DT/8	
ADRCLK delay after CLKIN	t_{DADCCK}		9, 10, 11	All	4+DT/8	10+DT/8	
ADRCLK period	t_{ADRCK}		9, 10, 11	All	t_{CK}		
ADRCLK width high	t_{ADRCKH}		9, 10, 11	All	$(t_{CK}/2)-2$		
ADRCLK width low	t_{ADRCKL}		9, 10, 11	All	$(t_{CK}/2)-2$		
Address, $\overline{SW}$ setup before CLKIN	t_{SADRI}		9, 10, 11	All	15+DT/2		
Address, $\overline{SW}$ hold before CLKIN	t_{HADRI}		9, 10, 11	All		5+DT/2	
$\overline{RD}$ / $\overline{WR}$ low setup before CLKIN 29/	t_{SRWLI}		9, 10, 11	All	9.5+5DT/16		
$\overline{RD}$ / $\overline{WR}$ low hold before CLKIN	t_{HRWLI}		9, 10, 11	All	-3.5-5DT/16	8+7DT/16	
$\overline{RD}$ / $\overline{WR}$ pulse high	t_{RWHPI}		9, 10, 11	All	3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup before $\overline{WR}$ high	t_{SDATWH}	See figure 4 18/	9, 10, 11	All	5		ns
Data hold after $\overline{WR}$ high	t_{HDATWH}		9, 10, 11	All	1		
Data disable after CLKIN 27/	t_{DATTR}		9, 10, 11	All	0-DT/8	7-DT/8	
ACK delay after address, $\overline{SW}$ 30/	t_{DACKAD}		9, 10, 11	All		9	
ACK disable after CLKIN 30/	t_{ACKTR}		9, 10, 11	All	-1-DT/8	6-DT/8	
$\overline{HBG}$ low to $\overline{RD}$ / $\overline{WR}$ / $\overline{CS}$ valid 31/	$t_{HBGRCSV}$		9, 10, 11	All		20+5DT/4	
$\overline{HBR}$ setup before CLKIN 32/	t_{SHBRI}		9, 10, 11	All	20+3DT/4		
$\overline{HBR}$ hold before CLKIN 32/	t_{HHBRI}		9, 10, 11	All		14+3DT/4	
$\overline{HBG}$ setup before CLKIN	t_{SHBGI}		9, 10, 11	All	13+DT/2		
$\overline{HBG}$ hold before CLKIN high	t_{HHBGI}		9, 10, 11	All		5.75+DT/2	
$\overline{BRx}$, $\overline{CPA}$ setup before CLKIN 33/	t_{SBRI}		9, 10, 11	All	13+DT/2		
$\overline{BRx}$, $\overline{CPA}$ hold before CLKIN high	t_{HBRI}		9, 10, 11	All		6+DT/2	
RPBA setup before CLKIN	t_{SRPBAI}		9, 10, 11	All	21+3DT/4		
RPBA hold before CLKIN	t_{HRPBAI}		9, 10, 11	All		12+3DT/4	
$\overline{HBG}$ delay after CLKIN	t_{DHBGO}		9, 10, 11	All		7-DT/8	
$\overline{HBG}$ hold after CLKIN	t_{HHBGO}		9, 10, 11	All	-2-DT/8		
$\overline{BRx}$ delay after CLKIN	t_{DBRO}		9, 10, 11	All		7-DT/8	
$\overline{BRx}$ hold after CLKIN	t_{HBRO}		9, 10, 11	All	-2-DT/8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CPA}$ low delay after CLKIN	t_{DCPAO}	See figure 4 18/	9, 10, 11	All		8-DT/8	ns
$\overline{CPA}$ disable after CLKIN	t_{TRCPA}		9, 10, 11	All	-2-DT/8	4.5-DT/8	
READY (o/d) or (a/d) low from $\overline{CS}$ and $\overline{HBR}$ low 34/	t_{DRDYCS}		9, 10, 11	All		8.5	
READY (o/d)disable or READY (a/d) low from $\overline{HBG}$ 34/	t_{TRDYHG}		9, 10, 11	All	40+23DT/16		
READY (a/d)disable from $\overline{CS}$ or $\overline{HBR}$ high 34/	t_{ARDYTR}		9, 10, 11	All		10	
Address setup/ $\overline{CS}$ low before $\overline{RD}$ low 35/ 31/	t_{SADRDL}		9, 10, 11	All	0		
Address hold/ $\overline{CS}$ hold low after $\overline{RD}$	t_{HADRDH}		9, 10, 11	All	0		
$\overline{RD}$ / $\overline{WR}$ high Width	t_{WRWH}		9, 10, 11	All	6		
$\overline{RD}$ high delay after READY (o/d or a/d) disable 34/	$t_{DRDHRDY}$		9, 10, 11	All	0		
Data valid before READY disable from low	$t_{SDATRDY}$		9, 10, 11	All	2		
READY (o/d or a/d) low delay after RD low 34/	$t_{DRDYRDL}$		9, 10, 11	All		10	
READY (o/d or a/d) low pulse width for read	t_{RDYPRD}		9, 10, 11	All	45+21DT/16		
Data disable after $\overline{RD}$ high	t_{HDARWH}		9, 10, 11	All	2	8	
$\overline{CS}$ low setup before $\overline{WR}$ low	t_{SCSWRL}		9, 10, 11	All	0		
$\overline{CS}$ low hold after $\overline{WR}$ high	t_{HCSWRH}		9, 10, 11	All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup before $\overline{WR}$ high	t_{SADWRH}	See figure 4 18/	9, 10, 11	All	5		ns
Address hold after $\overline{WR}$ high	t_{HADWRH}		9, 10, 11	All	2		
$\overline{WR}$ low width	t_{WWRL}		9, 10, 11	All	7		
$\overline{RD}$ / $\overline{WR}$ high width	t_{WRWH}		9, 10, 11	All	6		
$\overline{WR}$ high delay after REDY (o/d or a/d) disable	$t_{DWRHRDY}$		9, 10, 11	All	0		
Data Setup before $\overline{WR}$ high	t_{SDATWH}		9, 10, 11	All	5		
Data hold after $\overline{WR}$ high	t_{HDATWH}		9, 10, 11	All	1		
REDY (o/d or a/d) low delay after $\overline{WR}$ / $\overline{CS}$ low	$t_{DRDYWRL}$		9, 10, 11	All		10	
REDY (o/d or a/d) low pulse width for write	t_{RDYPWR}		9, 10, 11	All	15+7DT/16		
REDY (o/d or a/d) disable to CLKIN	t_{SRDYCK}		9, 10, 11	All	1+7DT/16	8+7DT/16	
$\overline{SBTS}$ setup before CLKIN	t_{STSCK}		9, 10, 11	All	12+DT/2		
$\overline{SBTS}$ hold before CLKIN	t_{HTSCK}		9, 10, 11	All		6+DT/2	
Address/Selects enable after CLKIN	t_{MIENA}		9, 10, 11	All	-1.5-DT/8		
Strobes enable after CLKIN 36/	t_{MIENS}		9, 10, 11	All	-1.5-DT/8		
$\overline{HBG}$ enable after CLKIN	t_{MIENHG}		9, 10, 11	All	-1.5-DT/8		
Address/Selects disable after CLKIN	t_{MITRA}		9, 10, 11	All		0.15-DT/4	
Strobes disable after CLKIN 36/	t_{MITRS}		9, 10, 11	All		1.5-DT/4	
$\overline{HBG}$ disable after CLKIN	t_{MITRHG}		9, 10, 11	All		2.0-DT/4	
Data enable after CLKIN 37/	t_{DATEN}		9, 10, 11	All	9+5DT/16		
Data disable after CLKIN 37/	t_{DATTR}		9, 10, 11	All	0-DT/8	7-DT/8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ACK enable after CLKIN 37/	t_{ACKEN}	See figure 4 18/	9, 10, 11	All	7.5+DT/4		ns
ACK disable after CLKIN 37/	t_{ACKTR}		9, 10, 11	All	-1-DT/8	6-DT/8	
ADRCLK enable after CLKIN	t_{ADCEN}		9, 10, 11	All	-2-DT/8		
ADRCLK disable after CLKIN	t_{ADCTR}		9, 10, 11	All		8-DT/4	
Memory interface disable before $\overline{HBG}$ low 38/	t_{MTRHBG}		9, 10, 11	All	0+DT/8		
Memory interface enable after $\overline{HBG}$ high 38/	t_{MENHBG}		9, 10, 11	All	19+DT		
$\overline{DMARx}$ low setup before CLKIN 32/	t_{SDRLC}		9, 10, 11	All	5		
$\overline{DMARx}$ high setup before CLKIN 32/	t_{SDRHC}		9, 10, 11	All	5		
$\overline{DMARx}$ width low (nonsynchronous)	t_{WDR}		9, 10, 11	All	6		
Data setup after $\overline{DMAGx}$ low 39/	$t_{SDATDGL}$		9, 10, 11	All		10+5DT/8	
Data hold after $\overline{DMAGx}$ high	$t_{HDATIDG}$		9, 10, 11	All	2		
Data valid after $\overline{DMARx}$ high 39/	t_{DATDRH}		9, 10, 11	All		16+7DT/8	
$\overline{DMARx}$ low edge to low edge	t_{DMARLL}		9, 10, 11	All	23+7DT/8		
$\overline{DMARx}$ width high	t_{DMARH}		9, 10, 11	All	6		
$\overline{DMAGx}$ low delay after CLKIN	t_{DDGL}		9, 10, 11	All	9+DT/4	15+DT/4	
$\overline{DMAGx}$ high width	t_{WDGH}		9, 10, 11	All	6+3DT/8		
$\overline{DMAGx}$ low width	t_{WDGL}		9, 10, 11	All	12+5DT/8		
$\overline{DMAGx}$ high delay after CLKIN	t_{HDGC}		9, 10, 11	All	-2-DT/8	6-DT/8	
Data valid before $\overline{DMAGx}$ high 40/	$t_{VDATDGH}$		9, 10, 11	All	8+9DT/16		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data disable after $\overline{\text{DMAGx}}$ high 27/	$t_{DATRDGH}$	See figure 4 18/	9, 10, 11	All	0	7	ns
$\overline{\text{WR}}$ low before $\overline{\text{DMAGx}}$ low	t_{DGWRL}		9, 10, 11	All	0	2	
$\overline{\text{DMAGx}}$ low before $\overline{\text{WR}}$ high	t_{DGWRH}		9, 10, 11	All	10+5DT/8+W		
$\overline{\text{WR}}$ high before $\overline{\text{DMAGx}}$ high	t_{DGWRR}		9, 10, 11	All	1+DT/16	3+DT/16	
$\overline{\text{RD}}$ low before $\overline{\text{DMAGx}}$ low	t_{DGRDL}		9, 10, 11	All	-0.5	2	
$\overline{\text{RD}}$ low before $\overline{\text{DMAGx}}$ high	t_{DRDGH}		9, 10, 11	All	11+9DT/16+W		
$\overline{\text{RD}}$ high before $\overline{\text{DMAGx}}$ high	t_{DGRDR}		9, 10, 11	All	0	3	
$\overline{\text{DMAGx}}$ high to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ low	t_{DGWR}		9, 10, 11	All	5+3DT/8+HI		
Address/Select valid to $\overline{\text{DMAGx}}$ high	t_{DADGH}		9, 10, 11	All	17+DT		
Address/Select hold after $\overline{\text{DMAGx}}$ high	t_{DDGHA}		9, 10, 11	All	-0.5		
Data setup before LCLK low (1x)	t_{SLDCL}		9, 10, 11	All	3.5		
Data hold after LCLK low (1x)	t_{HLDCL}		9, 10, 11	All	3		
LCLK period (1x)	t_{LCLKIW}		9, 10, 11	All	t_{CK}		
LCLK width low (1x)	$t_{LCLKRWL}$		9, 10, 11	All	6		
LCLK width high (1x)	$t_{LCLKRWH}$		9, 10, 11	All	5		
LACK high delay after CLKIN high (1x)	t_{DLAHC}		9, 10, 11	All	18+DT/2	28.5+DT/2	
LACK low delay after LCLK high (1x) 41/	t_{DLALC}		9, 10, 11	All	-3	13	
LACK setup before LCLK high (1x)	t_{SLACH}		9, 10, 11	All	19.25		
LACK hold after LCLK high (1x)	t_{HLACH}		9, 10, 11	All	-7		
LCLK delay after CLKIN (1x)	t_{DLCLK}		9, 10, 11	All		16.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data delay after LCLK high (1x)	t_{DLDCH}	See figure 4 18/	9, 10, 11	All		3	ns
Data hold after LCLK high (1x)	t_{HLDCH}		9, 10, 11	All	-3		
LCLK width low (1x)	$t_{LCLKTWL}$		9, 10, 11	All	$(t_{CK}/2)$ -2.0	$(t_{CK}/2)$ +2.25	
LCLK width high (1x)	$t_{LCLKTWH}$		9, 10, 11	All	$(t_{CK}/2)$ -2.25	$(t_{CK}/2)$ +2.0	
LCLK low delay after LACK high (1x)	t_{DLACLK}		9, 10, 11	All	$(t_{CK}/2)$+8.5	$(3t_{CK}/2)$+18	
LACK/LCLK setup before CLKIN low (1x, 2x) 42/	t_{SLCK}		9, 10, 11	All	10		
LACK/LCLK hold before CLKIN low (1x,2x) 42/	t_{HLCK}		9, 10, 11	All	2		
LACK, LDAT, LCLK enable from CLKIN (1x,2x)	t_{ENDLK}		9, 10, 11	All	5+DT/2		
LACK, LDAT, LCLK disable from CLKIN (1x,2x)	t_{TDLK}		9, 10, 11	All		20+DT/2	
Data setup before LCLK low (2x)	t_{SLDCL}		9, 10, 11	All	2.75		
Data hold after LCLK low (2x)	t_{HLDCL}		9, 10, 11	All	2.25		
LCLK period (2x)	t_{LCLKIW}		9, 10, 11	All	$t_{CK}/2$		
LCLK width low (2x)	$t_{LCLKRWL}$		9, 10, 11	All	4.7		
LCLK width high (2x)	$t_{LCLKRWH}$		9, 10, 11	All	4.25		
LACK high delay after CLKIN high (2x)	t_{DLAHC}		9, 10, 11	All	18+DT/2	30.5+DT/2	
LACK low delay after LCLK high (2x) 41/	t_{DLALC}		9, 10, 11	All	6	17.3	
LACK setup before LCLK high (2x)	t_{SLACH}		9, 10, 11	All	19.25		
LACK hold after LCLK high (2x)	t_{HLACH}		9, 10, 11	All	-6.5		
LCLK delay after CLKIN (2x)	t_{DLCLK}		9, 10, 11	All		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data delay after LCLK high (2x)	t_{DLDCH}	See figure 4 18/	9, 10, 11	All		2.85	ns
Data hold after LCLK high (2x)	t_{HLDCH}		9, 10, 11	All	-2.0		
LCLK width low (2x)	$t_{LCLKTWL}$		9, 10, 11	All	$(t_{CK}/4)-1.0$	$(t_{CK}/4)+1.5$	
LCLK width high (2x)	$t_{LCLKTWH}$		9, 10, 11	All	$(t_{CK}/4)-1.5$	$(t_{CK}/4)+1.0$	
LCLK low delay after LACK high (2x)	t_{DLACLK}		9, 10, 11	All	$(t_{CK}/4)+9.0$	$(3t_{CK}/4)+16.5$	
Link Data set-up skew (2x) 43/	t_{SLSK}		9, 10, 11	All		0.45 44/	
Link Data hold skew (2x) 45/	t_{HLSK}		9, 10, 11	All		3.35	
TFS/RFS setup before TCLK/RCLK 46/	t_{SFSE}		9, 10, 11	All	3.5		
TFS/RFS hold after TCLK/RCLK 46/ 47/	t_{HFSE}		9, 10, 11	All	4		
Receive data setup before RCLK 46/	t_{SDRE}		9, 10, 11	All	1.5		
Receive data hold after RCLK 46/	t_{HDRE}		9, 10, 11	All	4		
TCLK/RCLK width	t_{SCLKW}		9, 10, 11	All	9.5		
TCLK/RCLK period	t_{SCLK}		9, 10, 11	All	t_{CK}		
TFS setup before TCLK, RFS setup before RCLK 46/	t_{SFSI}		9, 10, 11	All	8		
TFS hold after TCLK, RFS hold after RCLK 46/ 47/	t_{HFSI}		9, 10, 11	All	1		
Receive data setup before RCLK 46/	t_{SDRI}		9, 10, 11	All	3		
Receive data hold after RCLK 46/	t_{HDRI}		9, 10, 11	All	3		
RFS delay after RCLK (internally generated RFS), TFS delay after TCLK (internally generated TFS) 48/	t_{DFSE}		9, 10, 11	All		13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RFS hold after RCLK (internally generated RFS), TFS hold after TCLK (internally generated TFS) 48/	t_{HOFSE}	See figure 4 18/	9, 10, 11	All	3		ns
Transmit data delay after TCLK 48/	t_{DDTE}		9, 10, 11	All		16	
Transmit data hold after TCLK 48/	t_{HODTE}		9, 10, 11	All	5		
TFS delay after TCLK (internally generated TFS) 48/	t_{DFSI}		9, 10, 11	All		4.5	
TFS hold after TCLK (internally generated TFS) 48/	t_{HOFSI}		9, 10, 11	All	-1.5		
Transmit data delay after TCLK 48/	t_{DDTI}		9, 10, 11	All		7.5	
Transmit data hold after TCLK 48/	t_{HDTI}		9, 10, 11	All	0		
TCLK/RCLK width	t_{SCLKIW}		9, 10, 11	All	$(t_{SCLK}/2)-2$	$(t_{SCLK}/2)+2$	
DT enable delay from ext. TCLK or "late" ext. TFS 48/	t_{DDTEN}		9, 10, 11	All	3.5		
DT disable delay from external TCLK 48/	t_{DDTTE}		9, 10, 11	All		10.5	
DT enable delay from int. TCLK or "late" ext. TFS 48/	t_{DDTIN}		9, 10, 11	All	0		
DT disable delay from internal TCLK 48/	t_{DDTTI}		9, 10, 11	All		3	
TCLK/RCLK delay from CLKIN	t_{DCLK}		9, 10, 11	All		22+3DT/8	
SPORT disable after CLKIN	t_{DPTR}		9, 10, 11	All		17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ Unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TFS setup before CLKIN 49/	t_{STFSCK}	See figure 4 18/	9, 10, 11	All	5.10		ns
TFS hold after CLKIN 49/	t_{HTFSCK}		9, 10, 11	All	$t_{CK}/2$		
Data delay from late external RFS with MCE = 1, MFD = 0 50/	$t_{DDTLFSE}$		9, 10, 11	All		12.6	
Data enable from lated FS or MCE = 1, MFD = 0 50/	$t_{DDTENFS}$		9, 10, 11	All	3		
Boundary scan instruction code							
TCK period	t_{TCK}	See figure 4 18/	9, 10, 11	All	t_{CK}		ns
TDI, TMS setup before TCK high	t_{STAP}		9, 10, 11	All	5		
TDI, TMS hold after TCK high	t_{HTAP}		9, 10, 11	All	6		
System inputs setup before TCK high 51/	t_{SSYS}		9, 10, 11	All	7		
System inputs hold after TCK high 51/	t_{HSYS}		9, 10, 11	All	18		
$\overline{TRST}$ pulse width	t_{TRSTW}		9, 10, 11	All	$4t_{CK}$		
TDO delay from TCK low	t_{DTDO}		9, 10, 11	All		13	
System outputs delay after TCK low 52/	t_{DSYS}		9, 10, 11	All		18.5	

DT = t_{CK} - 25ns
W = (number of wait states specified in WAIT register) x t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (If an address hold cycle occurs as specified in WAIT register; otherwise H = 0).
I = t_{CK} (If a bus idle cycle occurs as specified in WAIT register, otherwise I = 0).

1/ Unless otherwise specified, all testing to be performed using worst-case conditions.

2/ Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ2-0}$, $FLAG_{3-0}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6-1}$, ID_{2-0}, RPBA, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI, TCK.

3/ Applies to input pins: CLKIN, $\overline{RESET}$, TCK, $\overline{TRST}$.

TABLE I. Electrical performance characteristics - Continued.

4/ Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6-1}$, $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

5/ Although specified for TTL outputs, all device outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc loads.

6/ Applies to input pins: $\overline{SBTS}$, $\overline{IRQ2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

7/ Applies to input pins with internal pullups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

8/ Applies to tristatable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, BRG_{6-1}, TFS_x, RFS_x, TDO, $\overline{EMU}$ (Note that ACK is pulled up internally with 2 KΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another DSP is not requesting bus mastership).

9/ Applies to tristatable pins with internal pullups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

10/ Applies to $\overline{CPA}$ pin.

11/ Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 KΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another DSP is not requesting bus mastership).

12/ Applies to ACK pin when keeper latch enabled.

13/ Applies to tristatable pins with internal pull downs: $LxDAT_{3-0}$, LxCLK, LxACK.

14/ Applies to VDD pins. Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers: $P_{TOTAL} = P_{INT} + P_{EXT}$. Internal power dissipation is $P_{INT} = I_{DDIN} \times V_{DD}$. The external component of total power dissipation is caused by the switching of output pins, and depends on: the number of pins that switch each cycle (O), the maximum frequency at which they can switch (f), the load capacitance per pin (C), the output voltage swing (V_{DD}): $P_{EXT} = O \times C \times V_{DD}^2 \times f$. Address and data pins can switch at $f = 1/(2t_{CK})$. $\overline{WR}$ can switch at $1/t_{CK}$. $\overline{MS}x$ pins switch at $1/(2t_{CK})$.

15/ Conditions of operation: Executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from each internal memory.

16/ Applies to VDD pins. Idle denotes device state during execution of IDLE instruction.

17/ Applies to all signal pins.

18/ Guaranteed but not tested. Timing characteristics are guaranteed by characterization at -55°C, 25°C, and 125°C of each performance parameter over the range of supply voltage (V_{DD}). Characterization is performed using devices whose transistor characteristics are deliberately skewed in processing to simulate maximum expected performance variation due to process variation. Selected timing characteristics are routinely tested in production devices.

19/ Applies after the powerup sequence is complete. At powerup, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while $\overline{RESET}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

20/ Only required if multiple device must come out of reset synchronous to CLKIN with program counter (PC) equal (i.e., for a SIMD system). Not required for multiple devices communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

21/ Only required for $\overline{IRQx}$ recognition in the following cycle.

22/ Applies only if t_{SIR} and t_{HIR} requirements are not met.

23/ Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

24/ Data Delay/Setup: User must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.

25/ The falling edge of $\overline{MS}x, \overline{SW}, \overline{BMS}$ is referenced.

26/ Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}.

27/ To determine the data output hold time in a particular system, first calculate $t_{DECAY} = C_{LOAD} \times \Delta V / I_{LOAD}$. Choose ΔV to be the difference between the microcontroller's output voltage and the input threshold of the device requiring the data hold time. A typical ΔV will be 0.4 V. C_{LOAD} is the total bus capacitance (per data line), and I_{LOAD} is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time.

28/ ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

TABLE I. Electrical performance characteristics - Continued.

29/ t_{SRWLI}(min) = 9.5+5DT/16 when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI}(min) = 4+DT/8.

30/ t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10+DT/8 and less than 19+3DT/4. If the address and $\overline{SW}$ inputs have setup times greater than 19+3DT/4, then ACK is valid 14+DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

31/ For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted.

32/ Only required for recognition in the current cycle.

33/ $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

34/ (o/d) = open drain, (a/d) = active drive.

35/ Not required if $\overline{RD}$ and Address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low.

36/ Strobes = $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, PAGE, $\overline{DMAG}$.

37/ In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

38/ Memory interface = address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{SW}$, $\overline{HBG}$, PAGE, $\overline{DMAGx}$, $\overline{BMS}$ (in EPROM boot mode).

39/ $t_{SDATDGL}$ is the setup requirement if $\overline{DMARx}$ is not being used to hold off completion of a write. Otherwise, if $\overline{DMARx}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMARx}$ is brought high.

40/ $t_{VDATDGH}$ is valid if $\overline{DMARx}$ is not being used to hold off completion of a read. If $\overline{DMARx}$ is used to prolong the read, then $t_{VDATDGH}$ = 8+9DT/16+(n x t_{CK}) when n equals the number of extra cycles that the access is prolonged.

41/ LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receiver's link buffer is not about to fill.

42/ Only required for interrupt recognition in the current cycle.

43/ t_{SLSK} is the maximum delay that can be introduced in the transmission path of LDATA relative to LCLK: t_{SLSK} = ($t_{LCLKTWH}$ - t_{DLDCH})min - t_{SLDCL}max.

44/ If link port 2 is transmitter, t_{SLSK} = 0.28 ns. Because of this small margin, extreme care must be taken in system design. If adequate setup time cannot be assured, link port operation should be limited to 1X, or system CLKIN frequency should be reduced to increase the setup margin at 2X.

45/ t_{HLSK} is the maximum delay that can be introduced in the transmission path of LCLK relative to LDATA: t_{HLSK} = ($t_{LCLKTWL}$- t_{HLDCH})min - t_{HLDCL}max.

46/ Referenced to sample edge.

47/ RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

48/ Referenced to drive edge.

49/ Applied only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems. See user's manual.

50/ MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

51/ System inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6-1}$, ID_{2-0}, RPBA, $\overline{IRQ2-0}$, $FLAG_{3-0}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, CLKIN, $\overline{RESET}$.

52/ System outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6-1}$, $\overline{CPA}$, $FLAG_{3-0}$, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

Case X - Cavity down

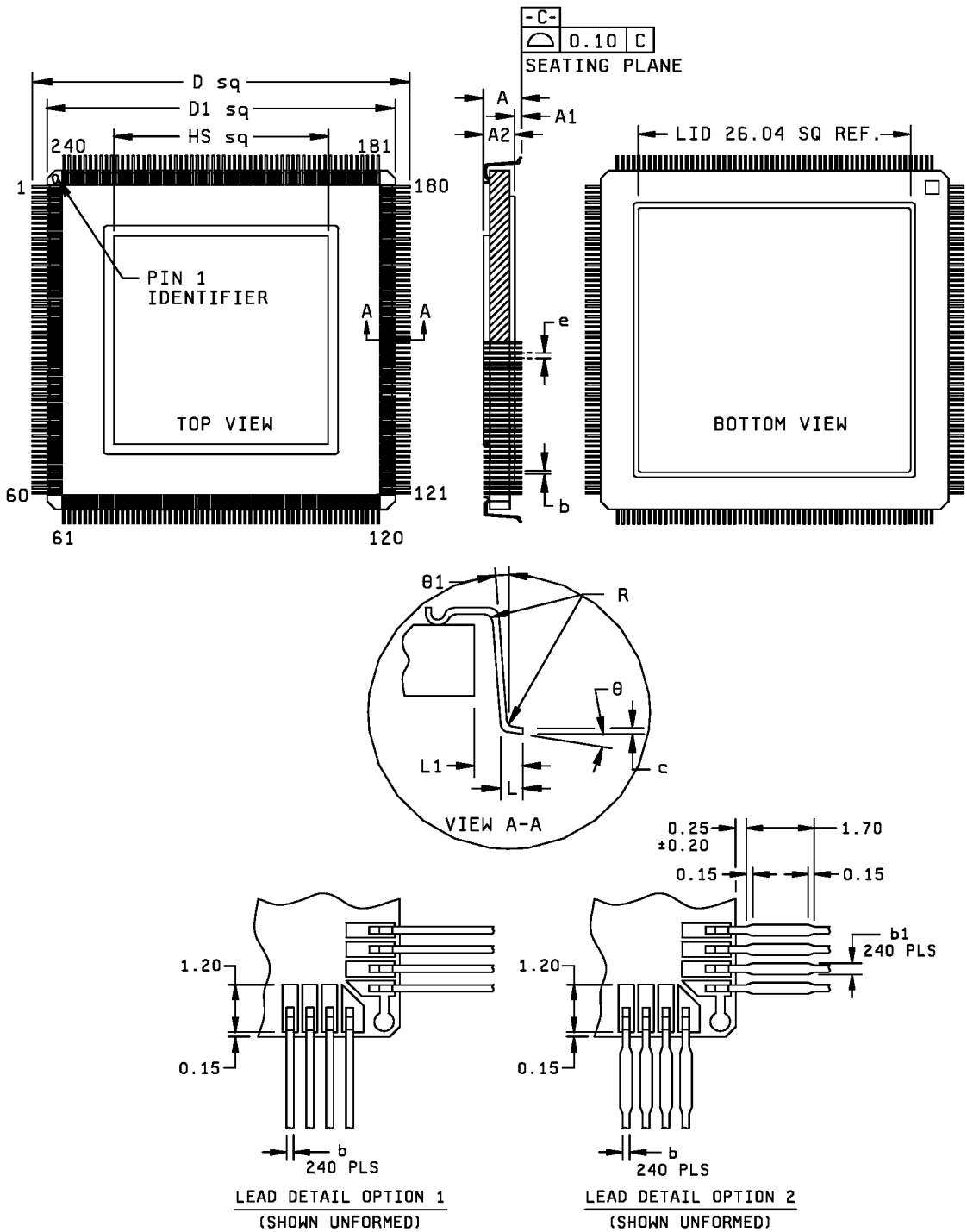


FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96745
		REVISION LEVEL	SHEET 21

Case X - Cavity down

Symbol	Dimensions (Millimeters)	
	Min	Max
A	2.95	4.30
A1	0.20	0.60
A2	2.75	3.70
b	0.17	0.23
b1	0.25	0.35
c	0.13	0.18
D	35.65	36.60
D1	32.00 REF	
e	0.50 BSC	
HS	19.00 REF	
L	0.60	0.90
L1	2.06 REF	
θ	-3°	7°
θ1	0°	

NOTES:
1. The lead style is at vendor's option.
2. The lead option does not affect device footprint.

FIGURE 1. Case outlines - Continued.

Case Y - Cavity up

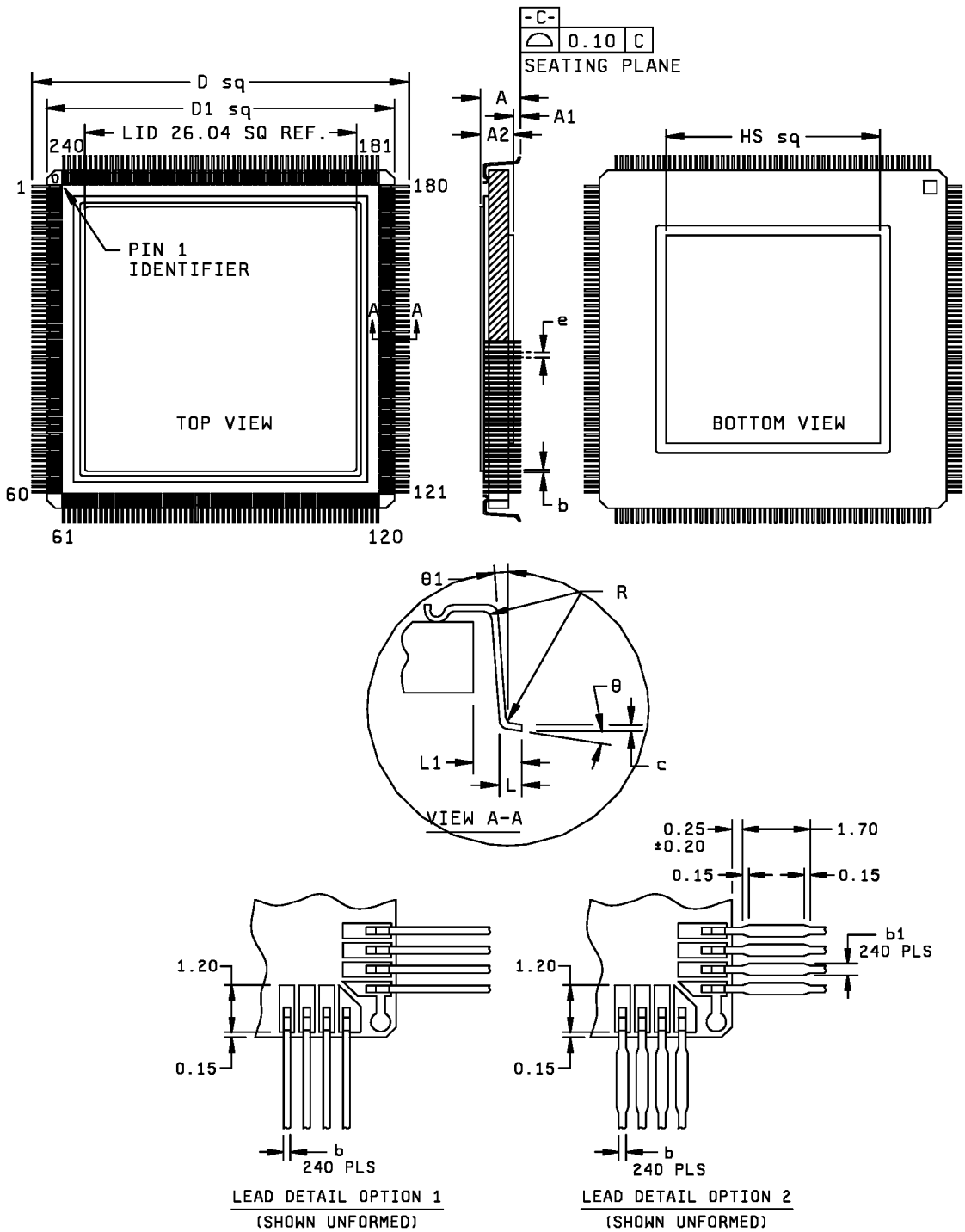


FIGURE 1. Case outlines - Continued.

Case Y - Cavity up

Symbol	Dimensions (Millimeters)	
	Min	Max
A	2.85	4.20
A1	0.10	0.50
A2	2.75	3.70
b	0.17	0.23
b1	0.25	0.35
c	0.13	0.18
D	35.65	36.60
D1	32.00 REF	
e	0.50 BSC	
HS	19.00 REF	
L	0.60	0.90
L1	2.06REF	
θ	-3°	7°
θ1	0°	

NOTES:
1. The lead style is at vendor's option.
2. The lead option does not affect device footprint.

FIGURE 1. Case outlines - Continued.

Case T - Cavity down

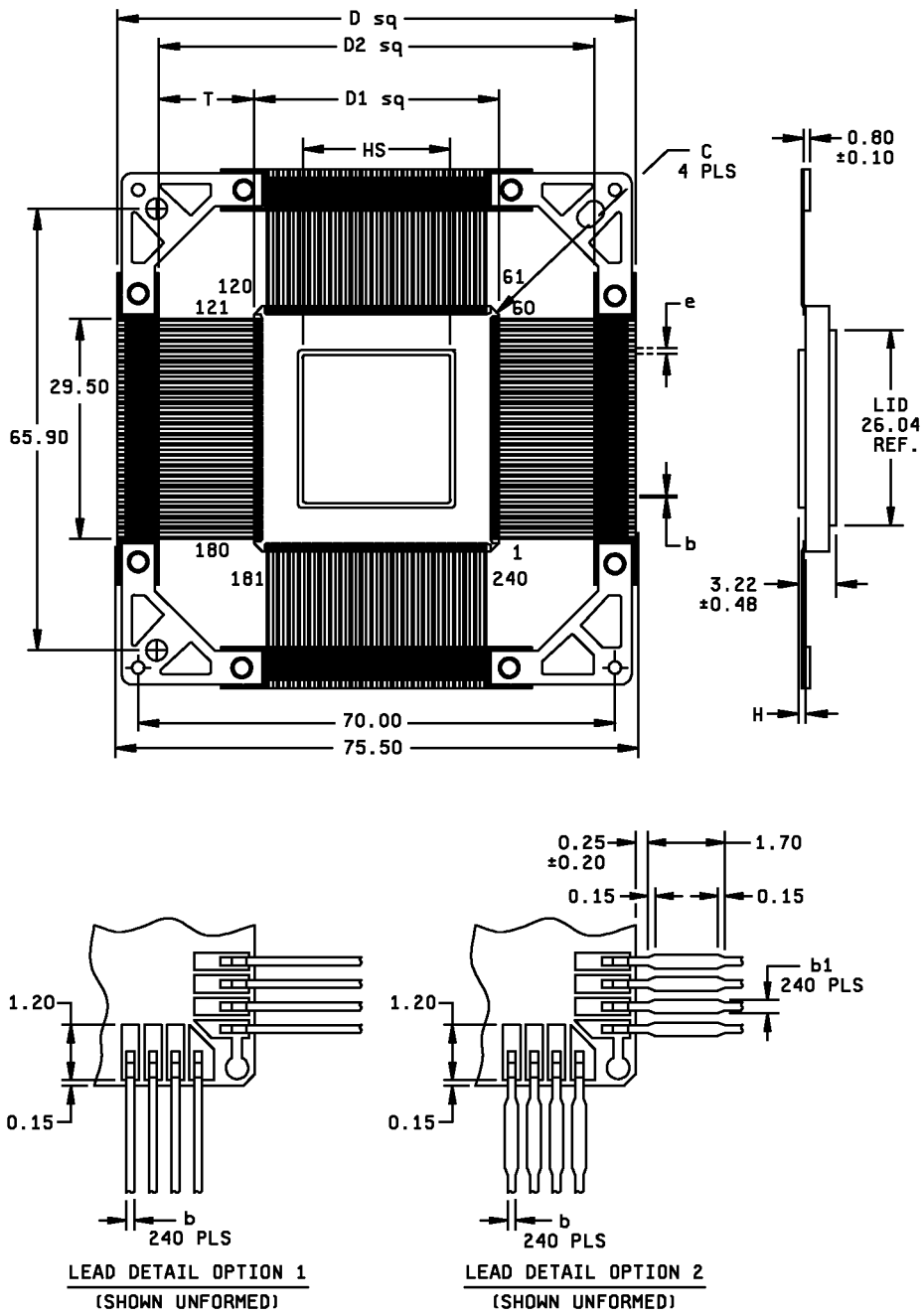


FIGURE 1. Case outlines - Continued.

Case T - Cavity down

Symbol	Dimensions (Millimeters)	
	Min	Max
b	0.17	0.23
b1	0.25	0.35
C	0.30 REF	
D	75.00 REF	
D1	32.00 REF	
D2	65.00 REF	
e	0.50 BSC	
H	0.50 REF	
HS	19.00 REF	
T	16.50 REF	

NOTES:
1. The lead style is at vendor's option.
2. The lead option does not affect device footprint.

FIGURE 1. Case outlines - Continued.

Case U - Cavity up

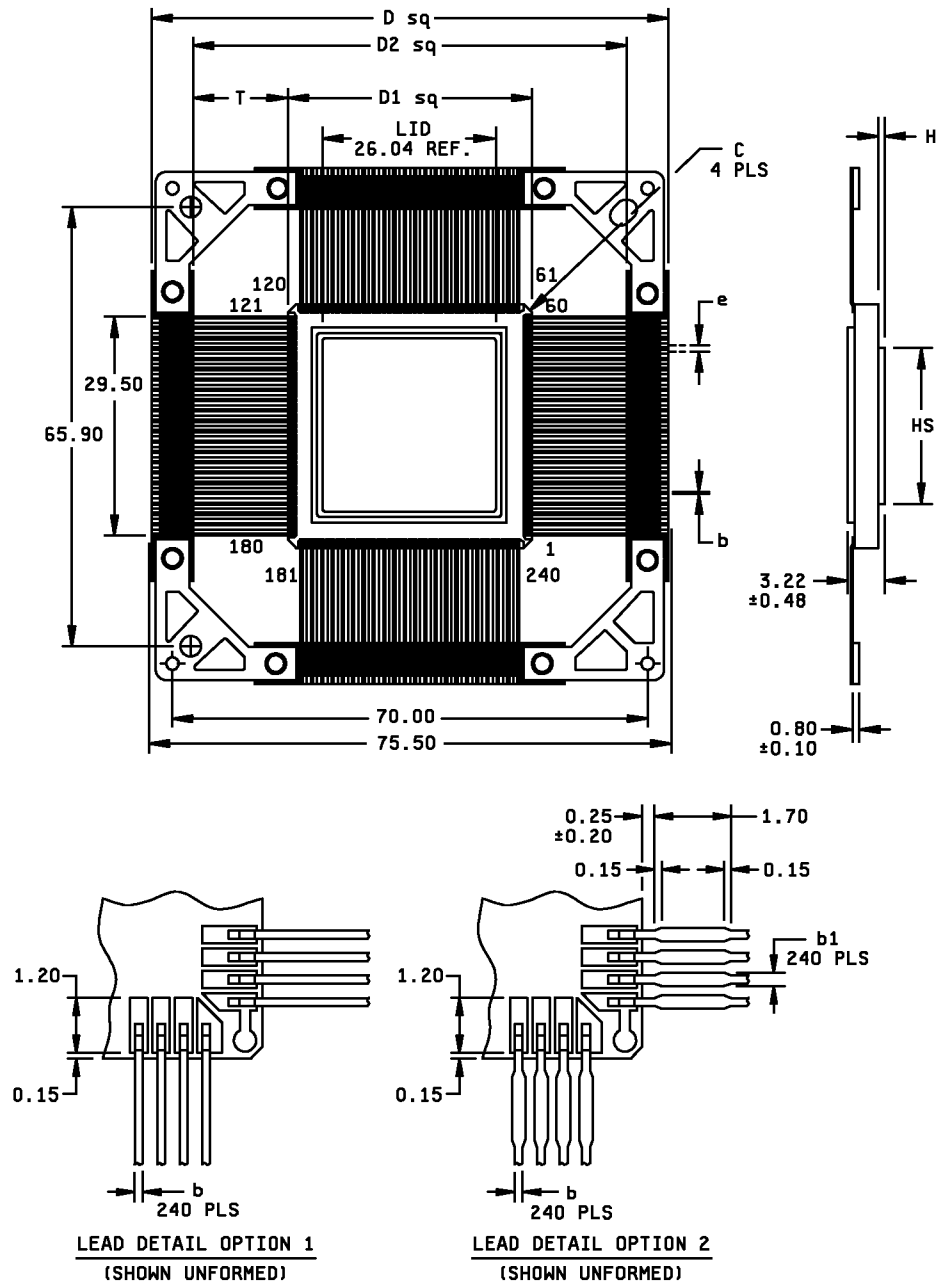


FIGURE 1. Case outlines - Continued.

Case U - Cavity up

Symbol	Dimensions (Millimeters)	
	Min	Max
b	0.17	0.23
b1	0.25	0.35
C	0.30 REF	
D	75.00 REF	
D1	32.00 REF	
D2	65.00 REF	
e	0.50 BSC	
H	0.50 REF	
HS	19.00 REF	
T	16.50 REF	

NOTES:
1. The lead style is at vendor's option.
2. The lead option does not affect device footprint.

FIGURE 1. Case outlines - Continued.

Device type	01, 02						
Case outline	X, T						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TDI	31	VDD	61	GND	91	$\overline{\text{HBG}}$
2	$\overline{\text{TRST}}$	32	ADDR14	62	VDD	92	$\overline{\text{CS}}$
3	VDD	33	ADDR15	63	VDD	93	$\overline{\text{RD}}$
4	TDO	34	GND	64	ADDR29	94	$\overline{\text{WR}}$
5	TIMEXP	35	ADDR16	65	ADDR30	95	GND
6	$\overline{\text{EMU}}$	36	ADDR17	66	ADDR31	96	VDD
7	ICSA	37	ADDR18	67	GND	97	GND
8	FLAG3	38	VDD	68	$\overline{\text{SBTS}}$	98	CLKIN
9	FLAG2	39	VDD	69	$\overline{\text{DMAR2}}$	99	ACK
10	FLAG1	40	ADDR19	70	$\overline{\text{DMAR1}}$	100	$\overline{\text{DMAG2}}$
11	FLAG0	41	ADDR20	71	$\overline{\text{HBR}}$	101	$\overline{\text{DMAG1}}$
12	GND	42	ADDR21	72	DT1	102	PAGE
13	ADDR0	43	GND	73	TCLK1	103	VDD
14	ADDR1	44	ADDR22	74	TFS1	104	$\overline{\text{BR6}}$
15	VDD	45	ADDR23	75	DR1	105	$\overline{\text{BR5}}$
16	ADDR2	46	ADDR24	76	RCLK1	106	$\overline{\text{BR4}}$
17	ADDR3	47	VDD	77	RFS1	107	$\overline{\text{BR3}}$
18	ADDR4	48	GND	78	GND	108	$\overline{\text{BR2}}$
19	GND	49	VDD	79	$\overline{\text{CPA}}$	109	$\overline{\text{BR1}}$
20	ADDR5	50	ADDR25	80	DT0	110	GND
21	ADDR6	51	ADDR26	81	TCLK0	111	VDD
22	ADDR7	52	ADDR27	82	TFS0	112	GND
23	VDD	53	GND	83	DR0	113	DATA47
24	ADDR8	54	$\overline{\text{MS3}}$	84	RCLK0	114	DATA46
25	ADDR9	55	$\overline{\text{MS2}}$	85	RFS0	115	DATA45
26	ADDR10	56	$\overline{\text{MS1}}$	86	VDD	116	VDD
27	GND	57	$\overline{\text{MS0}}$	87	VDD	117	DATA44
28	ADDR11	58	$\overline{\text{SW}}$	88	GND	118	DATA43
29	ADDR12	59	$\overline{\text{BMS}}$	89	ADRCLK	119	DATA42
30	ADDR13	60	ADDR28	90	REDY	120	GND

FIGURE 2. Terminal connections.

Device type	01, 02						
Case outline	X, T						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
121	DATA41	151	DATA21	181	GND	211	L3ACK
122	DATA40	152	VDD	182	L0DAT3	212	GND
123	DATA39	153	DATA20	183	L0DAT2	213	L4DAT3
124	VDD	154	DATA19	184	L0DAT1	214	L4DAT2
125	DATA38	155	DATA18	185	L0DAT0	215	L4DAT1
126	DATA37	156	GND	186	L0CLK	216	L4DAT0
127	DATA36	157	DATA17	187	L0ACK	217	L4CLK
128	GND	158	DATA16	188	VDD	218	L4ACK
129	NC	159	DATA15	189	L1DAT3	219	VDD
130	DATA35	160	VDD	190	L1DAT2	220	GND
131	DATA34	161	DATA14	191	L1DAT1	221	VDD
132	DATA33	162	DATA13	192	L1DAT0	222	L5DAT3
133	VDD	163	DATA12	193	L1CLK	223	L5DAT2
134	VDD	164	GND	194	L1ACK	224	L5DAT1
135	GND	165	DATA11	195	GND	225	L5DAT0
136	DATA32	166	DATA10	196	GND	226	L5CLK
137	DATA31	167	DATA9	197	VDD	227	L5ACK
138	DATA30	168	VDD	198	L2DAT3	228	GND
139	GND	169	DATA8	199	L2DAT2	229	ID2
140	DATA29	170	DATA7	200	L2DAT1	230	ID1
141	DATA28	171	DATA6	201	L2DAT0	231	ID0
142	DATA27	172	GND	202	L2CLK	232	LBOOT
143	VDD	173	DATA5	203	L2ACK	233	RPBA
144	VDD	174	DATA4	204	NC	234	$\overline{\text{RESET}}$
145	DATA26	175	DATA3	205	VDD	235	EBOOT
146	DATA25	176	VDD	206	L3DAT3	236	$\overline{\text{IRQ2}}$
147	DATA24	177	DATA2	207	L3DAT2	237	$\overline{\text{IRQ1}}$
148	GND	178	DATA1	208	L3DAT1	238	$\overline{\text{IRQ0}}$
149	DATA23	179	DATA0	209	L3DAT0	239	TCK
150	DATA22	180	GND	210	L3CLK	240	TMS

FIGURE 2. Terminal connections - Continued.

Device type	01, 02						
Case outline	Y, U						
Terminal Number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	31	DATA22	61	GND	91	REDY
2	DATA0	32	DATA23	62	DATA42	92	ADRCLK
3	DATA1	33	GND	63	DATA43	93	GND
4	DATA2	34	DATA24	64	DATA44	94	VDD
5	VDD	35	DATA25	65	VDD	95	VDD
6	DATA3	36	DATA26	66	DATA45	96	RFS0
7	DATA4	37	VDD	67	DATA46	97	RCLK0
8	DATA5	38	VDD	68	DATA47	98	DR0
9	GND	39	DATA27	69	GND	99	TFS0
10	DATA6	40	DATA28	70	VDD	100	TCLK0
11	DATA7	41	DATA29	71	GND	101	DT0
12	DATA8	42	GND	72	$\overline{BR1}$	102	$\overline{CPA}$
13	VDD	43	DATA30	73	$\overline{BR2}$	103	GND
14	DATA9	44	DATA31	74	$\overline{BR3}$	104	RFS1
15	DATA10	45	DATA32	75	$\overline{BR4}$	105	RCLK1
16	DATA11	46	GND	76	$\overline{BR5}$	106	DR1
17	GND	47	VDD	77	$\overline{BR6}$	107	TFS1
18	DATA12	48	VDD	78	VDD	108	TCLK1
19	DATA13	49	DATA33	79	PAGE	109	DT1
20	DATA14	50	DATA34	80	$\overline{DMAG1}$	110	$\overline{HBR}$
21	VDD	51	DATA35	81	$\overline{DMAG2}$	111	$\overline{DMAR1}$
22	DATA15	52	NC	82	ACK	112	$\overline{DMAR2}$
23	DATA16	53	GND	83	CLKIN	113	$\overline{SBTS}$
24	DATA17	54	DATA36	84	GND	114	GND
25	GND	55	DATA37	85	VDD	115	ADDR31
26	DATA18	56	DATA38	86	GND	116	ADDR30
27	DATA19	57	VDD	87	$\overline{WR}$	117	ADDR29
28	DATA20	58	DATA39	88	$\overline{RD}$	118	VDD
29	VDD	59	DATA40	89	$\overline{CS}$	119	VDD
30	DATA21	60	DATA41	90	$\overline{HBG}$	120	GND

FIGURE 2. Terminal connections - Continued.

Device type	01, 02						
Case outline	Y, U						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
121	ADDR28	151	ADDR13	181	TMS	211	L3CLK
122	$\overline{\text{BMS}}$	152	ADDR12	182	TCK	212	L3DAT0
123	$\overline{\text{SW}}$	153	ADDR11	183	$\overline{\text{IRQ0}}$	213	L3DAT1
124	$\overline{\text{MS0}}$	154	GND	184	$\overline{\text{IRQ1}}$	214	L3DAT2
125	$\overline{\text{MS1}}$	155	ADDR10	185	$\overline{\text{IRQ2}}$	215	L3DAT3
126	$\overline{\text{MS2}}$	156	ADDR9	186	EBOOT	216	VDD
127	$\overline{\text{MS3}}$	157	ADDR8	187	$\overline{\text{RESET}}$	217	NC
128	GND	158	VDD	188	RPBA	218	L2ACK
129	ADDR27	159	ADDR7	189	LBOOT	219	L2CLK
130	ADDR26	160	ADDR6	190	ID0	220	L2DAT0
131	ADDR25	161	ADDR5	191	ID1	221	L2DAT1
132	VDD	162	GND	192	ID2	222	L2DAT2
133	GND	163	ADDR4	193	GND	223	L2DAT3
134	VDD	164	ADDR3	194	L5ACK	224	VDD
135	ADDR24	165	ADDR2	195	L5CLK	225	GND
136	ADDR23	166	VDD	196	L5DAT0	226	GND
137	ADDR22	167	ADDR1	197	L5DAT1	227	L1ACK
138	GND	168	ADDR0	198	L5DAT2	228	L1CLK
139	ADDR21	169	GND	199	L5DAT3	229	L1DAT0
140	ADDR20	170	FLAG0	200	VDD	230	L1DAT1
141	ADDR19	171	FLAG1	201	GND	231	L1DAT2
142	VDD	172	FLAG2	202	VDD	232	L1DAT3
143	VDD	173	FLAG3	203	L4ACK	233	VDD
144	ADDR18	174	ICSA	204	L4CLK	234	L0ACK
145	ADDR17	175	$\overline{\text{EMU}}$	205	L4DAT0	235	L0CLK
146	ADDR16	176	TIMEXP	206	L4DAT1	236	L0DAT0
147	GND	177	TDO	207	L4DAT2	237	L0DAT1
148	ADDR15	178	VDD	208	L4DAT3	238	L0DAT2
149	ADDR14	179	$\overline{\text{TRST}}$	209	GND	239	L0DAT3
150	VDD	180	TDI	210	L3ACK	240	GND

FIGURE 2. Terminal connections - Continued.

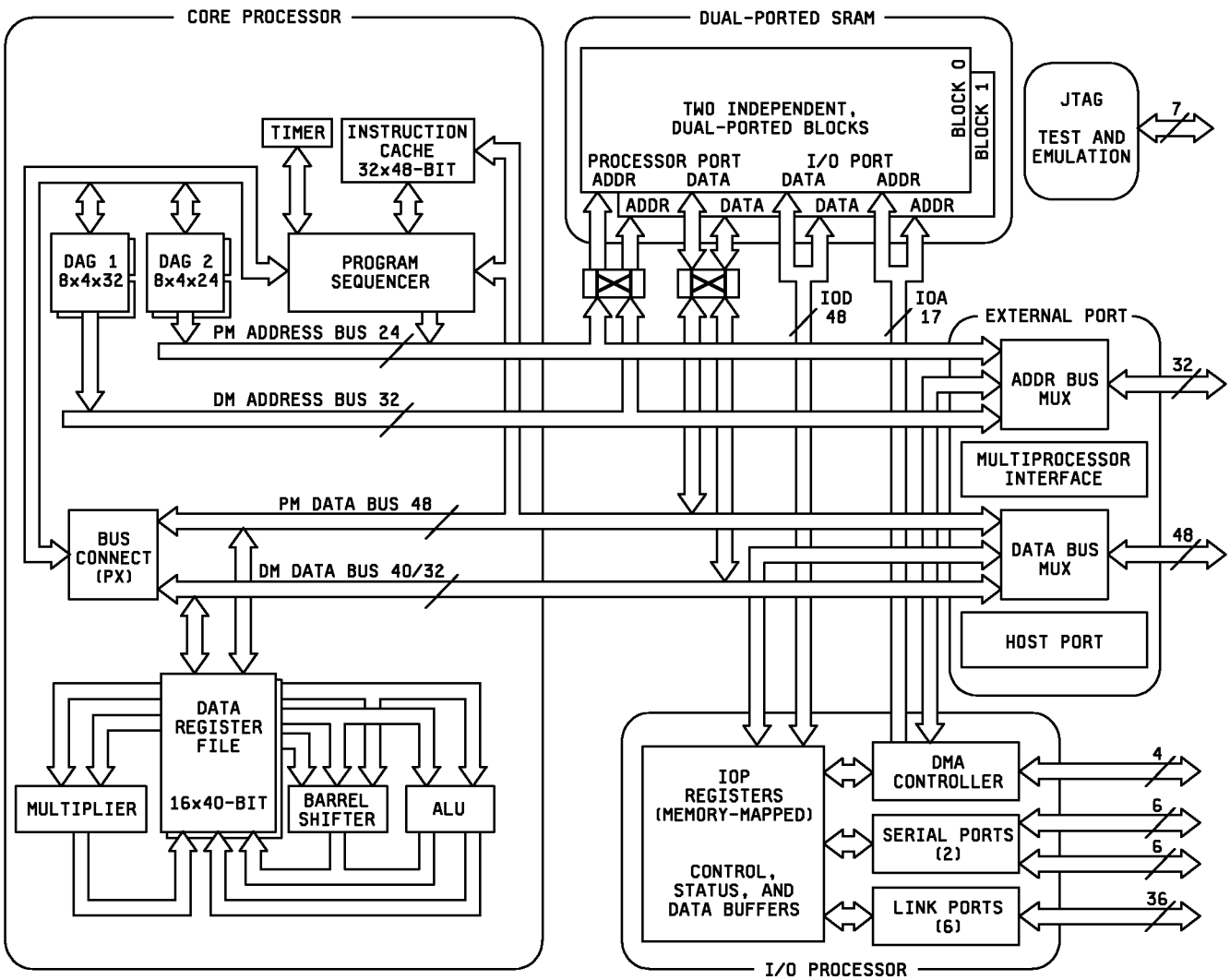
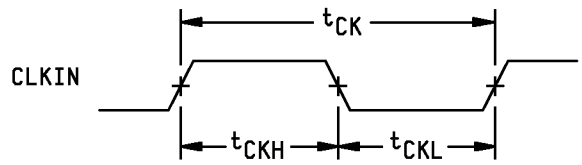


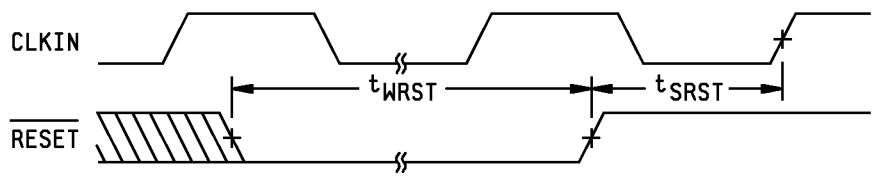
FIGURE 3. Block diagram.

Device types 01, 02	
Instruction name	Instruction code
BYPASS	1xxxx
EXTEST	00000
SAMPLE/PRELOAD	00001
INTEST	00011

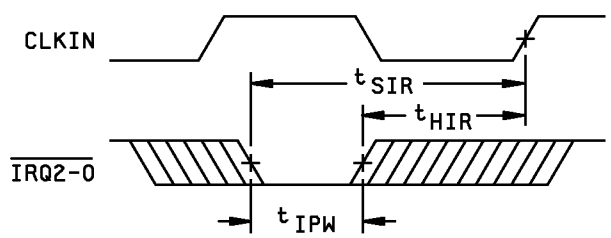
FIGURE 4. Boundary scan instruction codes.



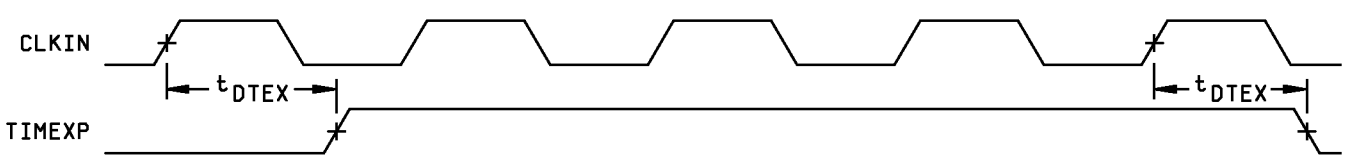
CLOCK INPUT



RESET

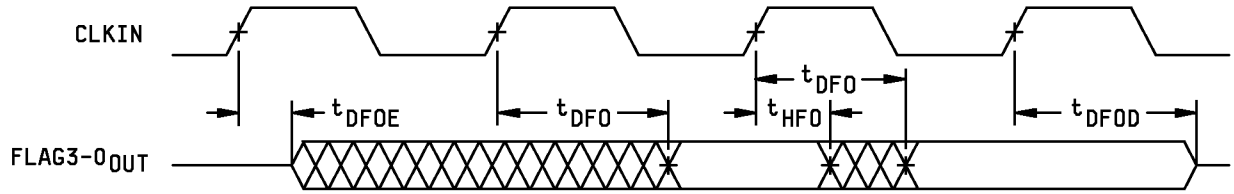


INTERRUPTS

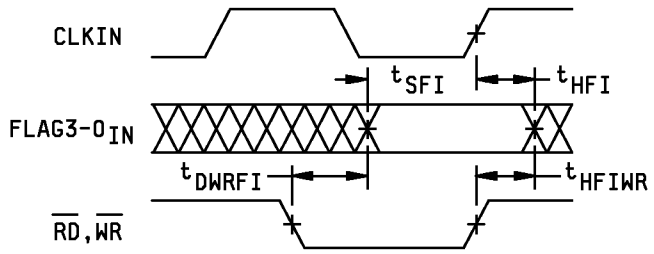


TIMER

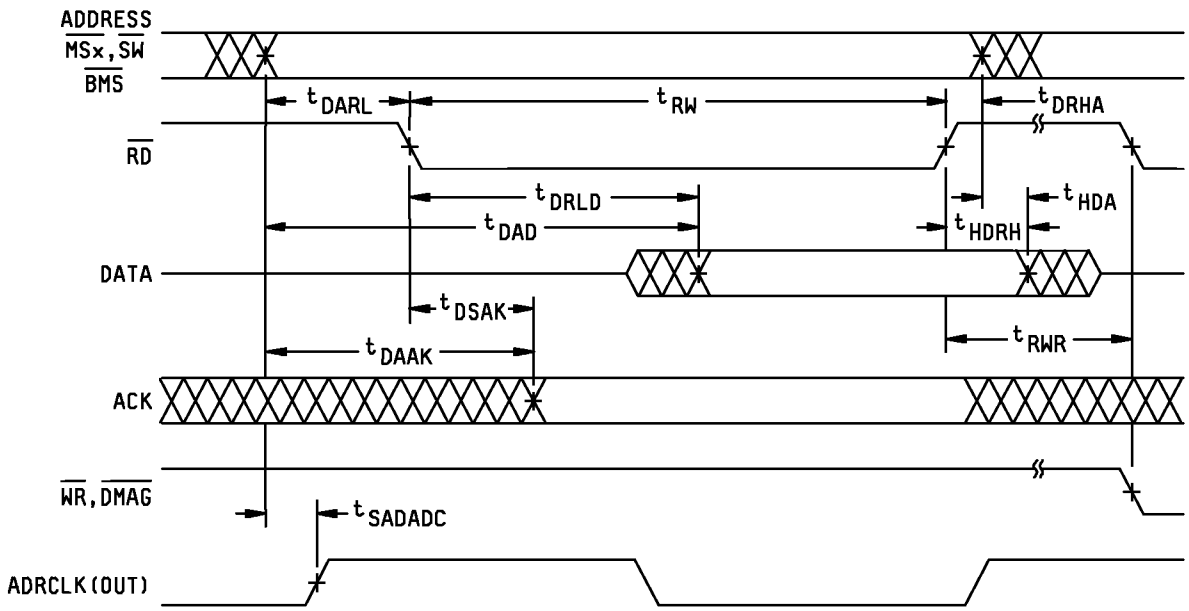
FIGURE 5. Timing waveforms.



FLAG OUTPUT

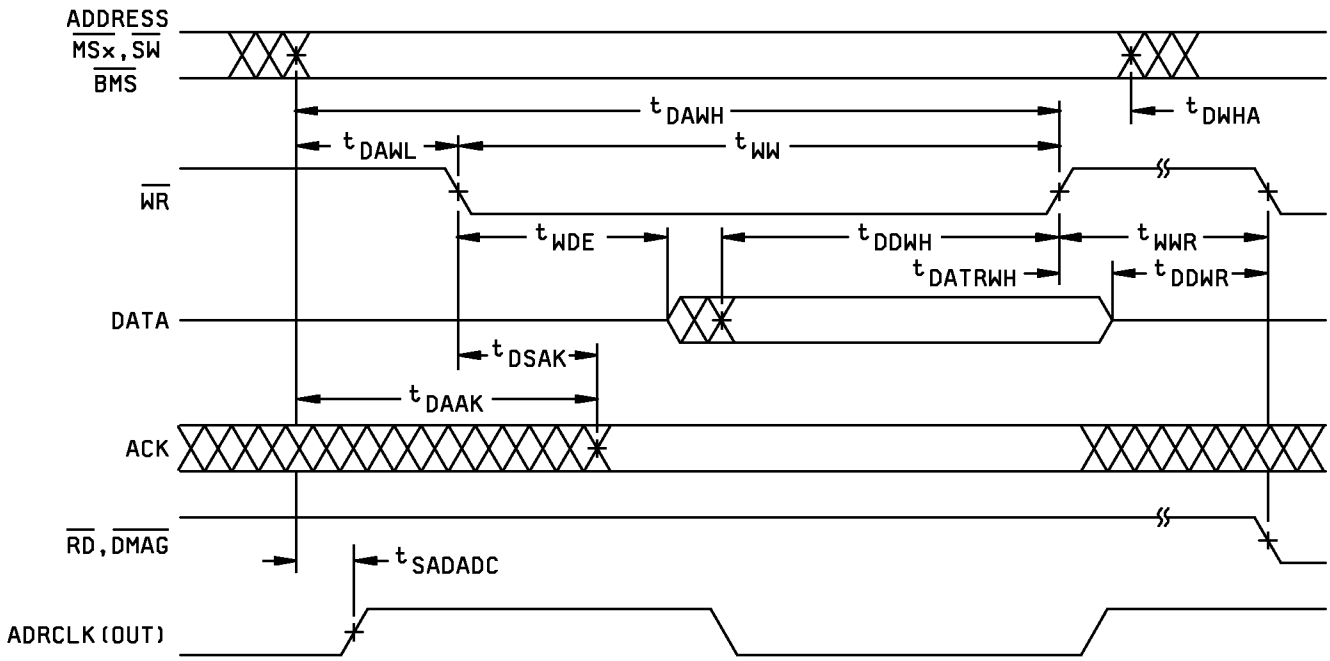


FLAG INPUT



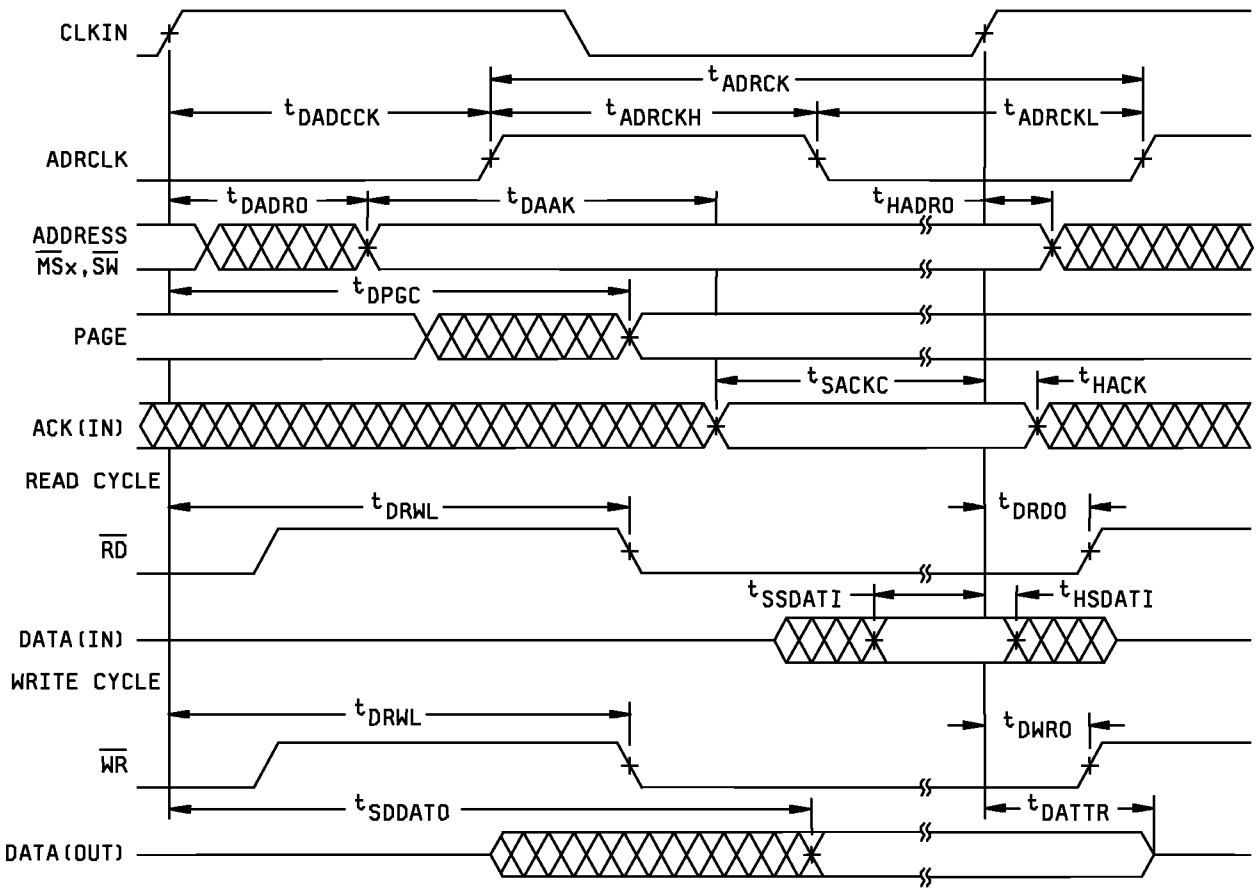
MEMORY READ - BUS MASTER

FIGURE 5. Timing waveforms - Continued.



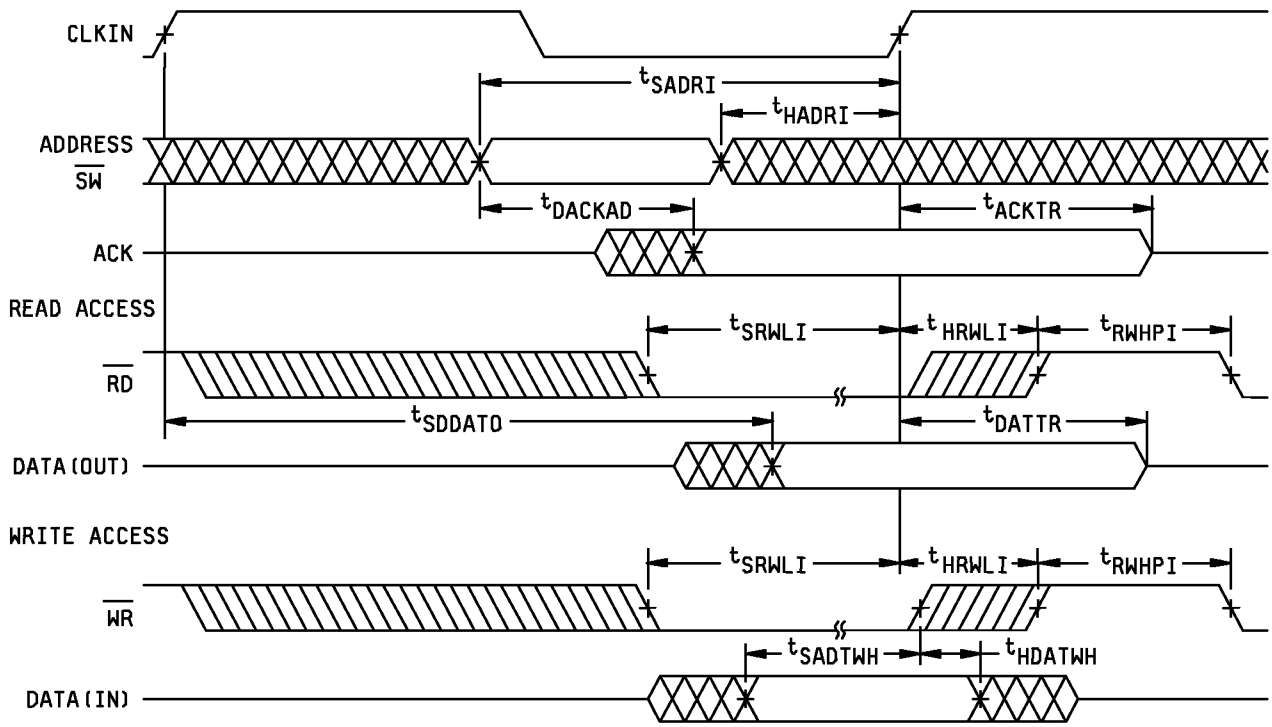
MEMORY WRITE - BUS MASTER

FIGURE 5. Timing waveforms - Continued.



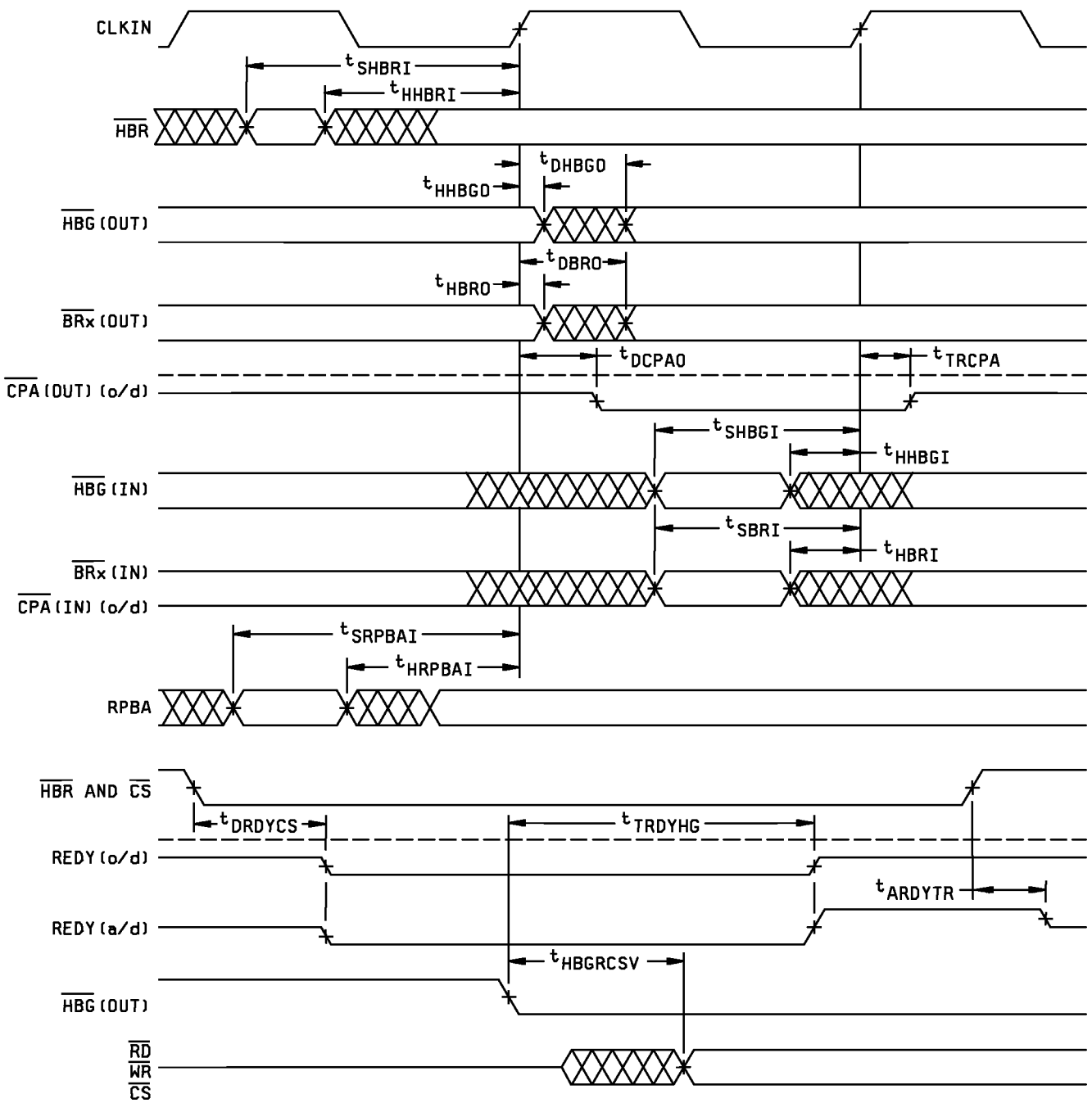
SYNCHRONOUS READ/WRITE - BUS MASTER

FIGURE 5. Timing waveforms - Continued.



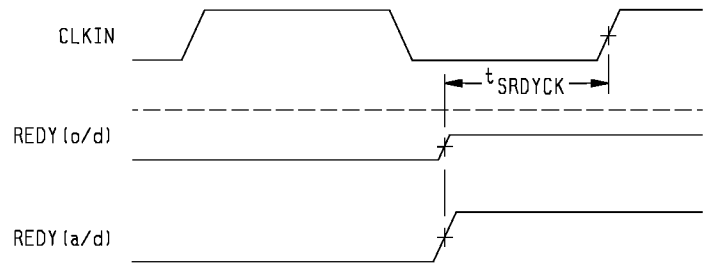
SYNCHRONOUS READ/WRITE - BUS SLAVE

FIGURE 5. Timing waveforms - Continued.

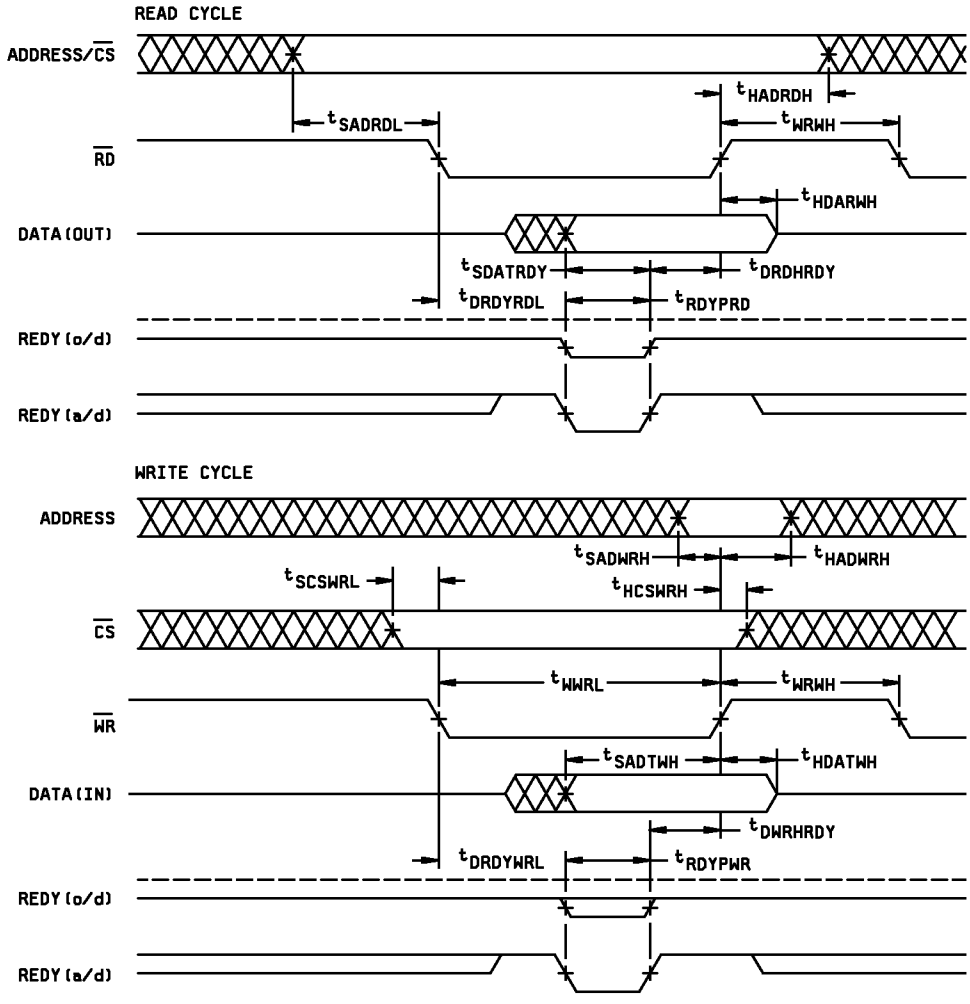


MULTIPROCESSOR BUS REQUEST AND HOST BUS REQUEST

FIGURE 5. Timing waveforms - Continued.

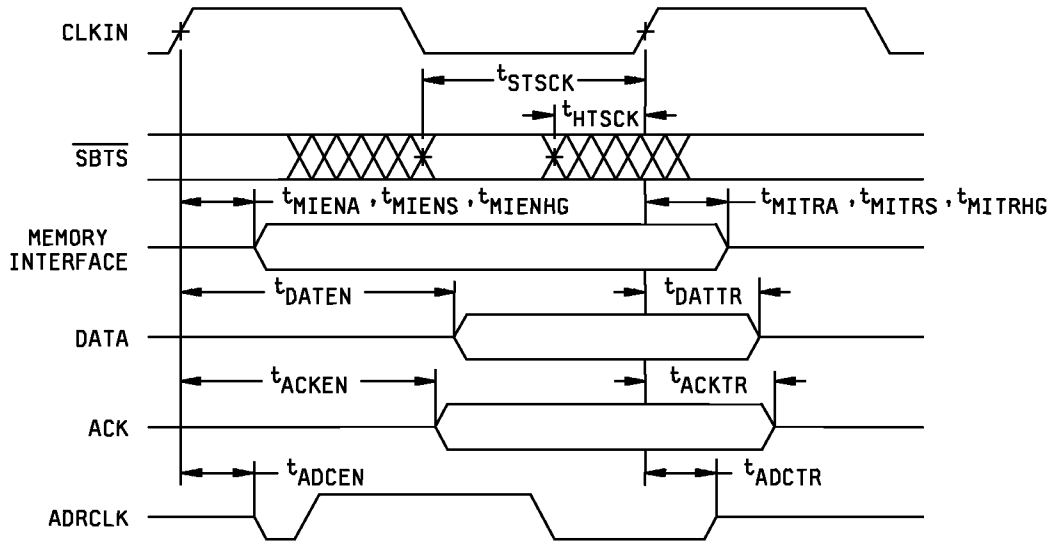


SYNCHRONOUS REDY TIMING

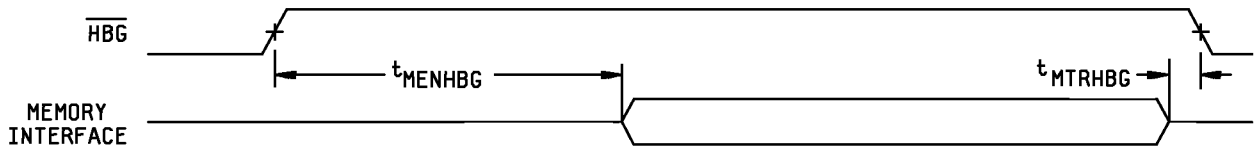


ASYNCHRONOUS READ/WRITE-HOST TO DSP

FIGURE 5. Timing waveforms - Continued.

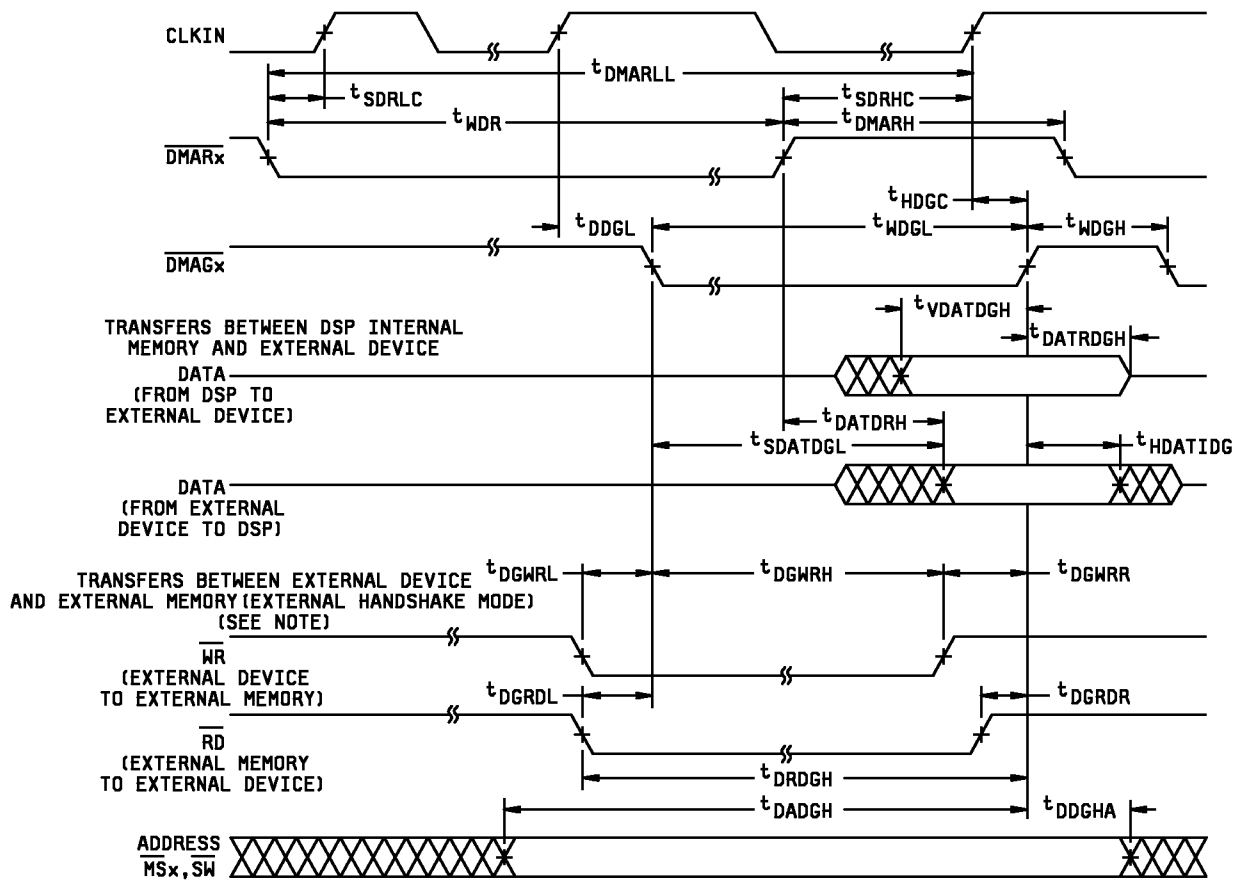


THREE-STATE TIMING (BUS TRANSITION CYCLE, $\overline{SBTS}$ ASSERTION)



THREE-STATE TIMING (HOST TRANSITION CYCLE)

FIGURE 5. Timing waveforms - Continued.



DMA HANDSHAKE TIMING

NOTE: Memory Read - Bus Master, Memory Write - Bus Master, and Synchronous Read/Write - Bus Master timing specifications for $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, $\overline{MS}_{3-0}$ and ACK also apply here.

FIGURE 5. Timing waveforms - Continued.

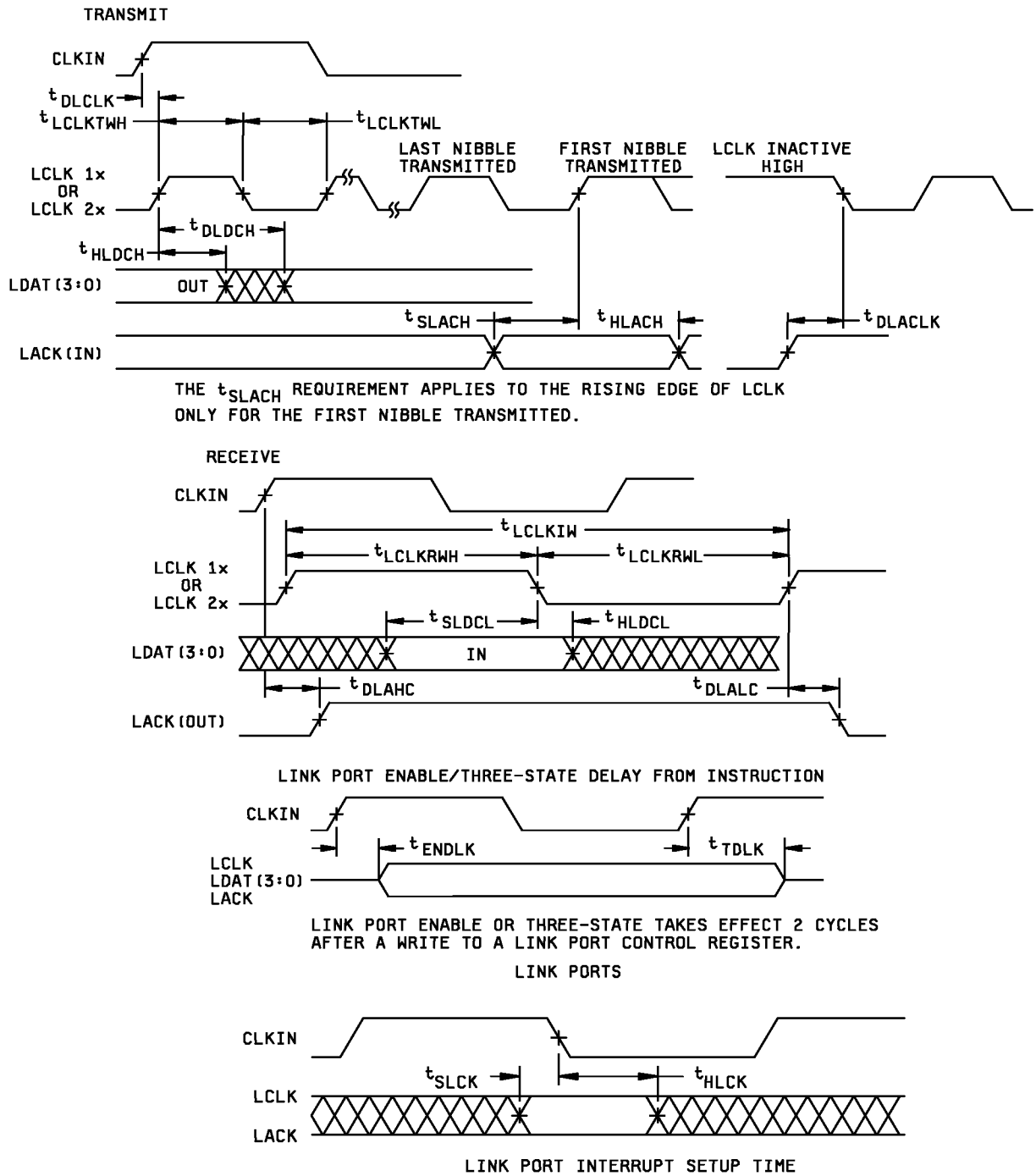


FIGURE 5. Timing waveforms - Continued.

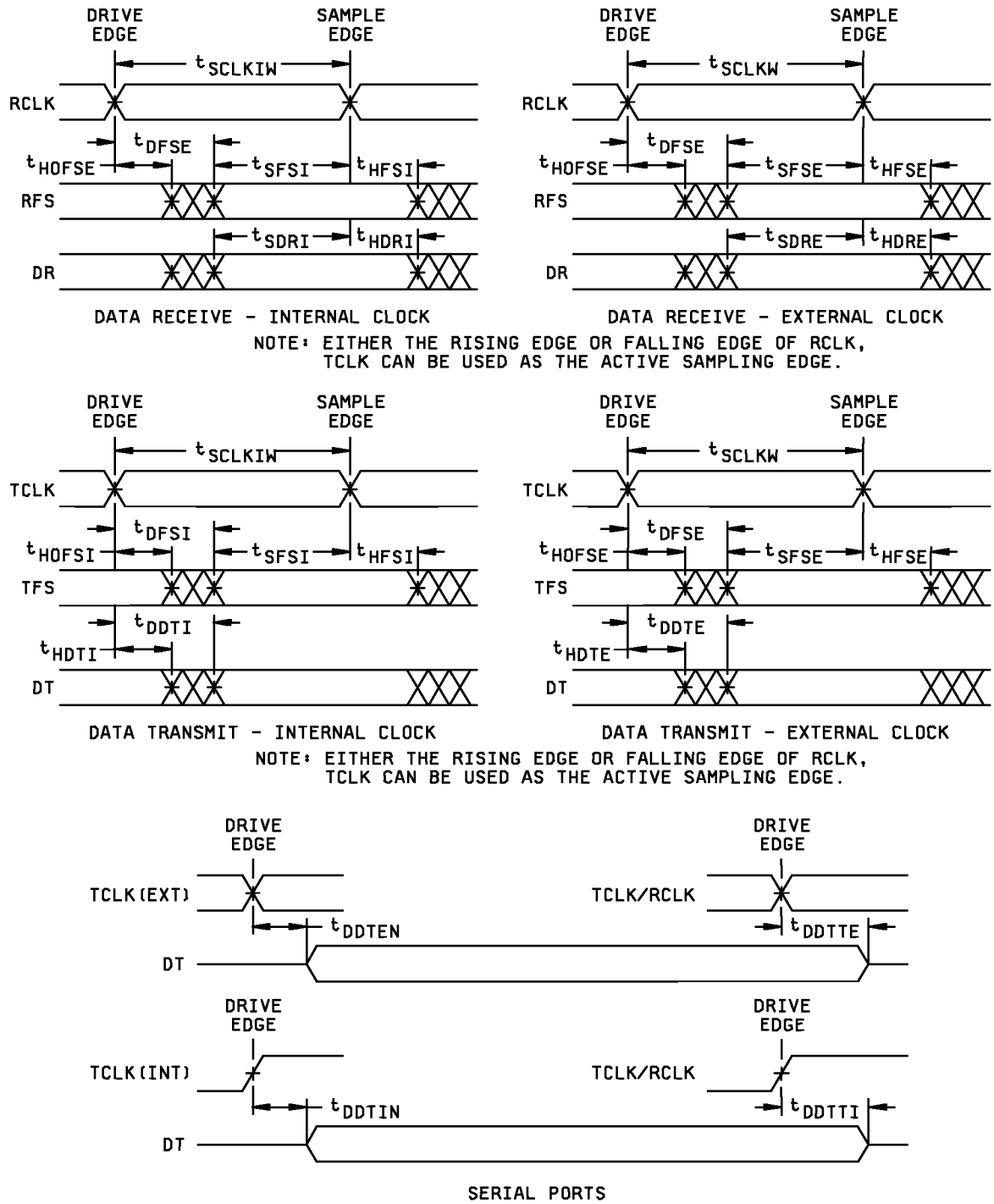
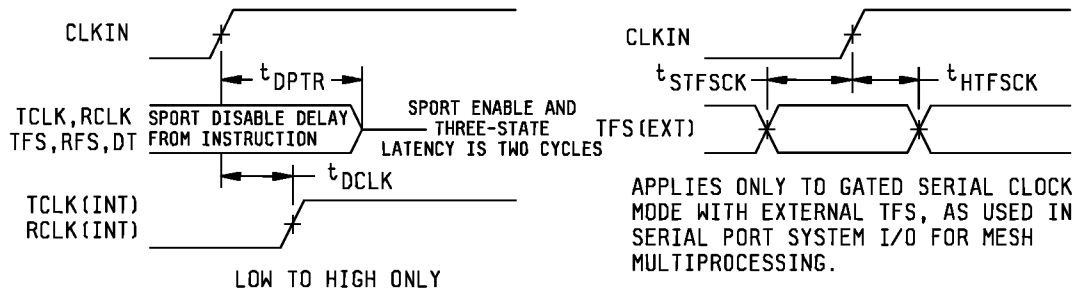
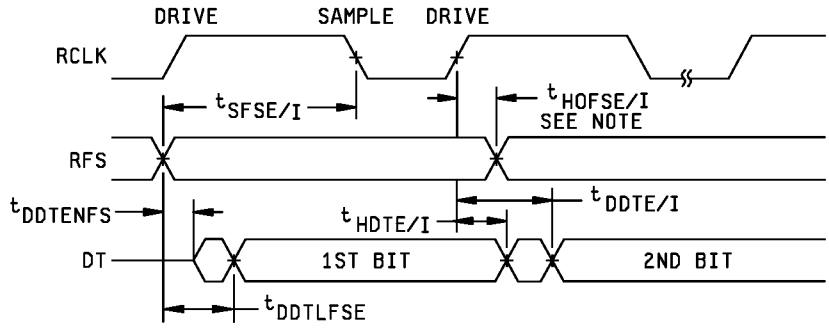


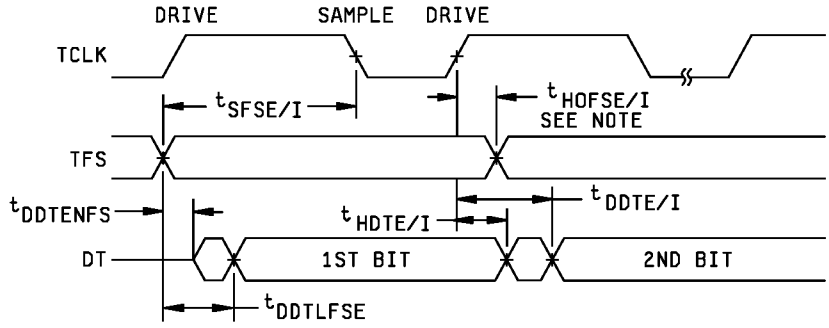
FIGURE 5. Timing waveforms - Continued.



SERIAL PORTS – CONTINUED.



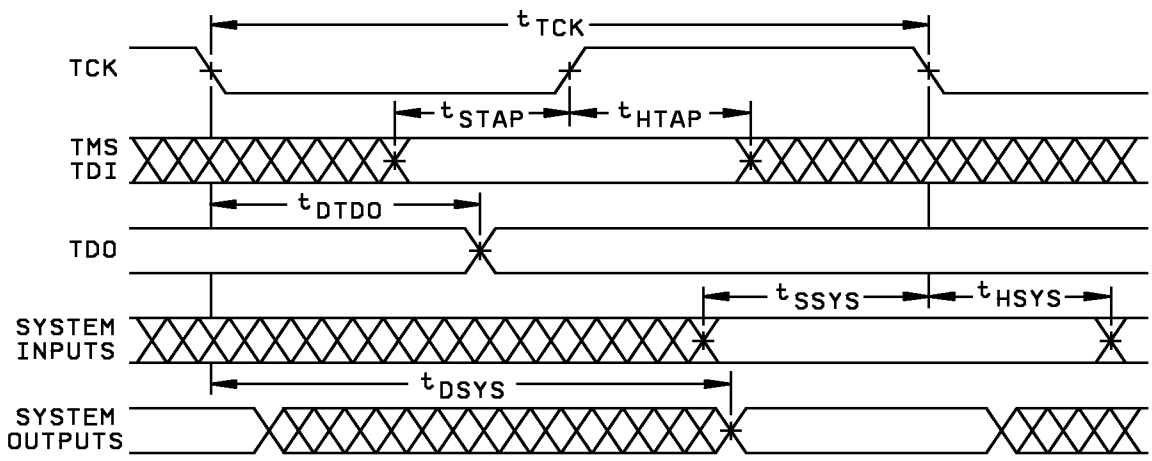
EXTERNAL RFS WITH MCE=1,MFD=0



LATE EXTERNAL TFS

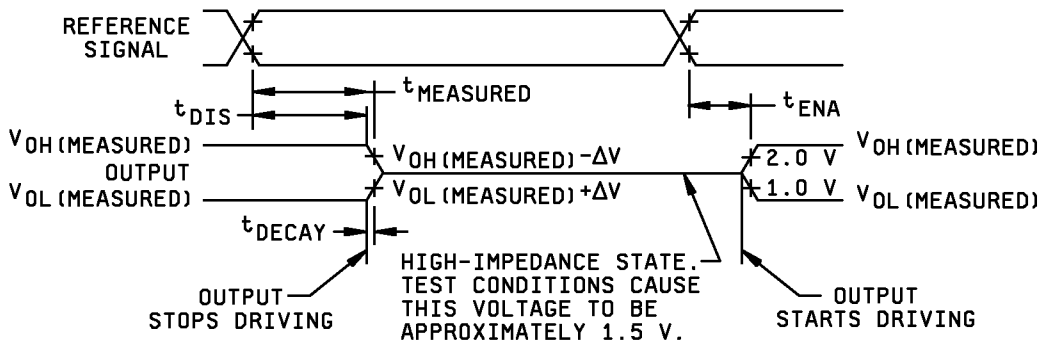
NOTE: RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

FIGURE 5. Timing waveforms - Continued.

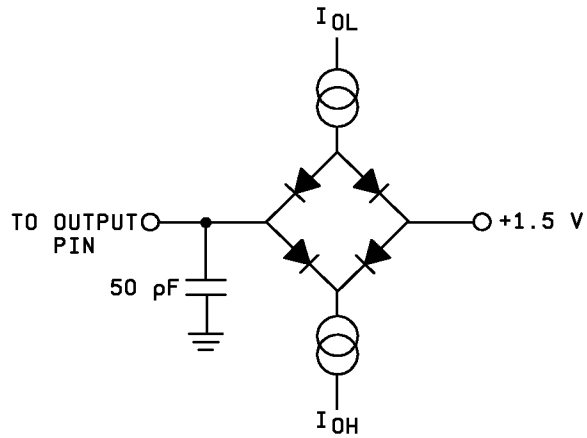


IEEE 11499.1 JTAG TEST ACCESS PORT

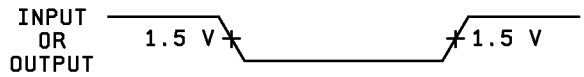
FIGURE 5. Timing waveforms - Continued.



OUTPUT ENABLE/DISABLE



EQUIVALENT DEVICE LOADING
FOR AC MEASUREMENTS
(INCLUDES ALL FIXTURES)



VOLTAGE REFERENCE LEVELS
FOR AC MEASUREMENTS
(EXCEPT OUTPUT ENABLE/DISABLE)

FIGURE 5. Timing waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

Pin symbol	Type 1/	Description
$ADDR_{31-0}$	I/O/T	External bus address. The processor outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the internal memory or IOP registers of other processors. The processor inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	External bus data. The processor inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47-16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47-8 of the bus. 16-bit short word data is transferred over bits 31-16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23-16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS3-0}$	O/T	Memory select line. These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the processor system control register (SYSCON). The $\overline{MS3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS0}$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS3-0}$ lines are output by the bus master.
$\overline{RD}$	I/O/T	Memory read strobe. This pin is asserted (low) when the processor reads from external memory devices or from the internal memory of other processors. External devices (including other processors) must assert $\overline{RD}$ to read from the processor internal memory. In a multiprocessing system $\overline{RD}$ is output by the bus master and is input by all other processors.
$\overline{WR}$	I/O/T	Memory write strobe. The pin is asserted (low) when the processor writes to external memory devices or to the internal memory of other processors. External devices must assert $\overline{WR}$ to write to the processor's internal memory. In a multiprocessing system $\overline{WR}$ is output by the bus master and is input by all other processors.

See footnote 1/ on sheet 55.

Pin symbol	Type 1/	Description - Continued.
PAGE	O/T	DRAM page boundary. The processor asserts this pin to signal that an external DRAM page boundary has ben crossed. DRAM page size must be defined in the processor's memory control register (WAIT). DRAM can only be implemented in external memory bank 0; the PAGE signal can only be activated for bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	Clock output reference. In a multiprocessing system ADRCLK is output by the bus master.
$\overline{SW}$	I/O/T	Synchronous write select. This signal is used to interface the device to synchronous memory devices (including other processors). The processor asserts $\overline{SW}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{WR}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{SW}$ is output by the bus master and is input by all other processors to determine if the multiprocessor memory access is a read or write. $\overline{SW}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the processor(s).
ACK	I/O/S	Memory acknowledge. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The processor deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave processor deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.
$\overline{SBTS}$	I/S	Suspend bus three-state. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high-impedance state for the following cycle. If the processor attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from host processor/processor dead lock,or used with a DRAM controller.
$\overline{IRQ2-0}$	I/A	Interrupt request lines. May be either edge-triggered or level-sensitive.
$FLAG_{3-0}$	I/O/A	Flag pins. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	Timer expired. Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{HBR}$	I/A	Host bus request. Must be asserted by a host processor to request control of the processor's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the processor that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the processor places the address, data, select, and strobe lines in a high-impedance state $\overline{HBR}$ has priority over all processor bus requests ($\overline{BR6-1}$) in a multiprocessing system.

See footnote 1/ on sheet 55.

Pin symbol	Type 1/	Description - Continued.
$\overline{HBG}$	I/O	Host bus grant. Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the processor until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the processor bus master and is monitored by all others.
$\overline{CS}$	I/A	Chip select. Asserted by host processor to select the processor.
REDY (o/d)	O	Host bus acknowledge. The processor deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (o/d) by default; can be programmed in ADREDY bit of SYSCON register to be active drive (a/d). REDY will only be output if the $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	DMA request 1 (DMA channel 7).
$\overline{DMAR2}$	I/A	DMA request 2 (DMA channel 8).
$\overline{DMAG1}$	O/T	DMA grant 1 (DMA channel 7).
$\overline{DMAG2}$	O/T	DMA grant 2 (DMA channel 8).
$\overline{BR6-1}$	I/O/S	Multiprocessing bus requests. Used by multiprocessing processors to arbitrate for bus mastership. A processor only drives its own $\overline{BRx}$ line (corresponding to the value of its ID_{2-0} inputs) and monitors all others. In a multiprocessor system with less than six processors, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
ID_{2-0}	I	Multiprocessing ID. Determines which multiprocessing bus request ($\overline{BR1}$ - $\overline{BR6}$) is used by processor. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, etc. ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired or only changed at reset.
RPBA	I/S	Rotating priority bus arbitration select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every processor. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every processor.
$\overline{CPA}$ (o/d)	I/O	Core priority access. Asserting its $\overline{CPA}$ pin allows the core processor of a processor bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to all processors in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pullup resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DTx	O	Data transmit (serial ports 0,1). Each DT pin has a 50 kΩ internal pullup resistor.
DRx	I	Data receive (serial ports 0,1). Each DR pin has a 50 kΩ internal pullup resistor.

See footnote 1/ on sheet 55.

Pin symbol	Type 1/	Description - Continued.
TCLKx	I/O	Transmit clock (serial ports 0,1). Each TCLK pin has a 50 kΩ internal pullup resistor.
RCLKx	I/O	Receive clock (serial ports 0,1). Each RCLK pin has a 50 kΩ internal pullup resistor.
TFSx	I/O	Transmit frame sync (serial ports 0,1).
RFSx	I/O	Receive frame sync (serial ports 0,1).
$LxDAT_{3-0}$	I/O	Link port data (link ports 0-5). Each LxDAT pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
LxCLK	I/O	Link port clock (link ports 0-5). Each LxCLK pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
LxACK	I/O	Link port acknowledge (link ports 0-5). Each LxACK pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	EPROM boot select. When EBOOT is high, the processor is configured for booting from an 8-bit EPROM. When EBOOT is low, LBOOT and $\overline{BMS}$ inputs determine booting mode. See table below. This signal is a system configuration selection which should be hardwired.
LBOOT	I	Link boot. When LBOOT is high, the processor is configured for link port booting. When LBOOT is low, the processor is set up for host processor booting or no booting. See table below. This signal is a system configuration selection which should be hardwired.
$\overline{BMS}$	I/O/T*	Boot memory select. Output: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{BMS}$ is output by the bus master. Input: When low, indicates that no booting will occur and that processor will begin executing instructions from external memory. See table below. This input is a system configuration selection which should be hardwired.

EBOOT	LBOOT	BMS	Booting mode
1	0	output	EPROM (connect $\overline{BMS}$ to EPROM chip select)
0	0	1 (input)	Host processor
0	1	1 (input)	Link port
0	0	0 (input)	No booting. Processor executes from external memory.
0	1	0 (input)	Reserved
1	1	x (input)	Reserved

* Three-statable only in EPROM boot mode (when $\overline{BMS}$ is an output).

CLKIN	I	Clock in. External clock input to the processor. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{RESET}$	I/A	Processor reset. Resets the processor to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.

See footnote 1/ on sheet 55.

Pin symbol	Type 1/	Description - Continued.
TCK	I	Test clock (JTAG). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test mode select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pullup resistor.
TDI	I/S	Test data input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pullup resistor.
TDO	O	Test data output (JTAG). Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. $\overline{\text{TRST}}$ has a 20 kΩ internal pullup resistor.
$\overline{\text{EMU}}$ (o/d)	O	Emulation status. Must be connected to the processor EZ-ICE target board connector only.
ICSA	O	Reserved, leave unconnected.
VDD	P	Power supply, nominally +5.0 V dc (30 pins).
GND	G	Power supply return (30 pins).
NC	---	Do not connect. Reserved pins which must be left open and unconnected.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

1/ A = Asynchronous
G = Ground
I = Input
O = Output
P = Power Supply
S = Synchronous
A/D = Active Drain
O/D = Open Drain
T = Three-state (when $\overline{\text{SBTS}}$ is asserted or when the processor is a bus slave.)

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-11-24

Approved sources of supply for SMD 5962-96745 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9674501QXC	3/	
5962-9674501QYC	3/	
5962-9674502QXC	24355	ADSP-21060DZ-160/QML
5962-9674502QYC	24355	ADSP-21060DW-160/QML
5962-9674502QTC	24355	ADSP-21060DZ-160/QML
5962-9674502QUC	24355	ADSP-21060DW-160/QML

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Incorporated One Technology Way P.O. Box 9106 Norwood, MA 02062-9106