16 Pin DIL 5 Tap 10K ECL Compatible Active Delay Lines

TAP 1 nS ±5%	TAP 2 nS ±5%	TAP 3 nS ±5%	TAP 4 nS ±5%	OUTPUT nS ±5%	RISE TIME nS MAX	PART NUMBER
3.0 Typ†	4 ± 0.3	5 ± 0.3	6 ± 0.3	7 ± 0.3	4	EP9445-7
3.0 Typ†	5 ± 0.5	7 ± 0.5	9 ± 0.5	11 ± 0.5	4	EP9445-11
3.0 Typ	6 ± 0.5	9 ± 0.5	12 ± 1.0	15 ± 1.5	4	EP9445-15
4 ± 1.0	8 ± 0.5	12 ± 1.0	16 ± 1.5	20 ± 2.0	4	EP9445-20
5 ± 1.0	10 ± 1.0	15 ± 1.5	20 ± 2.0	25 ± 2.0	4	EP9445-25
6 ± 1.0	12 ± 1.0	18 ± 1.5	24 ± 2.0	30 ± 2.0	4	EP9445-30
8 ± 1.0	16 ± 1.5	24 ± 2.0	32 ± 2.0	40	5	EP9445-40
10 ± 1.0	20 ± 2.0	30 ± 2.0	40	50	5	EP9445-50
15 ± 1.5	30 ± 2.0	45	60	75	8	EP9445-75
20 ± 2.0	40	60	80	100	10	EP9445-100
30 ± 2.0	60	90	120	150	15	EP9445-150
40	80	120	160	200	20	EP9445-200
50	100	150	200	250	25	EP9445-250
60	120	180	240	300	30	EP9445-300
70	140	210	280	350	35	EP9445-350
80	160	240	320	400	40	EP9445-400
90	180	270	360	450	45	EP9445-450
100	200	300	400	500	50	EP9445-500
120	240	360	480	600	50	EP9445-600
140	280	420	560	700	50	EP9445-700
160	320	480	640	800	50	EP9445-800
180	360	520	720	900	50	EP9445-900
200	400	600	800	1000	50	EP9445-1000

Delay time measured at - 1.3V, no load
Delay times referenced from input to leading edges
†Inherent delay

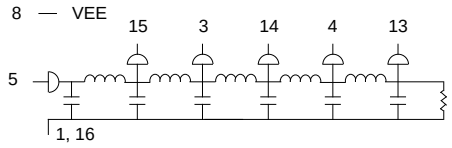
Rise time output measured from 20% to 80%
Output terminated (externally) with 50Ω to - 2.0Vdc

DC Electrical Characteristics

	Parameter	*Test Conditions	Min	Max	Unit
V_{OH}	High-Level Output Voltage	V_{IL} = Min	-960		mV
V_{OHT}	High-Level Output Threshold Voltage		-980		mV
V_{OLT}	Low-Level Output Threshold Voltage			-1630	mV
V_{OH}	Low-Level Output Voltage	V_{IH} = Max		-1650	mV
I_{IH}	High-Level Input Current	V_{IH} = Max		265	µA
I_{IL}	Low-Level Input Current	V_{IL} = Min	0.5		µA
I_{EE}	V_{EE} Supply Current			50	mA

* (V_{CC1} = V_{CC2} = GRD, V_{EE} = -5.2V ± 0.01V, Output Loading with 50Ω to -2.0V ± 0.01V)

Schematic



Recommended Operating Conditions

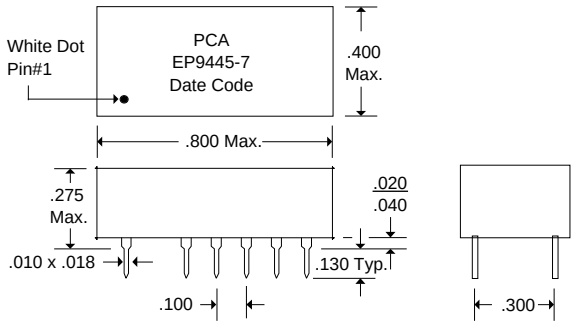
		Min	Max	Unit
V_{EE}	Supply Voltage (Negative)	4.94	5.46	V
V_{CC}	Circuit Ground (Pins 1 and 16)	0	0	V
V_{IH}	HIgh-Level Input Voltage	-980		mV
V_{IHT}	High-Level Input Threshold Voltage		-1105	mV
V_{ILT}	Low-Level Input Threshold Voltage		-1475	mV
V_{IL}	Low-Level Input Voltage		-1630	mV
P_W*	Pulse Width of Total Delay	300		%
d*	Duty Cycle		20	%
T_A	Operating Free-Air Temperature	-30	+80	°C

These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C

V_{IN}	Pulse Input Voltage	-1.0V (-0.75 to -1.75V)
P_W	Pulse Width of Total Delay	3x Total Delay
T_{RI}	Pulse Rise Time (20% to 80%)	2 nS
P_{RR}	Pulse Spacing	10x Total Td
V_{EE}	Supply Voltage	-5.2V

Package Dimensions



DSD9445 8/25/94

QAF-CSO1 Rev. B 8/25/94

Unless Otherwise Noted Dimensions in Inches
Tolerances:
Fractional = ± 1/32
.XX = ± .030 .XXX = ± .010

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