APPLICATION NOTE

AN214
74F extended octal-plus family applications

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Philips
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74F extended octal-plus family applications AN214

74F Extended Octal-Plus Family Features

- 8-, 9-, and 10-bit "Light-Load" bus products
  - Buffers/Drivers
    With and without latches or registers
    With and without 8-bit parity checker/generator
  - Transceivers
    With and without dual registers
    With and without 8-bit parity checker/generator
- Patented "Light-Load" inputs:
  - Input Current = ±20µA per input
  - Transceiver I/O pins = ±70µA
- High performance output drive currents:
  - I_{OL} = 64mA/48mA @ ±5%/10% V_{CC}
  - I_{OH} = –15mA/–3mA @ ±5%/10% V_{CC}
- "Flow-through" or "broadside" I/O pin configuration
- Ideal for MOS CPU, peripherals and semi-custom bus interface
- 24-pin, 300mil-wide, plastic slim-DIPs
- High performance buffers — $t_{P(max)}$ = 7.5ns
- High performance latches/registers — f_T = 100MHz

Introduction

The 74F Extended Octal-Plus Family incorporates all of the latest Philips Semiconductors octal, 9-bit and 10-bit buffer, transceiver, latch and register functions. all devices in this family utilize the Philips Semiconductors patented "Light-Load" NPN, ±20µA input current structure and have "flow-through" or "broadside" input/output pin configurations where the inputs and outputs are lined-up on opposite sides of a standard 24-pin Slim-DIP package. The "light-load" inputs, "broadside" design and high functional density/performance of the family make this product line ideal for buffering the limited drive capabilities of standard, custom and semicustom MOS VLSI devices to the rigorous environments of today's leading edge high performance logic designs. The family also is an excellent choice for all general interface applications.

"Flow-Through" Design

The "flow-through" or "broadside" chip layout/package design is illustrated in Figure 1 showing the block diagrams and pin configurations of the 74F828 10-bit Inverting buffer. Note that all of these "broadside" designs allow logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F240 Octal Buffers (Figure 2). If you compare the physical layout requirements of the path of PC board bus lines for the 74F828 to that of the 74F240's "zig-zag" path, you will see the significant advantages of the 74F Extended Octal-Plus Family's "flow-through" design in simplifying the design and layout of large, high density, bus-oriented PC boards.

The 24-pin, 300mil-wide, Slip-DIP Solution

With the advent of advanced Schottky TTL technology came the ability to significantly increase the functional density of standard logic building blocks. However, not until the development of the 24-pin, 300mil-wide, Slim-DIP package was it possible to take full advantage of these new chip densities. The entire family provides significant advantages in package count, pin count and packing density when compared to older technologies. Further density enhancements can be achieved by using Philips surface mounted packages.

By combining high functional density into a 24-pin 300mil-wide Slim-DIP package, the Philips Semiconductors 74F Extended Octal-Plus Family allows the reduction of PC board parts count and cost while optimizing layout with "broadside" chip designs, reducing total system power dissipation and increasing system reliability.

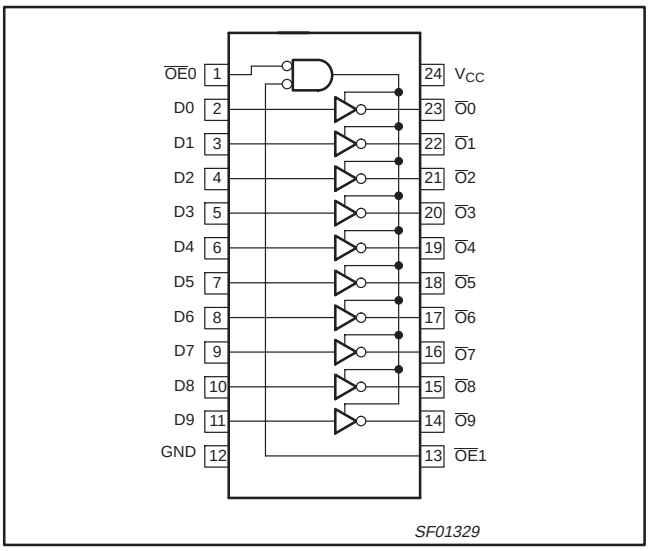


Figure 1. 74F828 Broadside Pin Configuration

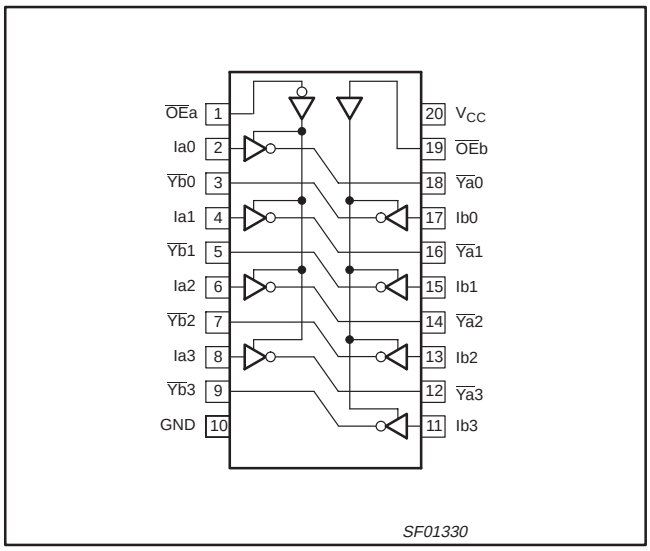


Figure 2. 74F240 'Zig-Zag" Pin Configuration

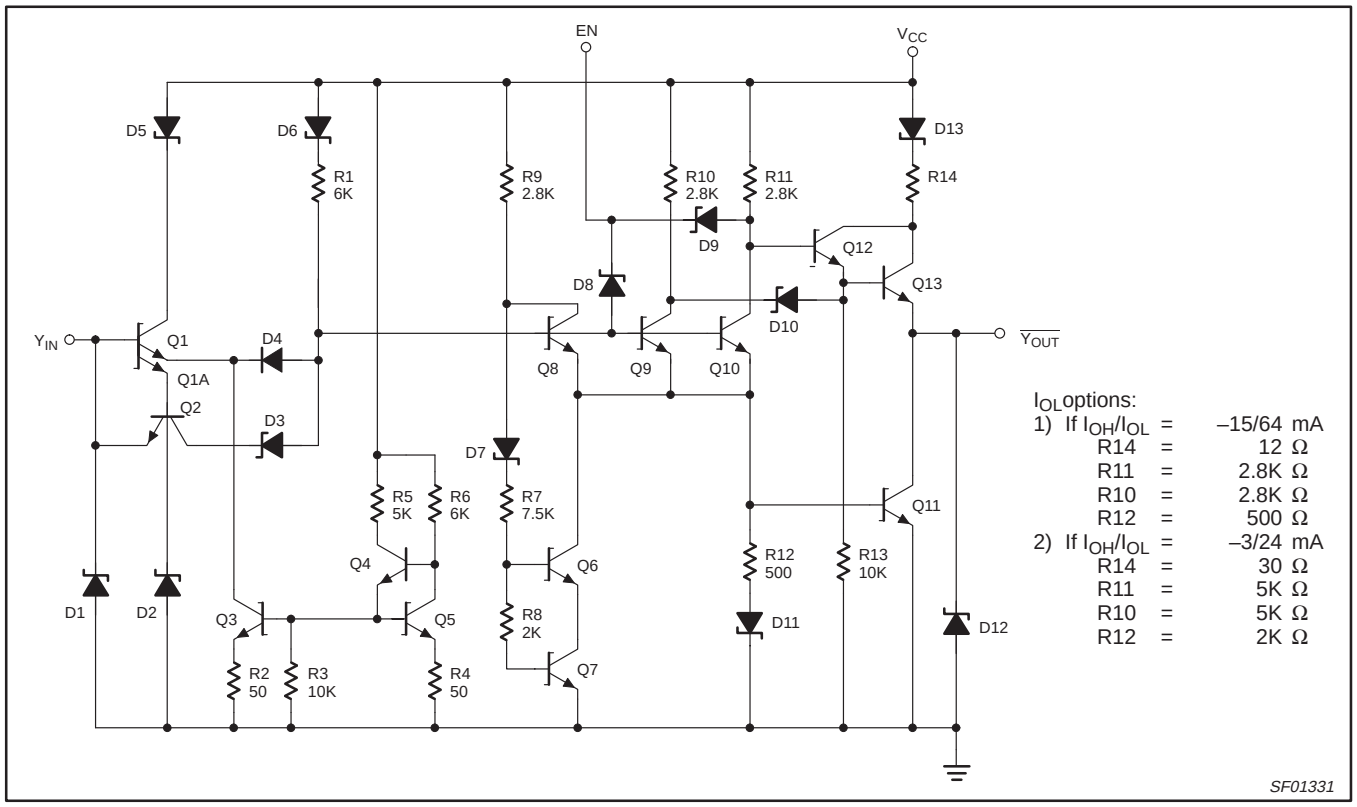


Figure 3. 74F455 Buffer/Drive Cell Circuit Diagram

The 8-, 9-, and 10-bit Series 24-pin Solution

Whether your system requires an 8–, 9-, or 10-bit bus interface, the Extended Octal-Plus Family has standardized solutions in 24-pin/Slim-DIP/Broadside input/output packages with corner power supply pins (12 & 24) and standard designations for common control functions located at or near the package corners. Octals offer more mode control inputs than do the 9- or 10-bit products. Virtually all family devices with 3-State outputs are guaranteed to source/sink –15/64mA @ V_{OH}/V_{OL} = 2.0/0.55V (except for the 74F841–846 Latched Drivers, which are spec'ed at –15mA/48mA). The A_N port outputs of several of the family's transceivers are guaranteed to supply –3mA/48mA).

The Octal Parity Bus Series offers several notable exceptions to the above standard pinouts. This series has three parts with two center-package ground pins to minimize ground-bounce noise. All outputs (except the A_N port of the 74F657 Parity Bus Transceiver spec'ed at –3mA/24mA) are guaranteed to source/sink more than –15mA/64mA.

Current PC board, multi-layer technology make is possible to take into consideration the physical location of input/output pins, transmission line characteristics and supply power distribution. Lining up all inputs and output on opposite sides of the package allows the address, data and control bus signal to flow in a direct physical path from the μP CPU through the bus interface chips and onto the appropriate bus. This "broadside" bus design approach produces very clean PC board layouts and may, in fact eliminate and entire PC board interconnection layer. Standardization of power supply, mode control and input/output pins, whether 8-, 9-, or 10-bit bus functions, permits simplified, structured PC board layout.

Input Structures

Referring to Figure 3, the 74F455 Inverting Buffer/Driver Cell Circuit Diagram is an example of the family's input and output circuitry. The patented Philips Semiconductors "Light-Load" NPN input structure (Q1/23/4/5, R1/2/3/4/5/6 and D4) and turn-OFF speed-up circuit (Q2 and D2/3) are used throughout the 74F Extended Octal-Plus Family. the "Light-Load" NPN input is actually a high speed, differential amplifier with the reference side, the anode of D4, clamped at two diode voltage drops above ground (BE junctions of Q8/9/10 and Q 11 of ~1.4V at 25°C). When the V_{IH} rises above this clamp voltage, the BE junction of Q1 is forward based allowing beta amplified, CE current to flow into the <1.0mA constant current source, Q3 (driven by Q4/5 and R2/3/4/5/6). The beta of Q1 is guaranteed, by design, to be >50, thereby guaranteeing that the input base bias current will be <20μA. The emitter of Q1 rises to $1V_{BE}$ (~300mV) below the V_{IH}, reverse biasing D4 and permitting C8/9/10 base bias current to flow through R1.

The patented turn-OFF circuit consisting of Q2 and D2/3 produces a dynamic speed to help turn Q8/9/10 OFF quickly. During the time that the Q1 is turned-ON (input = V_{IH} >2.0V), the revers-biased Schottky diode, D2, acting as a capacitor, will be charged to the voltage at the emitter of Q1A or $1V_{BE}$ voltage drop below the input (>2.0 – $1V_{BE}$). When the input is switched to <V_{IL} (or <0.8V), the D2 stored charge discharges through the BE of Q2. Q2 CE current through D3 rapidly turns Q8/9/10 OFF.

These circuit innovations produce high performance, very low input bias current (±20μA) gate inputs. This input leakage represents a 30X reduction over the standard 74F family's 600μA input current with virtually no loss in speed. The 74F Extended Octal-Plus

Transceivers have an input loading current of ±70µA, which is the combination of the "Light-Load" NPN input structure's ±20µA and the 3-State Hi-Z output's ±50µA leakage current.

The low "Light-Load" input current and high speed performance makes this family ideal for interfacing to low drive capability, slower MOS CPU, peripherals and semi-custom chips used in most of today's state-of-the-art logic designs. Besides very low input current requirements, this "Light-Load" input has another significant advantage over "traditional" input structures: Very low input capacitance (smaller stored charge) due to very small device geometries. Therefore, when Extended Octal-Plus devices are connected to a bus, they present less AC bus loading and do not significantly lower the characteristic impedance of the bus to the extent "traditional" input structures do. Thus, the amount of the AC current a bus driver has to produce to change the state of the bus is lowered and in many cases can make a difference between incident wave switching of the bus versus losing time waiting for a reflected wave.

The Philips Semiconductors 74F "Light-Load" input structure is discussed in more detail in *Application Note AN215*.

Output Drive Capabilities

Virtually all devices in the EXtended Octal-Plus Family are guaranteed to source/sink more than –15mA/64mA @ $V_{OH}V_{OL}$ = 2.0/0.55V. One exception is the 74F841-thru-846 Series of Bus Interface Latches which are specified at –15/48mA. Several of the family's transceiver products have lower A_N output drive capabilities to reduce package power dissipation. Refer to Tables 1 and 3.

For example, the 74F657 Parity Bus Transceiver has two output ports with different capacities: The A_N port is guaranteed to source/sink –3mA/24mA (I_{OH}/I_{OL} = 2.4/0.50V), and the B_N port has an output drive capability of –15mA/64mA at 2.0V/0.55V. The 74F657's A_N port is designed to interface the chip side of the PC board to the backplane bus, while the B_N port is capable of driving a transmission line or bus backplane line.

Referring to Figure 3, all of the Family's 3-State, totem-pole output structures have a schottky blocking diode, D13, in their pull-up output structures. These diodes block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground.

This gives a very important advantage of being able to power down a PCB (or several PCBs) without disabling the bus and even without producing any glitching on the bus due to an undesired change in the output state of the device being powered down.

The output short-circuit (I_{OS}) limiting resistor (R14), the anode-to-cathode resistance/voltage drop of D13 and the collector-to-emitter/base-to-emitter resistance/voltage drop of Q13 limit the amount of current that can be sourced from a HIGH level output at a specified V_{OH}. For most of the parts in the family, R14 is equal to 12Ω. the A_N port of several of the transceivers utilize an R14 of 30Ω producing I_{OH} (@ V_{OH} = 20V) of –6mA versus –15mA from the B_N ports 12Ω R14.

The output HIGH level sourcing current, I_{OH}, at a specified output voltage, V_{OH}, can be calculated by subtracting the voltage drops of D13, the pull-up darlington transistor, Q12/13, and the desired V_{OH} level from V_{CC} and dividing by the value of R14 plus the anode-to-cathode resistance of D13 and the collector-to-emitter/base-to-emitter resistance.

Assumptions:
$V_{D13} \cong 0.5V$ @ $R_{ON} = 3\Omega$ @ 25°C),
$V_{Q12/13} \cong 1.2V$ @ $R_{ON} = 8\Omega$ @ 25°C)
$I_{OH} = 1[V_{CC}–(V_{D13} + V_{Q12/Q13} + V_{OH})]/(R14 + R_{D13} + R_{Q13})$.
$I_{OH}(R14 = 12\Omega) = –[4.5V–(0.5V + 1.2V + 2.0V)]/23\Omega = –35mA$
$I_{OH}(R14 = 30\Omega) = –[4.5V–(0.5V + 1.2V + 2.0V)]/41\Omega = –20mA$
$I_{OS} = I_{OH}$ @ V_{OH} = 0.0V and V_{CC} = 5.5V
$I_{OS}(R14 = 12\Omega) = –[5.5V–(0.5V + 1.2V)]/23\Omega = –165mA$
$I_{OS}(R14 = 30\Omega) = –[5.5V–(0.5V + 1.2V)]/41\Omega = –93mA$

Obviously, we have been very conservative in the I_{OH} specification to guardband against all conditions of temperature and input/output/supply voltage levels. The R_{ON} resistances of the output pullup transistors and blocking diode are large enough to prevent I_{OS} from exceeding –225mA for R14 = 12Ω and –150mA for R14 = 30Ω. (Refer to Table 1.)

Table 1. Family Output Drive Capabilities Using the 74F657 Parity Bus Transceiver

DC ELECTRICAL CHARACTERISTICS
Over recommended operating conditions, V_{IL} = MAX and V_{IH} = MIN)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	I_{OH} = –3mA ±10% V_{CC}	2.4			V
			I_{OH} = –3mA ±5% V_{CC}	2.7	3.4		V
		B_N port, PARITY, $\overline{ERROR}$	I_{OH} = –15mA ±10% V_{CC}	2.0			V
			I_{OH} = –15mA ±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_N port	I_{OL} = 24mA ±10% V_{CC}		0.35	0.50	V
			I_{OL} = 24mA ±5% V_{CC}		0.35	0.50	V
		B_N port, PARITY, $\overline{ERROR}$	I_{OL} = 48mA ±10% V_{CC}		0.40	0.55	V
			I_{OL} = 48mA ±5% V_{CC}		0.40	0.55	V
I_{OS}	A_N output High level short circuit current (R14 = 30Ω)		V_{CC} = MAX			–150	mA
	B_N output High level short circuit current (R14 = 12Ω)		V_{CC} = MAX			–225	mA

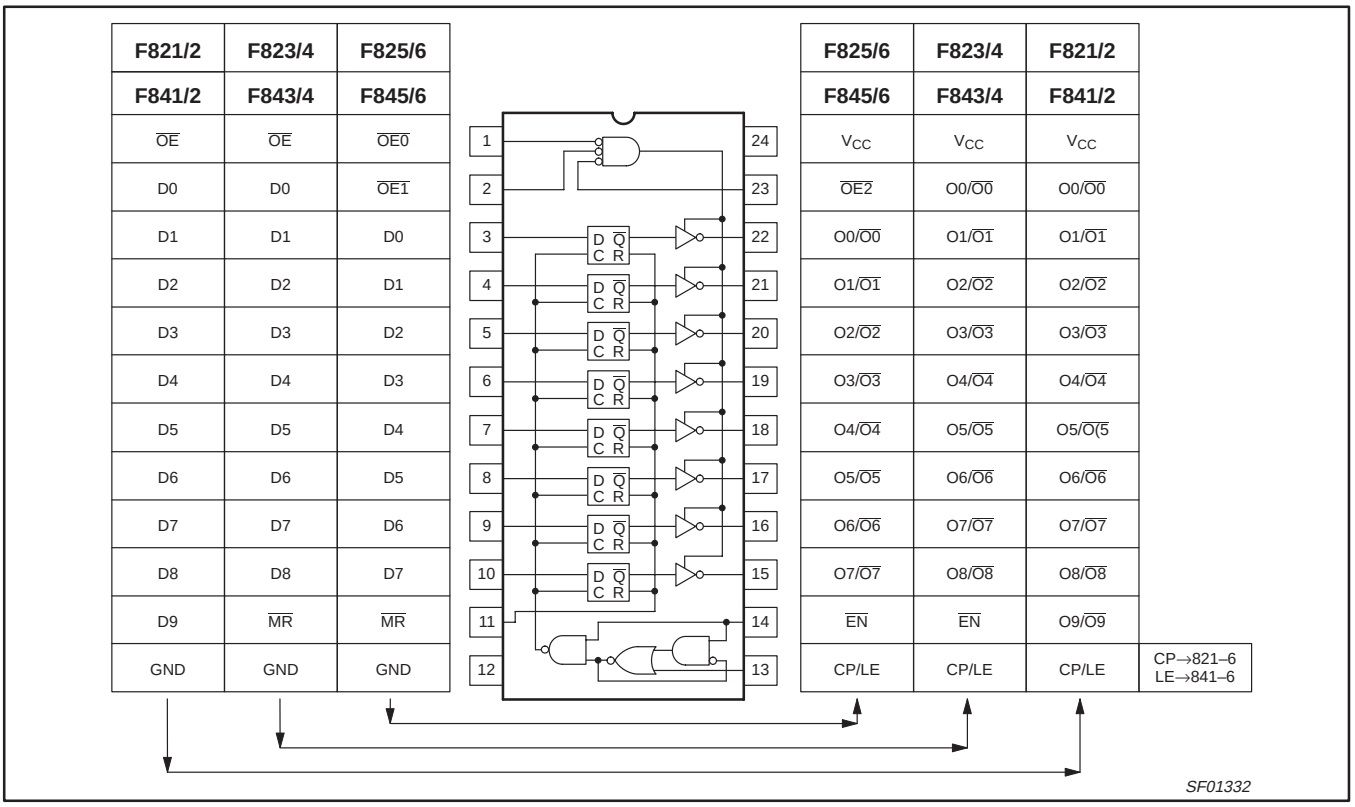


Figure 4. 74F82X and 74F84X Registered/Latched Buffer Pin Configurations

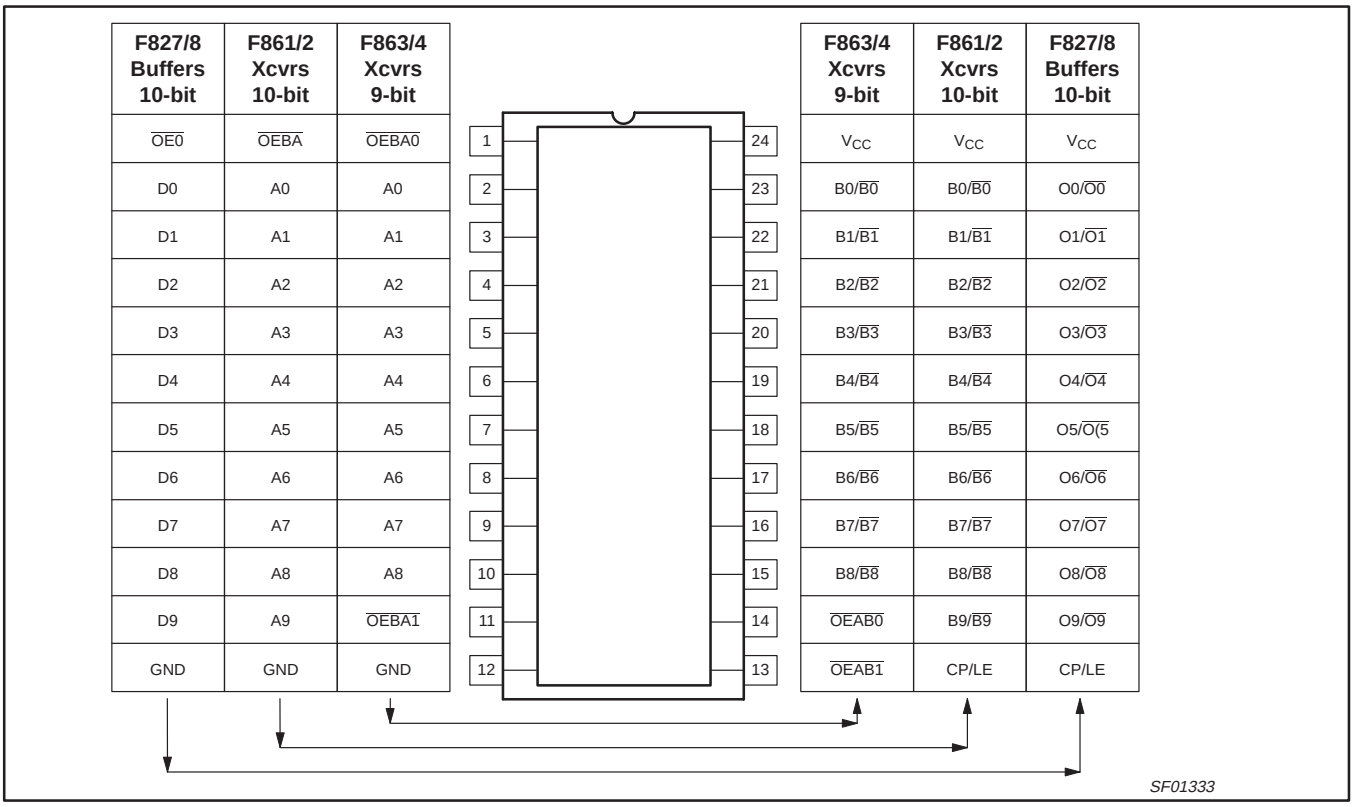


Figure 5. 74F827/8 and 74F861–4 Buffers and Transceivers Pin Configurations

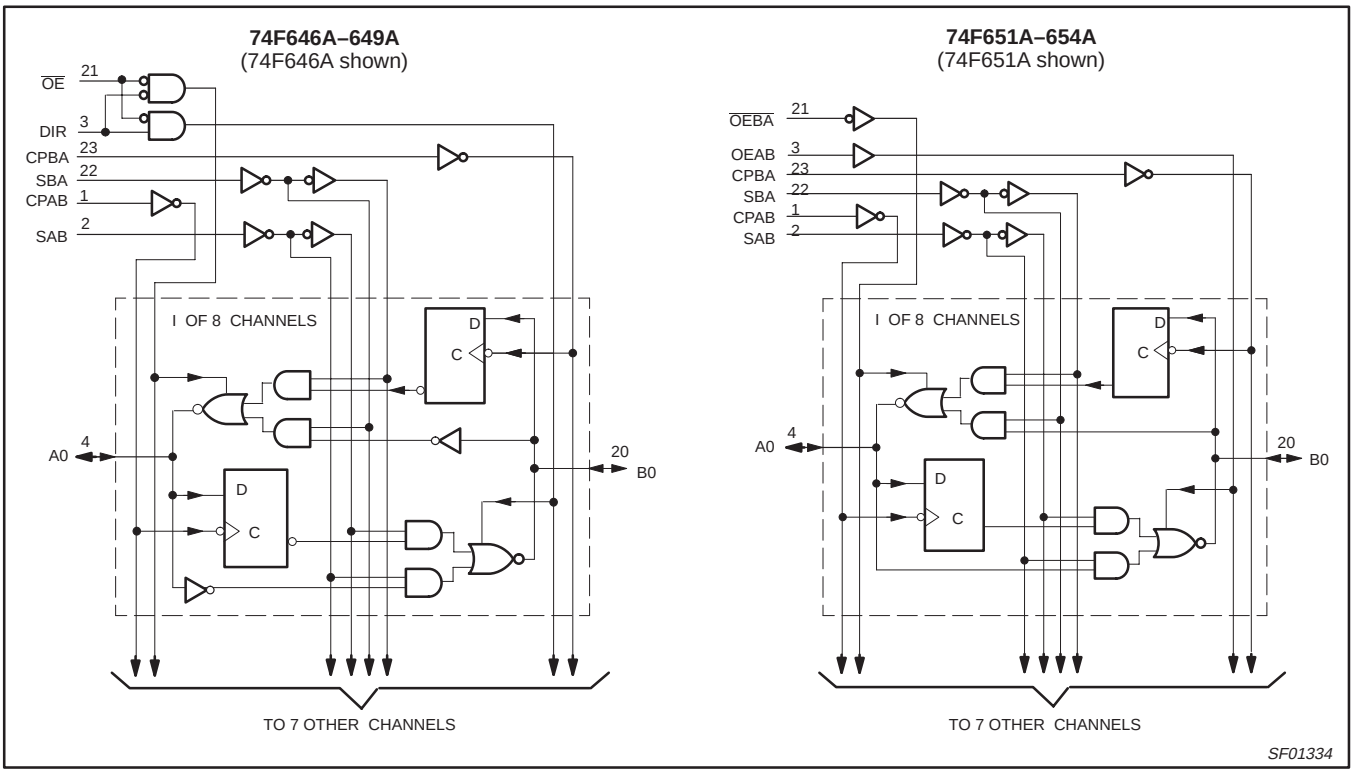
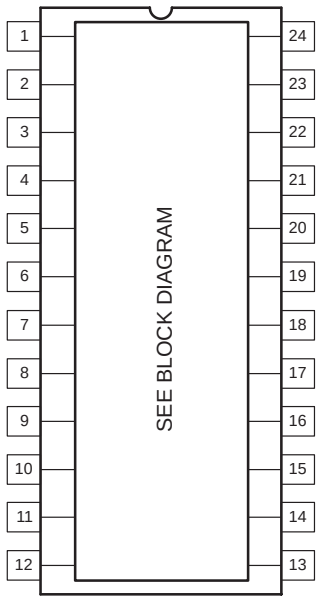


Figure 6. 74F646A–649A and 74F651A–654A Registered Transceivers Simplified Logic Block Diagrams

F646A/7A 3-St/OC	F648A/9A 3-St/OC	F651A/3A 3-St/OC	F652A/4A 3-St/OC
CPAB	CPAB	$\overline{OEBA}$	$\overline{OEBA0}$
SAB	SAB	SAB	SAB
DIR	DIR	OEAB	OEAB
A0	$\overline{A0}$	$\overline{A0}$	A0
A1	$\overline{A1}$	$\overline{A1}$	A1
A2	$\overline{A2}$	$\overline{A2}$	A2
A3	$\overline{A3}$	$\overline{A3}$	A3
A4	$\overline{A4}$	$\overline{A4}$	A4
A5	$\overline{A5}$	$\overline{A5}$	A5
A6	$\overline{A6}$	$\overline{A6}$	A6
A7	$\overline{A7}$	$\overline{A7}$	A7
GND	GND	GND	GND



F652A/4A 3-St/OC	F651A/3A 3-St/OC	F648A/9A 3-St/OC	F646A/7A 3-St/OC
V_{CC}	V_{CC}	V_{CC}	V_{CC}
CPBA	CPBA	CPBA	CPBA
SBA	SBA	SBA	SBA
$\overline{OEBA}$	$\overline{OEBA}$	$\overline{OE}$	$\overline{OE}$
B0	$\overline{B0}$	$\overline{B0}$	B0
B1	$\overline{B1}$	$\overline{B1}$	B1
B2	$\overline{B2}$	$\overline{B2}$	B2
B3	$\overline{B3}$	$\overline{B3}$	B3
B4	$\overline{B4}$	$\overline{B4}$	B4
B5	$\overline{B5}$	$\overline{B5}$	B5
B6	$\overline{B6}$	$\overline{B6}$	B6
B7	$\overline{B7}$	$\overline{B7}$	B7

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Figure 7. 74F646A–649A and 74F651A–654A Dual Registered Transceivers Pin configurations

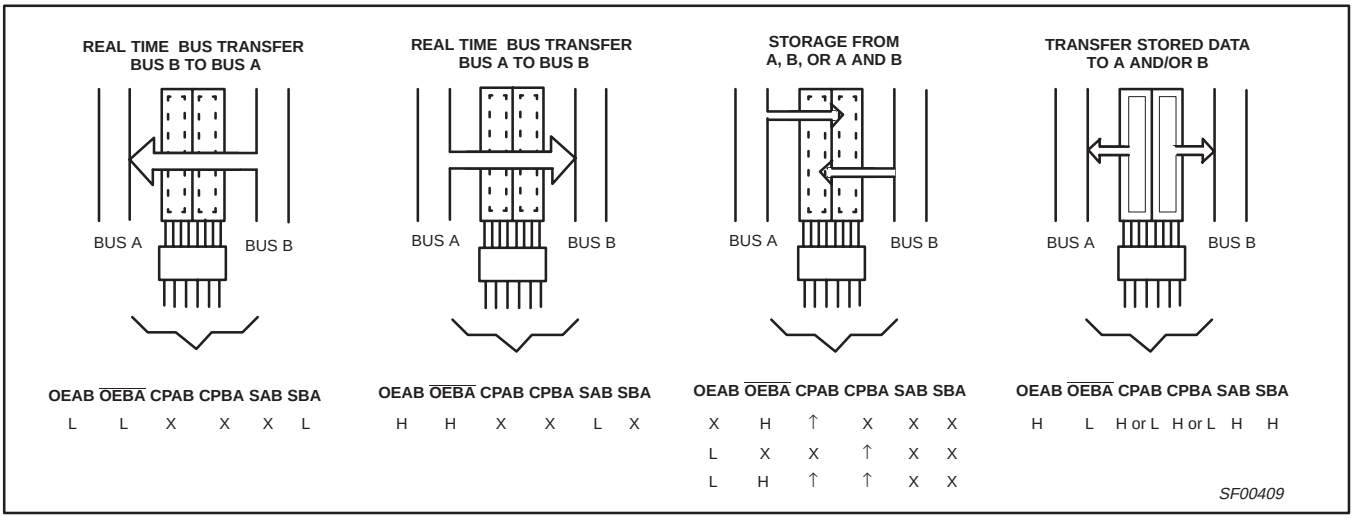

Figure 8. 74F651A–654A Registered Transceivers Storage Options (74F646A–649A not shown)

Table 2. Parity Bus Family versus the Competition

PART NUMBER	DESCRIPTION	TOTAL # OF PINS	t_{PDmax}* IN to OUT	t_{PDmax}* IN to PARITY	I_{CCmax}**	POWER PINS	BROADSIDE DESIGN
74F455/F456 vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Center	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F655A/F656A vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Corner	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F657 vs. 74F240/F245 + 74F280 + 1 AND gate	Octal Parity Transceiver	24	7.5ns	16.0ns	110mA	Center	Yes
		38	8.0ns	14.5ns	125mA	Corner	No

NOTES:
* Propagation delays of DATA IN-to-DATA OUT and IN-to-PARITY OUT, T_{amb} = 0°C to 70°C, V_{CC} = +5.0V ±10%, Output Load = C_L = 50pF, and R_L = 500Ω.
** Worst case power, T_{amb} = 0°C to 70°C, V_{CC} = +5.0V ±10%, Output Load = C_L = 50pF, and R_L = 500Ω.

74F821–74F863 Series

The 74F821 through 74F863 Series of Octal 9-bit and 10-bit Buffers, Latch Buffers, Register Buffers and Transceivers are standardized around the AMD 298XX series with one significant difference—the Philips Semiconductors "Light-Load" NPN input offers a 50:1 reduction in input loading (1000µA vs. 20µA). This series illustrates the standardized on 24-pin/300mil-wide Slim-DIP packages, "broadside" input/output pinouts and control function pins. All 74F8XX 3-State outputs are guaranteed to source/sink –15mA/64mA, except for the 74F84X Latched Buffers, which are specified at –15mA/48mA.

The logic diagram and pin configurations of the 74F828 Non-Inverting 10-bit Buffer (Figure 1) and the 74F821–826 and 74F841–846 Registered/Latched Buffers (Figure 4) are excellent illustrations of the standardized pin configuration illustrating "broadside" chip design.

Figure 5 shows the pinouts of the 74F827/828 buffers and 74F861–864 Transceivers. There currently are no 9-bit buffer offerings in this series.

Registered Transceiver Series

the 74F646A–649A and 74F651A–654A Octal Dual-Registered Transceivers offer a "Light-Load" combination of a 74F245 type transceiver with two 74F373/374 type octal registers within a 24-pin Slim-DIP broadside input/output package. This series offers a significant 6:1 package count reduction advantage over older technologies.

Figure 6 shows the 74F646A and 74F651A Transceivers Simplified Block Diagrams, and this series' pin configurations are depicted in Figure 7. Figure 8 graphically illustrates four optional storage and transfer modes of the 74F651A Octal, Non-Inverting, 3-State, Dual-Registered Transceiver. The 74F654A will be used to explain the operation of the entire series. The 74F646A/648A (3-State, INV/NINV) and the 74F647/649 (O.C., INV/NINV) Octal Dual-Registered Transceivers offer optional signal direction control logic and output enable to the 74F651A–654A series.

This series allows you to store or real-time transfer data in either direction through the transceiver function. Data at the A_N port can be stored in either the A_N port register or the B_N register and, then, can

be transferred either from the A_N port register to the B_N port outputs or from the B_N port register to the A_N port outputs.

The same capabilities are available to data presented to the B–port. When a port's output buffers are enabled ($\overline{OE}$ = LOW and DIR = LOW for A_N outputs enabled or HIGH for B_N outputs enabled), the SXX select inputs (SAB and SBA) control the two EX-OR gates allowing the output port data to come either directly from the other port (real-time transfer) or from the other port's input storage register.

The CPABN and CPBA inputs are the LOW-to-HIGH edge-triggered clock inputs for the A_N port register and B_N port register. Data presented to either port's inputs can be clocked into its input register on a LOW-to-HIGH CPXX input regardless of the logic levels on any of the other mode control inputs.

The 74F651A–654A's OEAB and $\overline{OEBA}$ output enable inputs may be tied together to enable the B outputs when HIGH or A_N outputs when held LOW or can be used separately to independently control the two output ports. Tying the 74F651A–654A's OEAB and $\overline{OEBA}$ together is logically equivalent to the DIR input of the 74F646A–649A.

Parity Bus Series Advantages

The increased functional density of the Parity Bus Series produces a 2:1 package reduction (plus 1 AND gate) and, therefore, 38:24 pin reduction. Power dissipation savings of 82.5mW for the 74F455/456/655A/656A Drivers and 137.5mW for the 74F657 are also achieved through shared internal logic. Table 2 shows the package/pin advantage as well as the worst case propagation delays and I_{CC} of the Family versus their competition.

Figure 9 is a summary of the pin configurations of the entire Parity Bus Drivers and Transceiver Series.

The 74F455/456/655A/656A Octal Parity Bus Drivers and the 74F657 Octal Parity Bus Transceiver Series combines the popular Philips Semiconductors 74F24X buffer/transceiver functions with the 74F280B 9-bit Parity Generator/Checker, "Broadside" input/output pin configurations, "Light-Load" inputs and an increased guaranteed sink/source capabilities of –15mA/64mA for low impedance bus environments. The 74F445/446 Drivers with their multiple center-package ground supply pins are logically identical to the 74F655A/656A Drivers, except for the latter's single corner-package supply pins and an additional $\overline{\text{Output Enable}}$ input. The 74F657 Parity Bus Transceiver allows the parity to be generated and checked in both directions in a single package replacing one 74F245 Transceiver, 20-pin DIP and two 74F280, 16-pin DIPs plus a couple of gates.

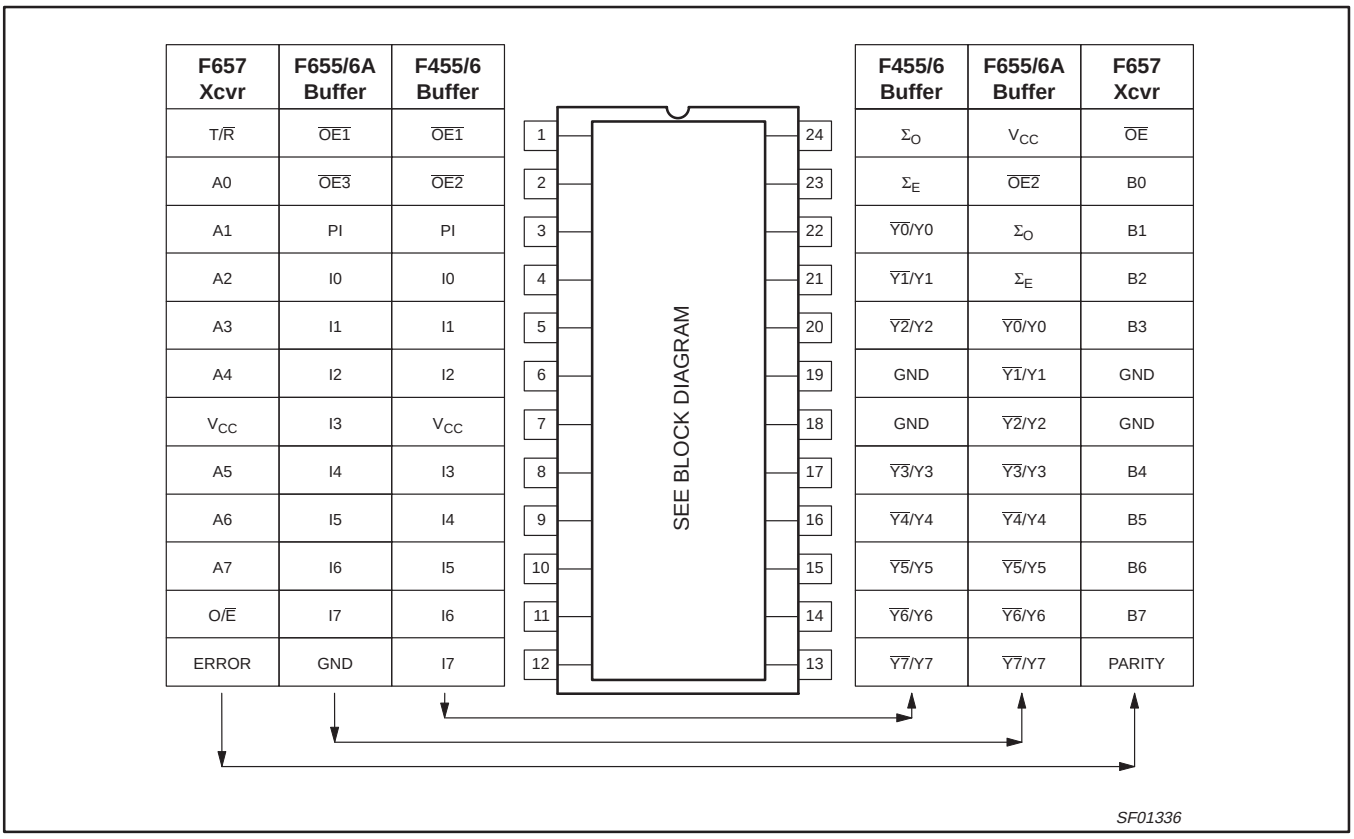

Figure 9. 74F Octal Parity Drivers/Transceiver Pin Configurations

74F657 Operation

The 74F657 Parity Bus Transceiver, as shown in its simplified logic diagram, Figure 10, is a combination of a 74F245 Octal Transceiver and a 74F280B 9-bit Parity Generator/Checker plus one AND gate. Figure 11 expands the logic block diagram of the Family's Parity Tree Logic (inside the dashed line of Figure 10).

During TRANSMIT mode (A_N = Hi-Z), the PARITY and $\overline{ERROR}$ outputs are generated from the A_N input/output port. In the RECEIVE mode, the B_N port is the input from the system or mother board bus (B-port outputs = Hi-Z).

For best speed performance, PARITY should always be generated from the A_N port for the B_N port (TRANSMIT mode), and parity $\overline{ERROR}$ should always be checked for data coming in on the B-port (RECEIVE mode). EVEN or ODD parity generation and checking is determined by the EVEN/$\overline{ODD}$ input (EVEN = HIGH, and ODD = LOW).

In the TRANSMIT mode (T/$\overline{R}$ = HIGH), transmitted data travels from the A-port to the B-port in less than 8.0ns generating a PARITY bit output in less than 16.0ns. Whereas, in the RECEIVE mode (T/$\overline{R}$ = LOW), received data traverses from the B-port to the A-port path in, again, less than 8.0ns, but then the $\overline{ERROR}$ checking output, being generated from the output data presented to the A-port and the PARITY input, takes an additional 16.5ns or less to stabilize. Therefore, the total RECEIVEd-data-to-$\overline{ERROR}$ checking output propagation time is the sum of the B_N-to-A_N delay (8ns) and the A_N/PARITY-to-$\overline{ERROR}$ output delay (16.5ns) or 22.5ns.

However, in many cases, the propagation delay that has to be taken into consideration does not have to include parity calculation time and could be equal to that of just the transceiver part (8ns). This is due to the fact that it may not be too late to interrupt whatever needs to be interrupted in case of a parity error after the data has already gone by (i.e., via late bus error).

Parity Tree Analysis

The basic 3-input Comparator Cell, inside the dashed line in Figure 11, is used throughout the Parity Bus Series. If there are an even number of HIGH inputs (0 or 2) the output of the 3-Input Comparator Cell will be HIGH, while an odd number (1 or 3) will produce an output LOW. The 74F657's Parity Tree Logic, combines four of the 3-Input Comparators with a 2-input comparator, a 2-input AND gate and output buffers for PARITY and $\overline{ERROR}$ to produce the complete parity generator/checker logic.

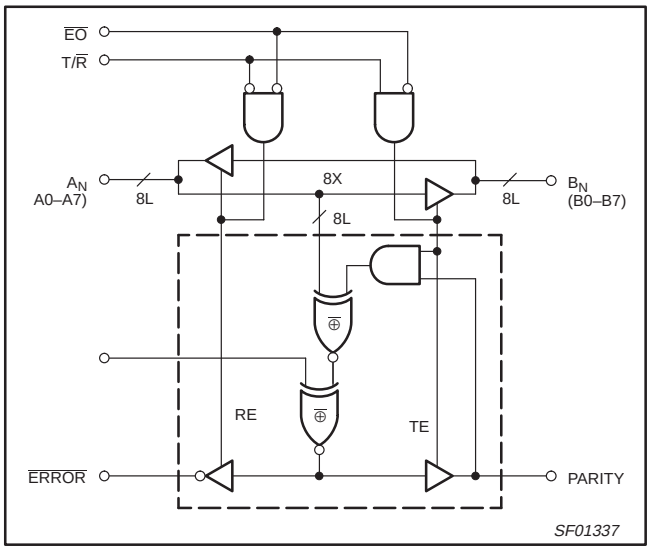

Figure 10. 74F657 Simplified Block Diagram

The 74F588 IEEE-488 Octal Transceiver

The 74F588 is a non-inverting IEEE-488 standard transceiver contains eight bidirectional 3-State buffers. The B_N port outputs can source/sink –15mA/64mA (guaranteed) and have series termination resistors as specified in the IEEE-488 specification. The A_N port, which interfaces to the PC board or system logic bus, is guaranteed to source/sink –3mA/24mA. The 74F588 pinout is identical to that of the 74F545 Octal Transceiver with the IEEE-488 termination resistors in series with the B_N port.

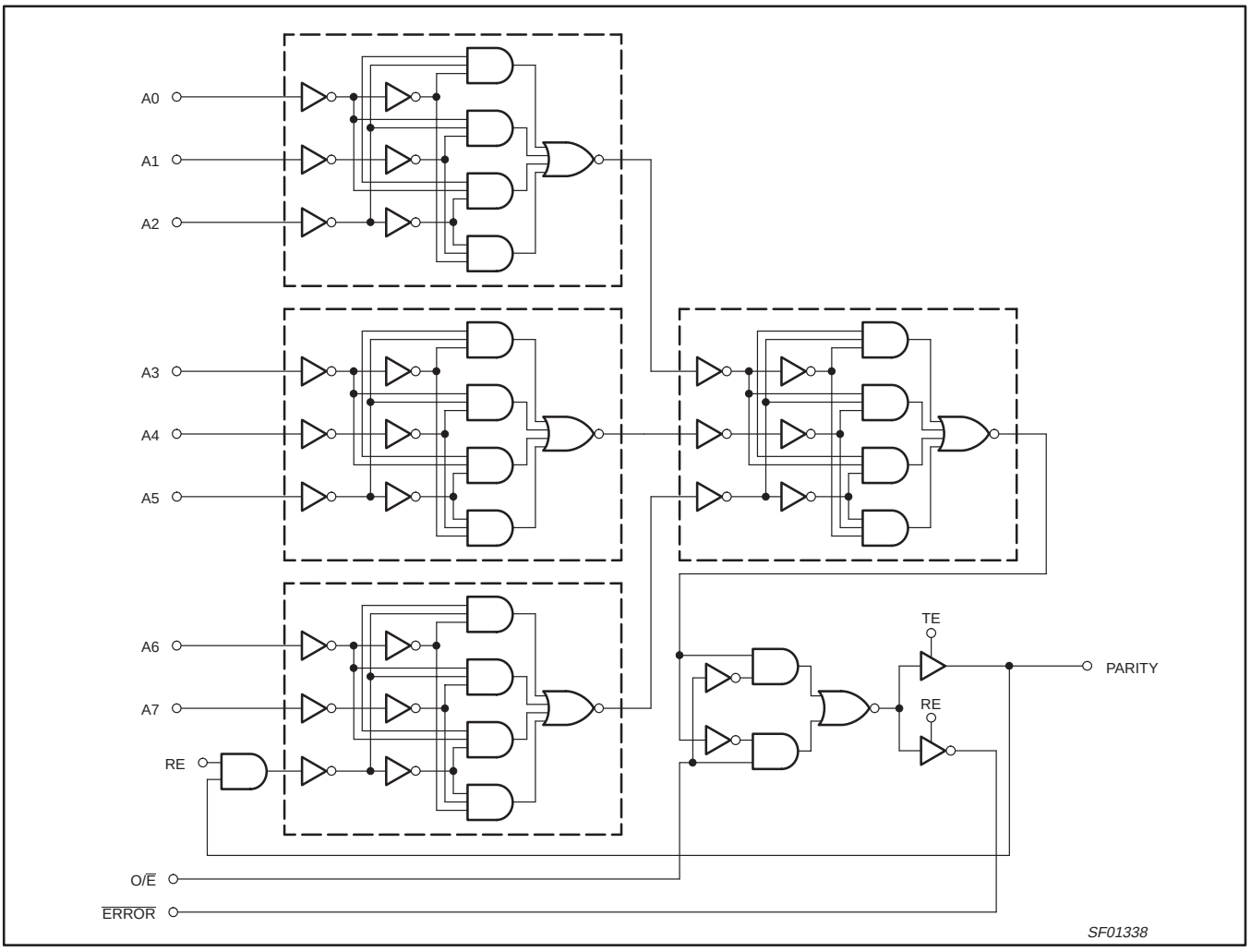

Figure 11. 74F657 Parity Tree Logic Diagram

Metastability in Latches and Registers

Interfacing a basically asynchronous real-world with synchronous logic systems can and does cause many circuit designer headaches. The problem: latches and registers which are **normally** considered to have only two stable states (High and Low) actually have a third—The METASTABLE State. This third operating point occurs when the corss-coupled latch is exactly balanced. This state is only stable when there is no noise on the chip which would tend to destabilize the perfect energy balance between the bi-stable states of the latch. Refer to Figure 12.

Metastability can occur when input data violate the setup time or hold time specifications at the clocking or strobing edge of the synchronizing clock input. With no system noise, the latch cannot decide “yes or no”, so it is possible for the latch to “go metastable” or “maybe”. With noise on the chip, random energy will “nudge” the latch toward one of its “bi-stable” states—HIGH or LOW. This metastable state time can range from nanoseconds to milliseconds. With today’s very high performance logic families, the metastable condition can last for, perhaps, 1000 times the latch’s normal propagation delay time. A metastable latch has an unpredictable delay time during which the output is between logic levels. This metastable state can easily last more than 50ns with today’s high performance logic families and WILL cause systems to “crash” if great care is not taken with asynchronous, real-world interfacing.

The D-type latch shown in Figure 12 has DATA applied to NAND gate 1 and $\overline{DATA}$ applied to NAND gate 2. When the LE (Latch Enable) input is LOW, gates 1 and 2 outputs are HIGH and the G3/4 R-S latch is latched and stable. When LE is HIGH, the latch appears to be transparent to the DATA input—Q equals DATA. On the HIGH-to-LOW transition of LE, the DATA logic level that meets the latch’s setup and hold time is stored in the latch.

If DATA changes during the setup time to hold time period, it is possible for both outputs of gates 1 and 2 to be in the input thresholds region of gates 3 and 4, respectively. Under these conditions, the latch (gates 3 and 4) could be perfectly balanced in the METASTABLE state. Eventually, chip and system noise will cause the latch to be forced into a HIGH/LOW stable state.

The Extended Octal-Puls Family, while not entirely immune, has been made metastable resistant by using design techniques which force the latch toward a stable state much more quickly than older bus interface families.

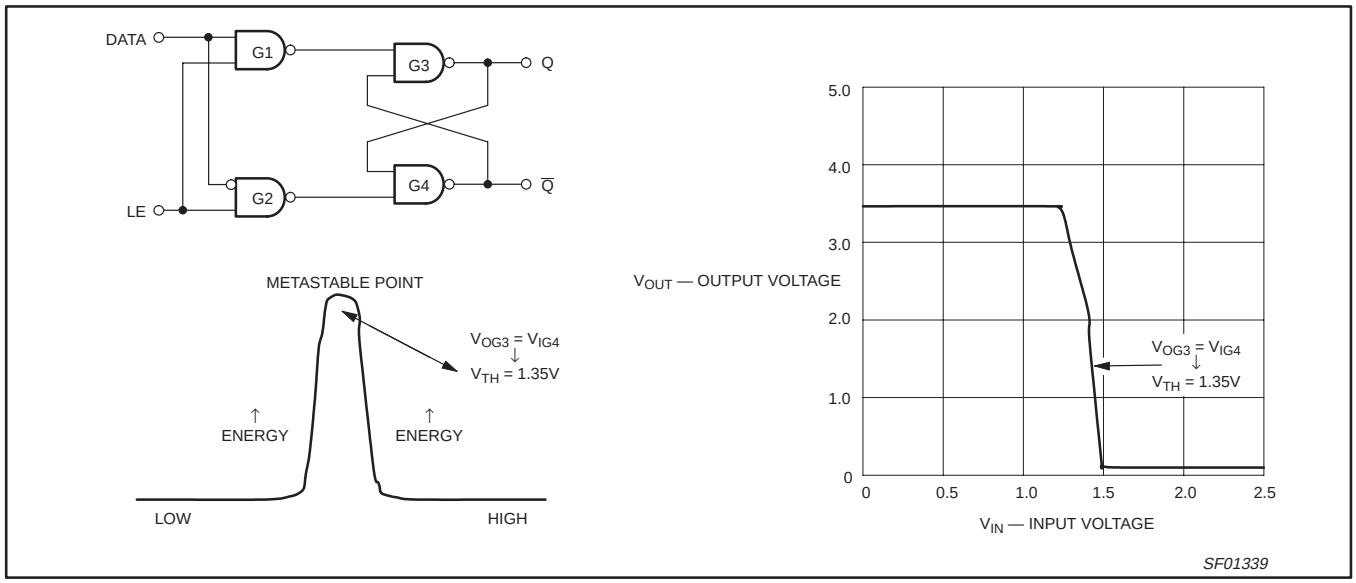

Figure 12. Metastability in Latches and Registers

Dual-Registered Transceiver Applications

Figure 13 illustrates how the 74F646A-649A and 74F651A-654A can be used to either synchronize data transfer between two systems, or pipeline data. Data is stored in a register, then, while retrieving more data, the first data is read. When the second is available, it can either be stored or read directly. Two slower systems can be multiplexed into a high speed system in the same way.

Parity Bus Transceiver Applications

Figure 14 illustrates the functional density advantages of the Parity Bus Series using the 74F657 in a typical microprocessor/data bus transceiver application. Note the 74F245 + 74F280B version would still require a 2-input AND gate and 3-State buffers for the PARITY and $\overline{\text{ERROR}}$ outputs. And, of course, it would require an order of magnitude higher input current than a single 74F657 would, and would also introduce much higher capacitive loading (for both the bus and the microcontroller).

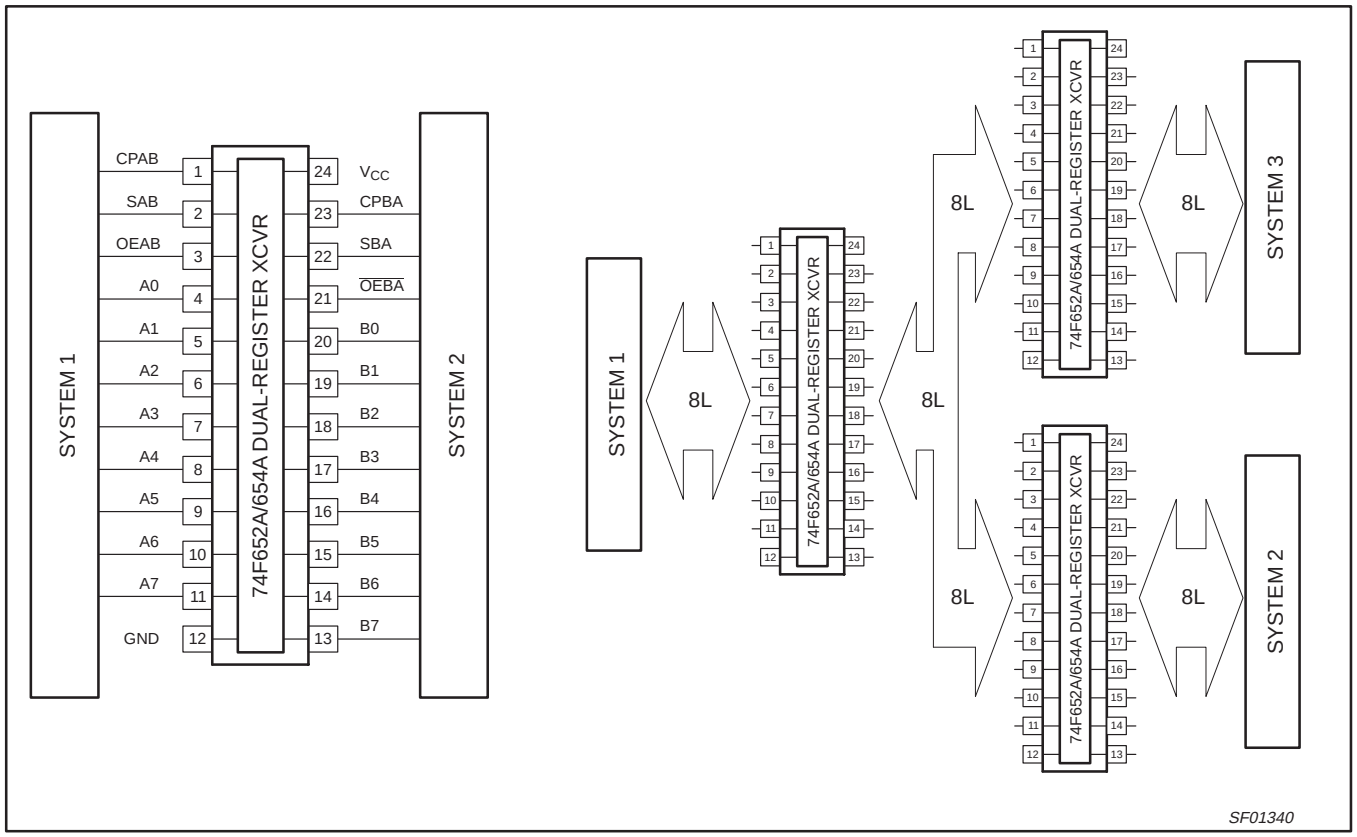

Figure 13. 74F Extended Octal-Plus Dual-Registered Transceiver Applications

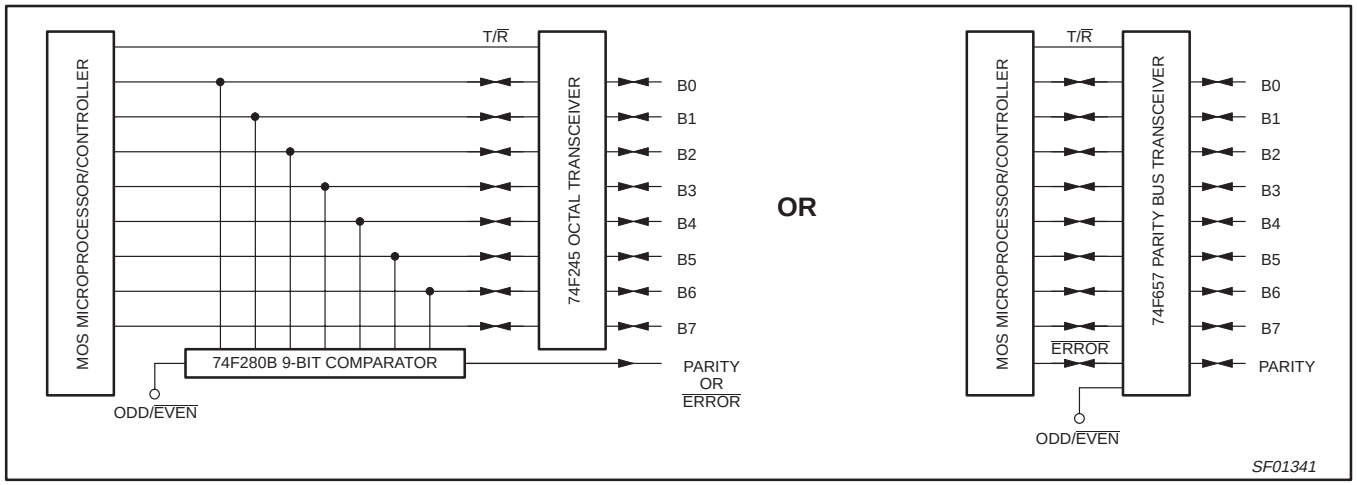

Figure 14. 74F657 Parity Bus Transceiver Applications

Table 3. The Extended Octal-Plus Family Capabilities Summary

Part Number	# Bits	Polarity	Output	Broad-side	I_{OH}/I_{OL} MIN	Storage	Speed	Parity	Comments
"Light-Load" buffer and Line Driver Functions									
74F455/456	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Multiple/Ctr Pkg. GND Pins, Σ_E, Σ_O = –15/64mA
74F540/541	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	No	Broadside pinout of 74F240
74F655A/656A	8-bit	INV/NINV	3-St	Yes	–15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = –15/64mA
74F827/828	10-bit	NINV/INV	3-St	Yes	–15/64mA	None	9.0ns	No	
"Light-Load" Register and Latch Functions									
74F821/822	10-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F823/824	9-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F825/826	8-bit	NINV/INV	3-St	Yes	–15/64mA	Reg	100MHz	No	Data, $\overline{MR}$, OE, & Clock EN Inputs
74F841/842	10-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
74F843/844	9-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
74F845/846	8-bit	NINV/INV	3-St	Yes	–15/48mA	Latch	100MHz	No	Data, $\overline{MR}$, OE, & LE Enable Inputs
"Light-Load" Transceiver Functions									
74F545	8-bit	NINV	A_N 3-St B_N 3-St	Yes Yes	–3/24mA –15/64mA	None None	7.0ns 7.0ns	No No	
74F550/551	8-bit	NINV/INV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	B_N-Reg A_N-Reg	10.5ns 10.5ns	No No	$A_N \rightarrow B_N$, ERROR, status registers, 50MHz $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins **
74F552	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	B_N-Reg A_N-Reg	10.5ns 10.5ns	Yes Yes	$A_N \rightarrow B_N$, PARITY, $\overline{ERROR}$, status registers $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins **
74F588	8-bit	NINV	A_N = 3-St B_N 3-St	Yes Yes	–3/24mA –15/64mA	None None	7.5ns 7.5ns	No No	 IEEE-488/GPIB w/line term. resistors
74F620/623	8-bit	INV/NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	7.5ns 7.5ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F621/622	8-bit	NINV/INV	B_N OC A_N OC	Yes Yes	OC/64mA OC/24mA	None None	13.0ns 12.5ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F640	8-bit	INV	A/B 3-St	Yes	–15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/642	8-bit	NINV/INV	B_N OC A_N OC	Yes Yes	OC/64mA OC/20mA	None None	13.0ns 12.0ns	No No	$A_N \rightarrow B_N$ $B_N \rightarrow A_N$
74F646A/648A	8-bit	NINV/INV	A/B 3-St	Yes	–15/48mA	2 Reg	11.0ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.)
74F647/649	8-bit	NINV/INV	AB OC	Yes	OC/64mA	2 Reg	19.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 40MHz (min.)
74F651A/652A	8-bit	INV/NINV	A/B 3-St	Yes	–15/48mA	2 Reg	11.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.)
74F653/654	8-bit	NINV/INV	B_N 3-St A_N OC	Yes Yes	–15/64mA OC/64mA	B_N-Reg A_N-Reg	11.0ns 20.0ns	No No	$A_N \rightarrow B_N$, B_N port = 85MHz (min.) $B_N \rightarrow A_N$, A_N port = 45MHz (min.)
74F657	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	8.0ns 8.0ns	Yes No	$A_N \rightarrow B_N$, PARITY, $\overline{ERROR}$ = –15/64mA $B_N \rightarrow A_N$, Multiple/Center Pkg. GND pins
74F861/862	10-bit	NINV/INV	A/B 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/864	9-bit	NINV/INV	A/B 3-St	Yes	–15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1245	8-bit	NINV	B_N 3-St A_N 3-St	Yes Yes	–15/64mA –3/24mA	None None	8.0ns 8.0ns	No No	$A_N \rightarrow B_N$, "Light-Load" pin-for-pin 'F245 replacement $B_N \rightarrow A_N$
74F2951/2952	8-bit	INV/NINV	A/B 3-St	Yes	–15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, registers for A_N & B_N ports, 80MHz (min.) **

NOTES:
All parameters are worst-case, unless otherwise specified.
3-St = 3-State
OC = Open Collector
Reg = LOW-to-HIGH edge clocked D-type register
Latch = HIGH logic level on the Latch Enable logic, data passes directly through D-type latch, HIGH-to-LOW logic level transition of the Latch Enable, data is stored in the D-type latch.
** = These devices utilize standard FAST input structures producing input currents of +20µA and –0.6mA.
$\overline{MR}$ = $\overline{Master\ Reset}$
OE = Output Enable

74F extended octal-plus family applications AN214

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