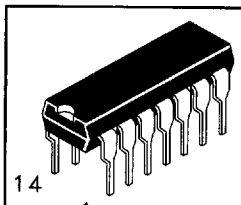
Available Q2, 1995

Dual 4-Bit Binary Counter

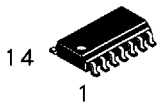
DV74HC393

This Device contains a pair of high-speed 4-stage ripple counters. Each half of this device operates a 16 bit binary divider with the last three stages triggered in a ripple fashion. The flip-flops are triggered by a High-to-Low transition of the clock inputs. Each half of each circuit has Reset input which responds to a High signal by forcing all four outputs to LOW state.

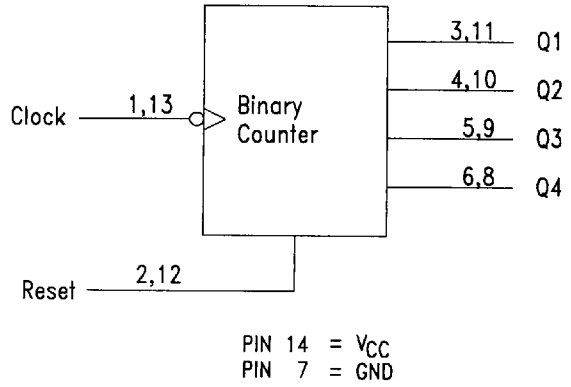
- **Output Drive Capability: 10 LSTTL Loads**
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V**
- **Low Input Current: 1 μA**
- **DC, AC parameters guaranteed from -55°C to 125°C**

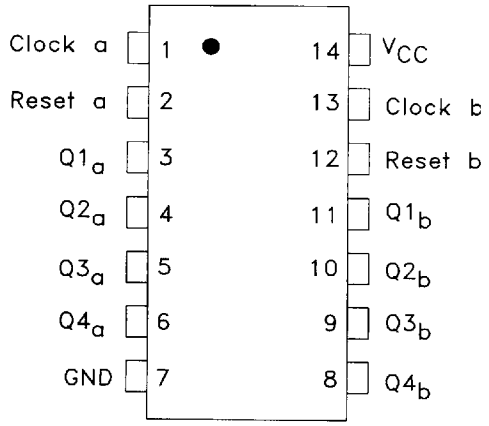


N Suffix
Plastic DIP
AVG-001 Case



D Suffix
Plastic SOP
AVG-002 Case





TRUTH TABLE				
Count	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H=High Level Logic
L=Low Level Logic

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ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP SOP Package	750 500	mW
T_{STG}	Storage Temperature Range	−65 to +150	oC
TL	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Ambient Temperature	−55	+125	°C
t_r, t_f	Input Rise and Fall Time: HC: V_{CC}=2.0V HCT: V_{CC}=5.5V / HC: V_{CC}=4.5V HC: V_{CC}=6.0V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} V	Guaranteed Limits			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} =0.1 V, $|I_{OUT}|\leq$20μA or V_{OUT} = V_{CC}−0.1V	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT} =0.1 V, $|I_{OUT}|\leq$20μA or V_{OUT} = V_{CC}−0.1V	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|\leq$ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|\leq$ 4.0mA $\|I_{OUT}\|\leq$ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|\leq$ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|\leq$ 4.0mA $|I_{OUT}|\leq$5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA (Per Package)	6.0	8.0	80	160	μA

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AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50 pF, Input t_f=t_r=6ns)

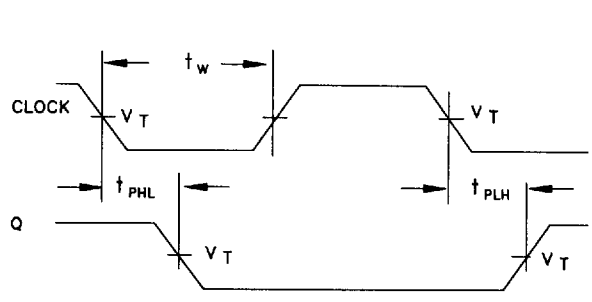
Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	2.0 4.5 6.0	5.4 27 32	4.4 22 26	3.6 18 21	MHz
t_{PLH} t_{PHL}	Maximum Propagation Delay Time, Clock to Q1	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay Clock to Q2	2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay Clock to Q3	2.0 4.5 6.0	240 48 41	300 60 51	360 72 61	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay Clock to Q4	2.0 4.5 6.0	290 58 49	365 73 62	435 87 74	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q	2.0 4.5 6.0	165 33 28	205 41 62	250 50 43	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	—	10	10	10	pF

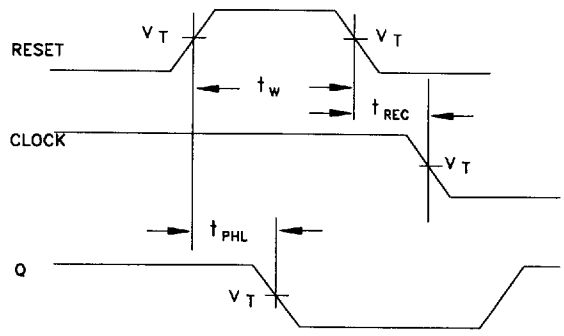
C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C. V_{CC} = 5.0 V 40	pF

TIMING REQUIREMENTS (Input t_r=t_f =6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time Rest Inactive to Clock	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width Clock	2.0 4.5 6.0	80 60 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width Reset	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns

SWITCHING WAVEFORMS





Input and Output Threshold Voltage, V_T=50% V_{CC}
V_H=V_{CC}

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