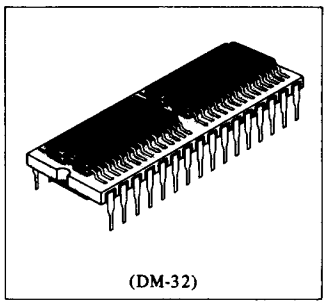
131072-word x 8-bit High Density Static RAM Module

Features

- High Density Industry Standard 32 Pin DIP Mounting 4pcs of 256k Static RAM (SOP).
- Single +5V Supply.
- High speed: Fast Access Time 100/120/150ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- Low Power
  Standby: 40μW typ. (L-version)
  Operation: 50mW typ. (f = 1MHz)
- Capability of Battery Back-up Operation (L-version).
- Common Data Input and Output, Three State Outputs.
- Directly TTL Compatible: All Inputs and Outputs.

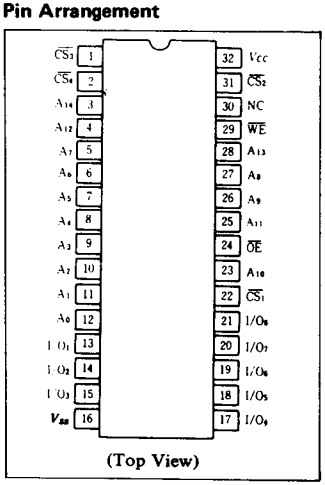


(DM-32)

Ordering Information

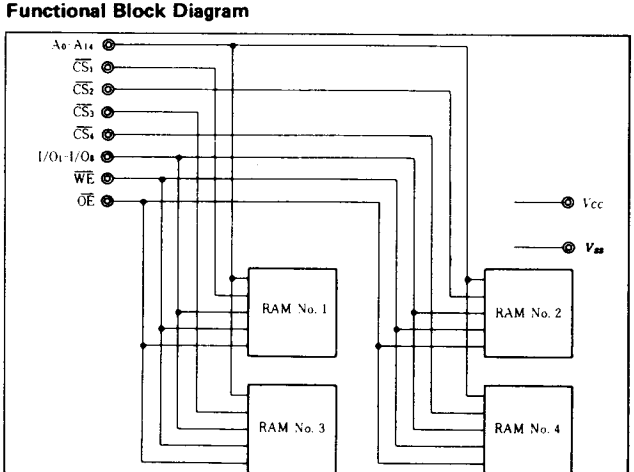
Type No.	Access Time	Package
HM66203-10	100ns	600 mil 32 pin DIP
HM66203-12	120ns	
HM66203-15	150ns	
HM66203L-10	100ns	
HM66203L-12	120ns	
HM66203L-15	150ns	

Pin Arrangement



(Top View)

Functional Block Diagram



Truth Table

Mode	$\overline{CSi}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not Selected (Power Down)	H*1	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L*2	H	L	D_{out}	I_{CC}	Read Cycle (1) to (3)
Write	L*2	L	H	D_{in}	I_{CC}	Write Cycle (1)
	L*2	L	L	D_{in}	I_{CC}	Write Cycle (2)

Note) *1. X: Don't Care (H or L); i = 1, 2, 3, 4 All chips are not selected.
*2. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding.
Only one chip should be selected.
Two or more chips must not be selected at one time.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.0V for pulse width ≦ 50ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min.	typ. *1	max.	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CSn}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2	μA	*2
Operating Power Supply Current: DC	I_{CC}	$\overline{CSN}$ = V_{IL} $I_{I/O}$ = 0mA	–	10	25	mA	*3
Average Operating Power Supply Current (1)	I_{CC1}	MIN. cycle	–	42	80	mA	HM66203/L −10
		duty = 100%	–	37	80		HM66203/L −12
		$I_{I/O}$ = 0mA	–	35	80		HM66203/L −15
Average Operating Power Supply Current (2)	I_{CC2}	$\overline{CSN}$ = V_{IL} V_{IH} = V_{CC} V_{IL} = 0V $I_{I/O}$ = 0mA f = 1MHz	–	10	15	mA	*3
Standby Power Supply Current: DC	I_{SB}	$\overline{CSn}$ = V_{IH}	–	2	12	mA	*2
Standby Power Supply Current (1): DC	I_{SB1}	$\overline{CSn}$ ≧ V_{CC} − 0.2V	–	8	400	μA	HM66203L Series
			–	0.16	8	mA	HM66203 Series
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V	

Note) *1. Typical values are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
*2. $\overline{CSn}$; All chips are not selected.
*3. $\overline{CSN}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	45	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	50	pF

Note) This parameter is sampled and not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

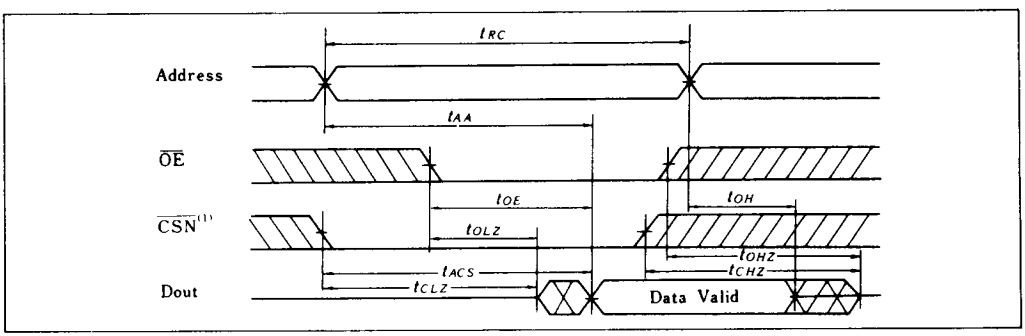
AC Test Conditions

- Input pulse levels . . . . . 0.8V to 2.4V
- Input rise and fall times 5ns
- Input and Output timing reference level 1.5V
- Output load . . . . . 1 TTL Gate and C_L (100pF) (Including scope & jig)

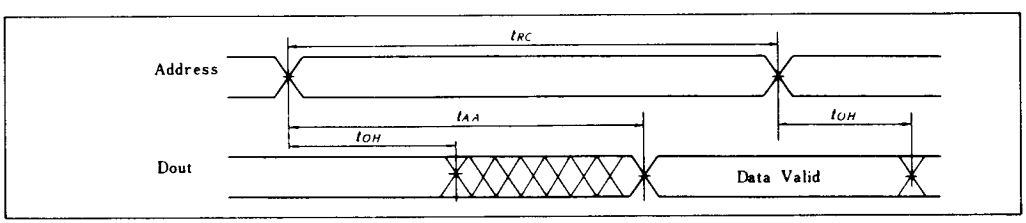
Read Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

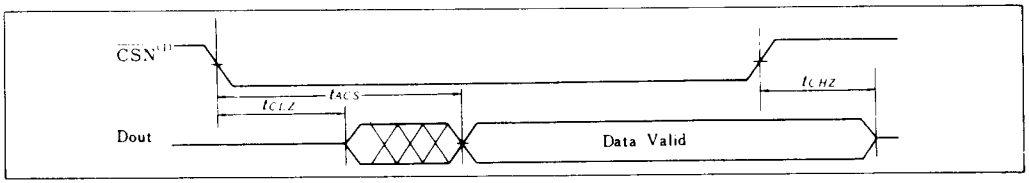
Timing Waveform of Read Cycle No. 1 *2



Timing Waveform of Read Cycle No. 2 *1,*2,*3,*5



Timing Waveform of Read Cycle No. 3 *2,*4,*5

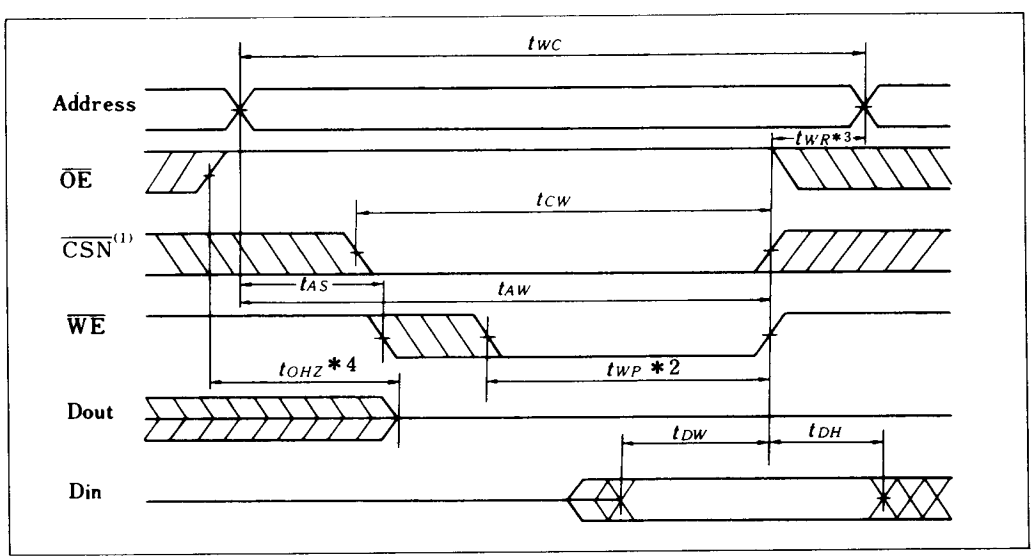


Note) *1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CSN} = V_{IL}$.
*4. Address should be valid prior to or coincident with $\overline{CSN}$ transition low.
*5. $\overline{OE} = V_{IL}$

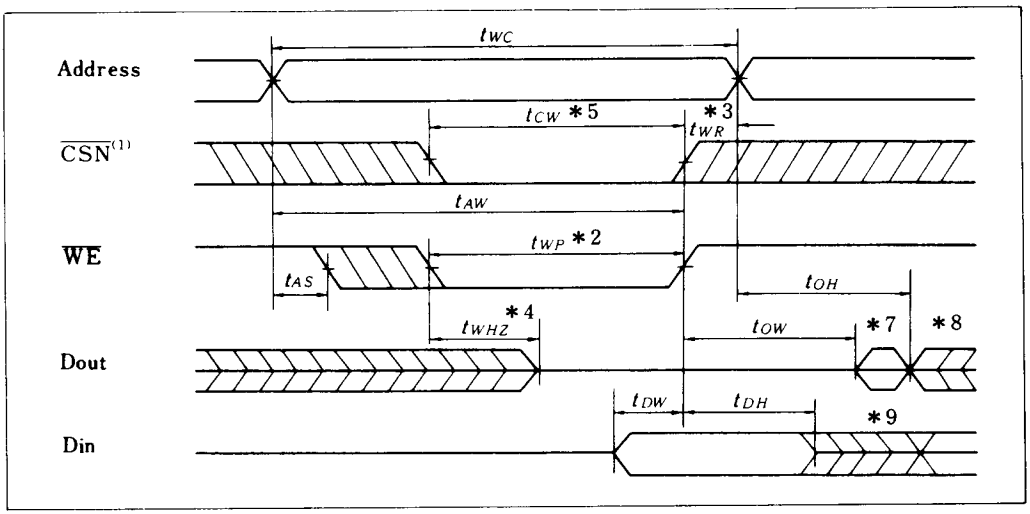
Write Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	90	–	100	–	120	–	ns
Address Valid to End of Write	t_{AW}	90	–	100	–	120	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	75	–	90	–	110	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ Low Fixed)*6



Notes)
*1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CSN}$ and a low $\overline{WE}$.
*3. t_{WR} is measured from the earlier of $\overline{CSN}$ or $\overline{WE}$ going high to the end or write cycle.
*4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
*5. If the $\overline{CSN}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*7. Dout should be held in phase of the written data during this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CSN}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

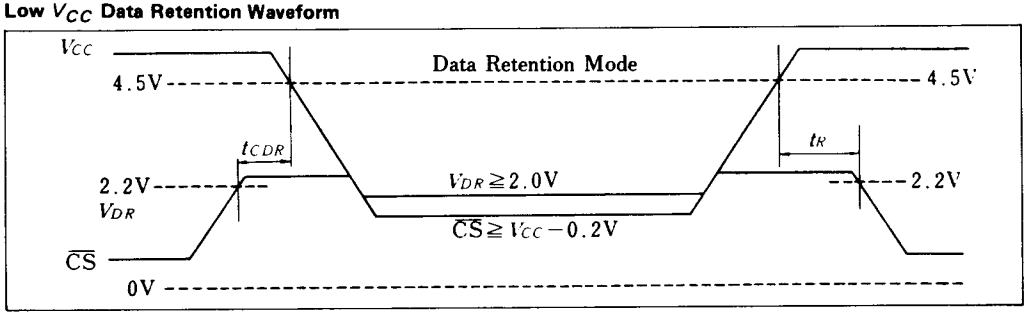
Low V_{CC} Data Retention Characteristics (T_a = 0°C to +70°C)

(Data retention characteristics is guaranteed only for HM66203L Series.)

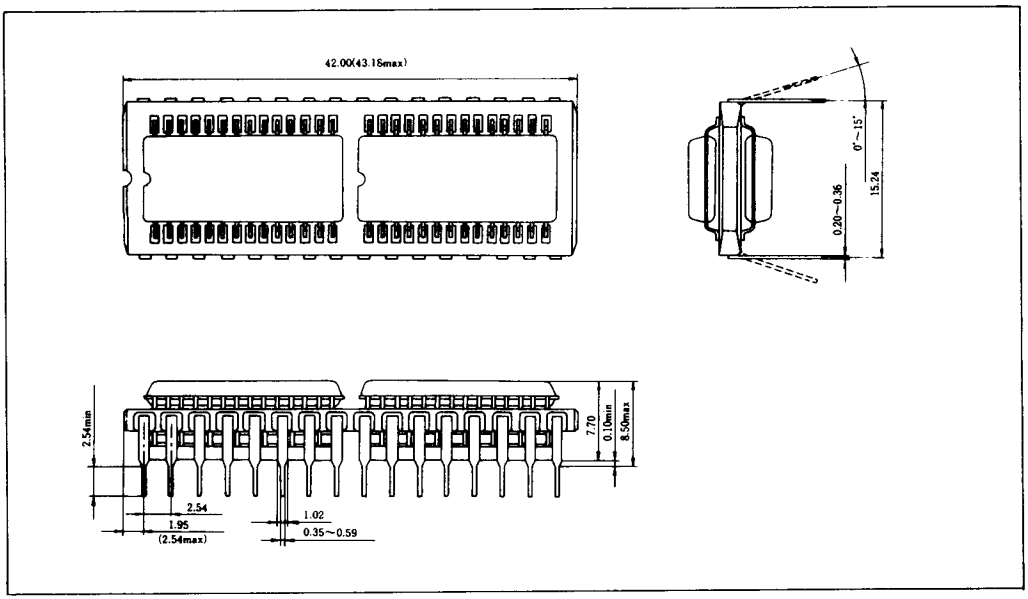
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CSn} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCDR}	–	–	200	µA	V_{CC} = 3.0V $\overline{CSn} \geqq 2.8V$*2
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	[1] t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.
*2. CSn: All chips are not selected.

Low V_{CC} Data Retention Waveform



Package Outline (Unit: mm)



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