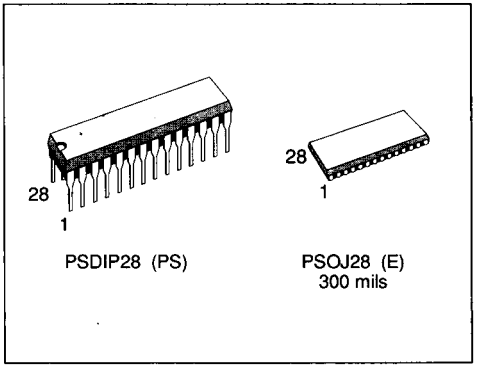
VERY FAST CMOS 8K x 8 SRAM WITH OUTPUT ENABLE

- 8K x 8 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 10, 12, 15, 20ns
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mils PACKAGES



PSDIP28 (PS)

PSOJ28 (E)
300 mils

DESCRIPTION

The M628008 is a 64K (65,536 bit) Fast CMOS SRAM, organized as 8,192 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

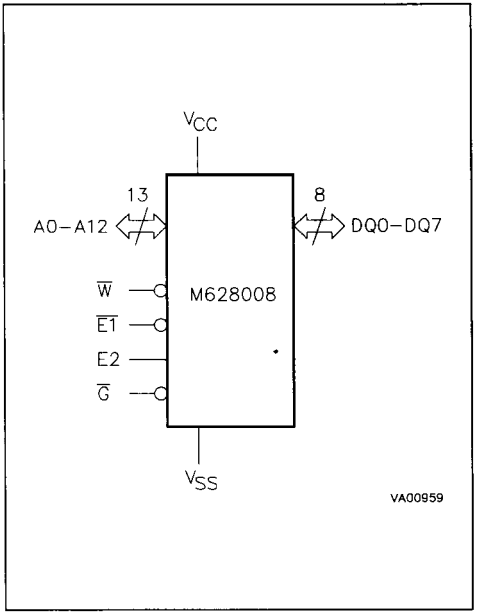
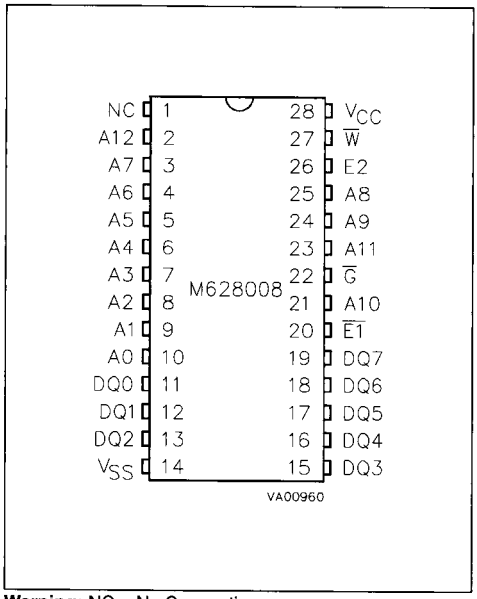


Table 1. Signal Names

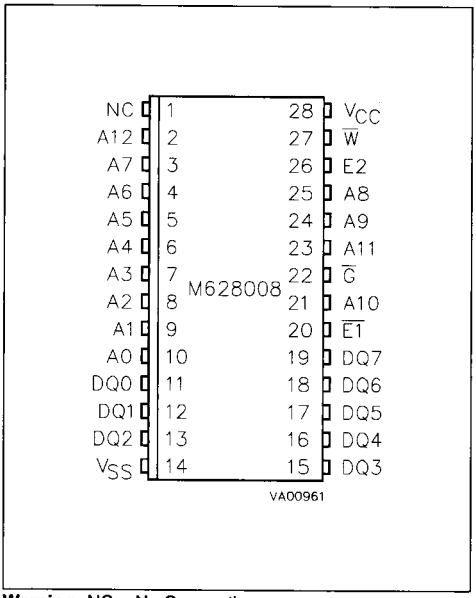
A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SDIP Pin Connections



Warning: NC = No Connection.

Figure 2B. SOJ Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M628008 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low, with both Chip Enables ($\overline{E1}$ and E2) asserted. This provides access to data from eight of the 65,536 locations in the static memory array, specified by the 13 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and Chip Enables are valid. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M628008 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low with E2 High. Chip Enables $\overline{E1}$, E2 or $\overline{W}$ must be deasserted during Access transitions for subsequent write cycles. Write begins with the concurrence of the two Chip Enables being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVE1L}, t_{AVE2H} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$ or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ Low, E2 High and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M628008 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ High or E2 Low). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E1}$, E2, as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

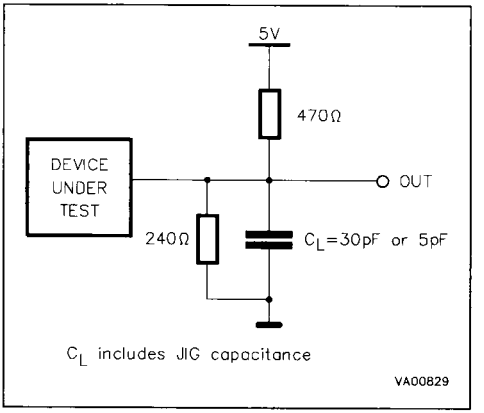


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-10 & -12)		140	mA
		V_{CC} = 5.5V, (-15 & -20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, f = 0		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E1} \ge V_{CC} - 0.3V$ or E2 ≤ 0.3V, f = 0		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628008								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	10		12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		10		12		15		20	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		10		12		15		20	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		10		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		5		7		8		10	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	3		3		3		3		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	3		3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns

Notes: 1. C_L = 30pF
2. C_L = 5pF

Figure 4. Read Mode AC Waveforms

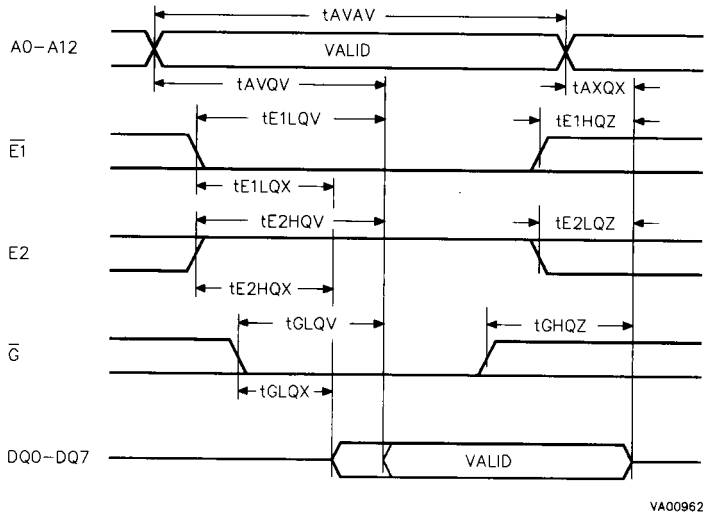


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628008								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	10		12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	10		12		15		20		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	10		12		15		20		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	10		12		15		20		ns
t_{WLWH}	Write Enable Pulse Width	10		12		15		20		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	7		9		10		15		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	7		9		10		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	5		7		8		10		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	5		7		8		10		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	5		7		8		10		ns

Note: 1. C_L = 5pF

Figure 5. Write Enable Controlled, Write AC Waveforms

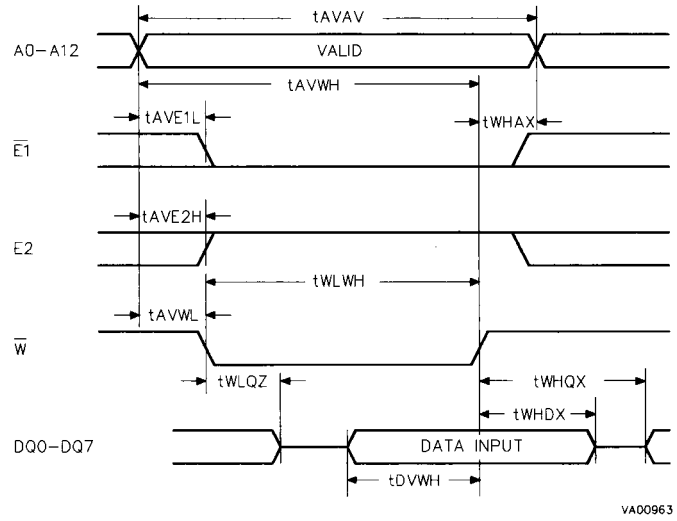
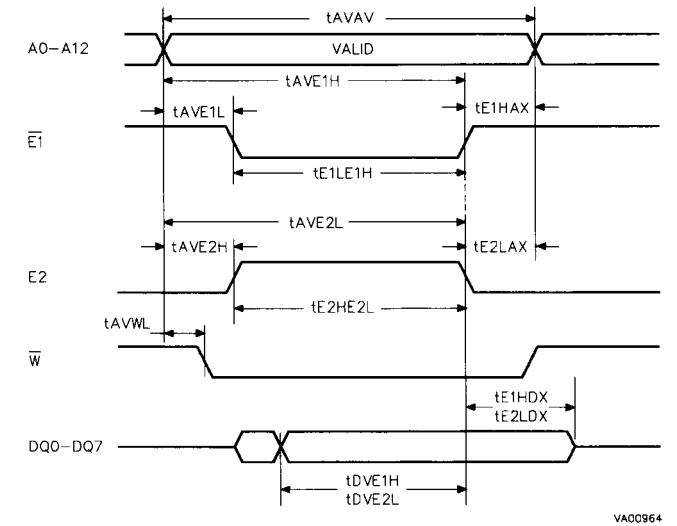
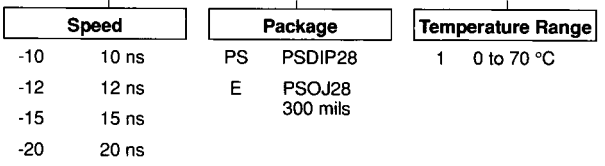


Figure 6. Chip Enable Controlled, Write AC Waveforms



ORDERING INFORMATION

Example: M628008 -10 E 1



Speed		Package		Temperature Range	
-10	10 ns	PS	PSDIP28	1	0 to 70 °C
-12	12 ns	E	PSOJ28 300 mils		
-15	15 ns				
-20	20 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.