ON Semiconductor®

Timing-Safe™ Peak EMI Reduction IC

General Features

- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 20MHz - 50MHz
- Multiple low skew Timing-safe™ Outputs:
  - P3P623S05: 5 Outputs
  - P3P623S09: 9 Outputs
- Supply Voltage: 3.3V±0.3V
- Packaging Information:
  - P3P623S05: 8 pin TSSOP
  - P3P623S09:16 pin TSSOP
- True Drop-in Solution for Zero Delay Buffer

Functional Description

P3P623S05/09 is a versatile, 3.3V Zero-delay buffer designed to distribute Timing-Safe™ clocks with Peak EMI reduction. P3P623S05 is an eight-pin version, accepts one reference input and drives out five low-skew Timing-Safe™ clocks. P3P623S09 accepts one reference input and drives out nine low-skew Timing-Safe™ clocks.

All parts have on-chip PLLs that lock to an input clock on the CLKIN pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad, internal to the device.

Multiple P3P623S05 / P3P623S09 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 700pS.

All outputs have less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than ±350pS, and the output-to-output skew is guaranteed to be less than 250pS.

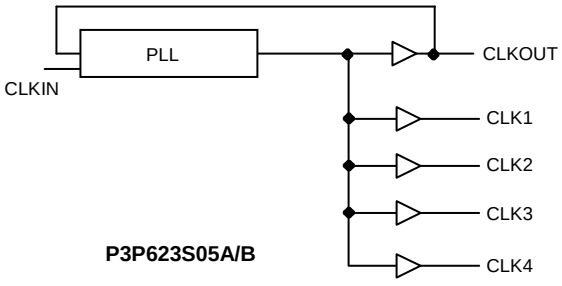
Refer "Spread Spectrum Control and Input-Output Skew Table" for deviations and Input-Output Skew for P3P623S05A/B and P3P623S09A/B devices.

P3P623S05/09 operates from a 3.3V supply and is available in TSSOP package, as shown in the ordering information table.

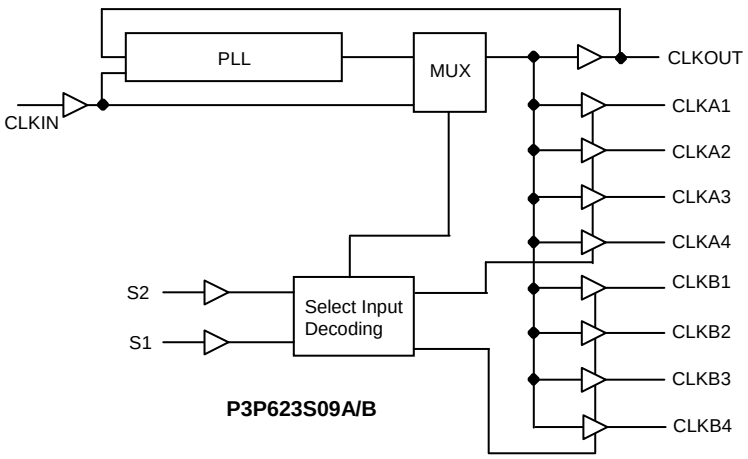
Application

P3P623S05/09 is targeted for use in Displays and memory interface systems.

General Block Diagram



P3P623S05A/B



P3P623S09A/B

July 2010 – Rev. 1

Publication Order Number:
P3P623S05/D

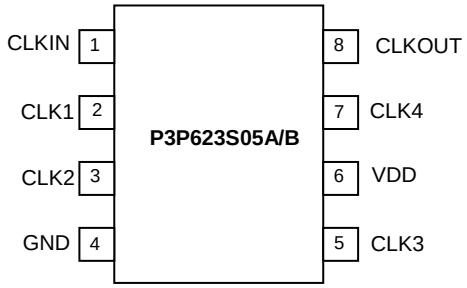
Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The P3P623S05/09 uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration for P3P623S05A/B

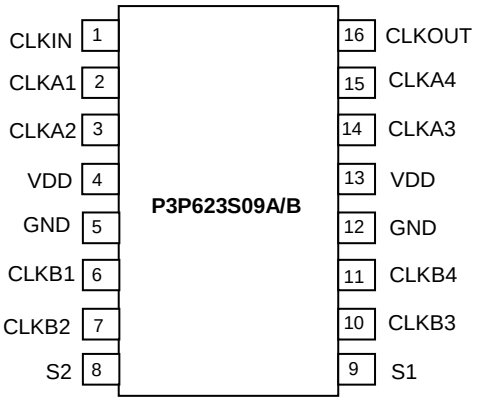


Pin Description for P3P623S05A/B

Pin #	Pin Name	Type	Description
1	CLKIN[1]	I	External reference Clock input, 5V tolerant input
2	CLK1[2]	O	Buffered clock output[4]
3	CLK2[2]	O	Buffered clock output[4]
4	GND	P	Ground
5	CLK3[2]	O	Buffered clock output[4]
6	VDD	P	3.3V supply
7	CLK4[2]	O	Buffered clock output[4]
8	CLKOUT[4]	O	Buffered clock output.Internal feedback on this pin.

Notes:
1. Weak pull down
2. Weak pull-down on all outputs
3. Weak pull-up on these Inputs
4. Buffered clock output is Timing-Safe™

Pin Configuration for P3P623S09A/B



Pin Description for P3P623S09A/B

Pin #	Pin Name	Pin Type	Description
1	CLKIN[1]	I	External reference Clock input, 5V tolerant input
2	CLKA1[2]	O	Buffered clock Bank A output[4]
3	CLKA2[2]	O	Buffered clock Bank A output[4]
4	VDD	P	3.3V supply
5	GND	P	Ground
6	CLKB1[2]	O	Buffered clock Bank B output[4]
7	CLKB2[2]	O	Buffered clock Bank B output[4]
8	S2[3]	I	Select input, bit 2. See *Select Input Decoding table for P3P623S09A/B* for more details
9	S1[3]	I	Select input, bit 1. See *Select Input Decoding table for P3P623S09A/B* for more details
10	CLKB3[2]	O	Buffered clock Bank B output[4]
11	CLKB4[2]	O	Buffered clock Bank B output[4]
12	GND	P	Ground
13	VDD	P	3.3V supply
14	CLKA3[2]	O	Buffered clock Bank A output[4]
15	CLKA4[2]	O	Buffered clock Bank A output[4]
16	CLKOUT[2]	O	Buffered clock output.Internal feedback on this pin.

Notes:
1. Weak pull down
2. Weak pull-down on all outputs
3. Weak pull-up on these Inputs
4. Buffered clock output is Timing-Safe™

Select Input Decoding table for P3P623S09A/B

S2	S1	CLK A1 - A4	CLK B1 - B4	CLKOUT[1]	Output Source	PLL Shut-Down
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Note1: This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the Output

Spread Spectrum Control and Input-Output Skew Table

Frequency (MHz)	Device	Deviation (±%)	Input-Output Skew (±T_{SKEW})
32	P3P623S05A / 09A	0.25	0.125
	P3P623S05B / 09B	0.5	0.25

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	-0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	-0.5 to +7	
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	℃
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage[5]				0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8mA			0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = -8mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs		15		mA
Z_o	Output Impedance			23		Ω

Notes: 5. CLKIN input has a threshold voltage of VDD/2
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

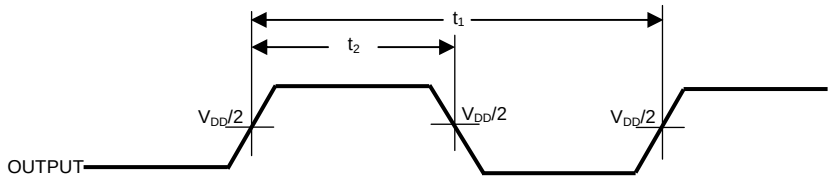
Switching Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Frequency		20		50	MHz
Output Frequency	30pF load	20		50	MHz
Duty Cycle [7,8] = (t_2 / t_1) * 100	Measured at VDD/2	40	50	60	%
Output Rise Time [7, 8]	Measured between 0.8V and 2.0V			2.5	nS
Output Fall Time [7, 8]	Measured between 2.0V and 0.8V			2.5	nS
Output-to-output skew [7, 8]	All outputs equally loaded			250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge [8]	Measured at VDD /2			±350	pS
Device-to-Device Skew [8]	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
Cycle-to-Cycle Jitter [7, 8]	Loaded outputs			±200	pS
PLL Lock Time [8]	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

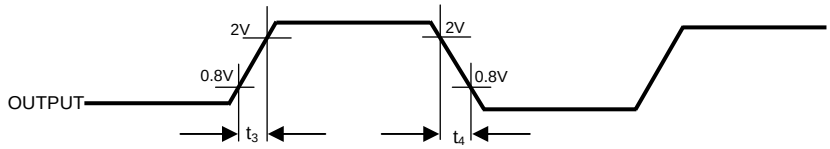
Notes: 7. All parameters specified with 30pF loaded outputs.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

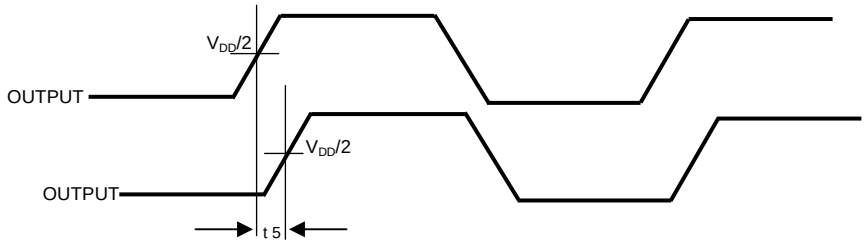
Duty Cycle Timing



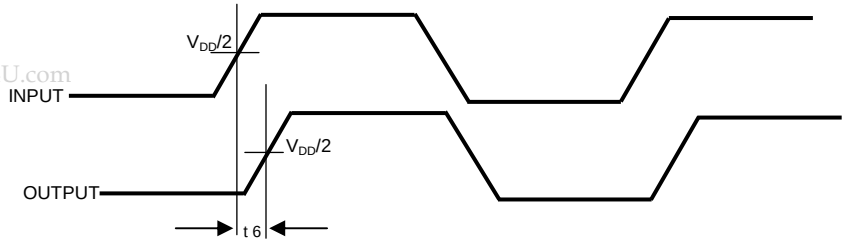
All Outputs Rise/Fall Time



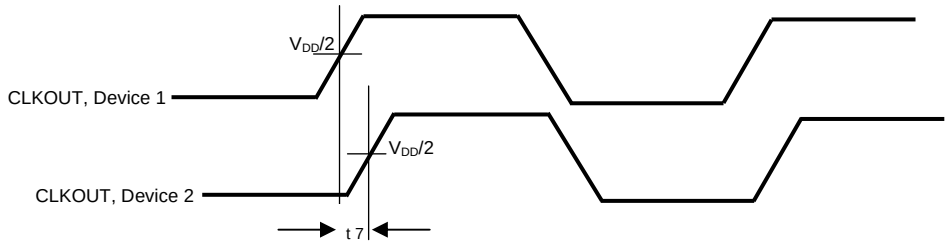
Output - Output Skew



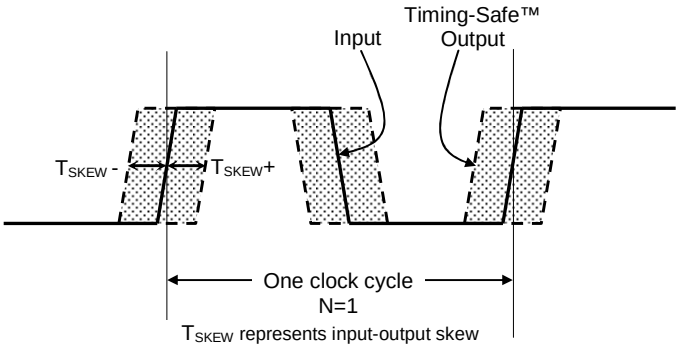
Input - Output Propagation Delay



Device - Device Skew

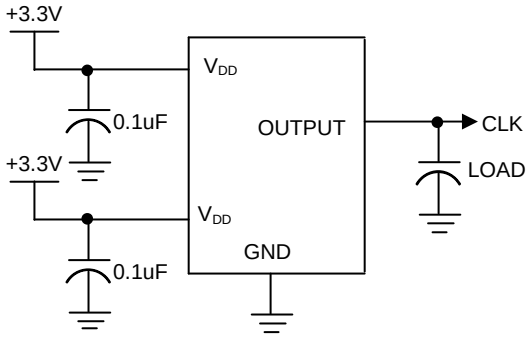


Input - Output Skew

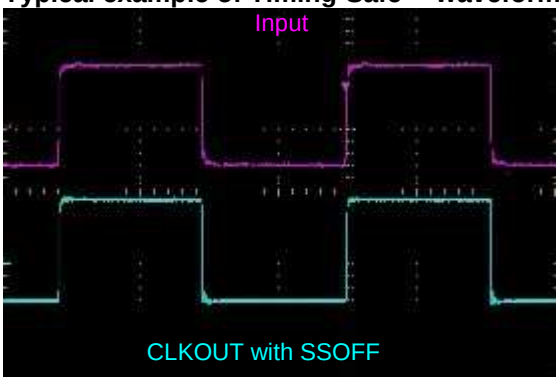


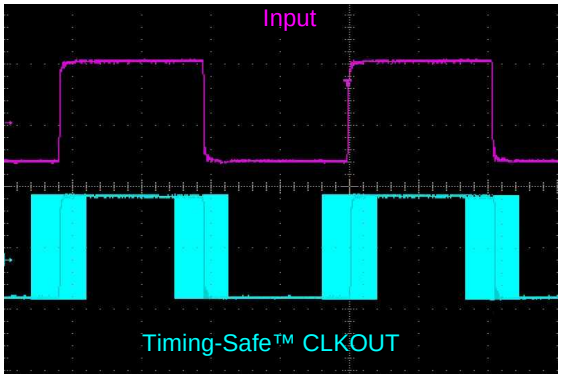
T_{SKEW} represents input-output skew when spread spectrum is ON
For example, T_{SKEW} = ± 0.125 for an Input clock12MHz, translates in to (1/12MHz) * 0.125=10.41nS

Test Circuit



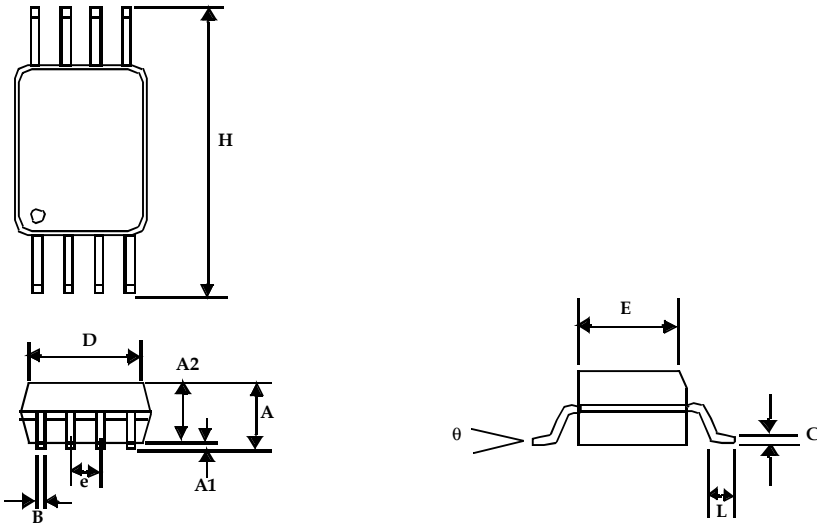
Typical example of Timing-Safe™ waveform





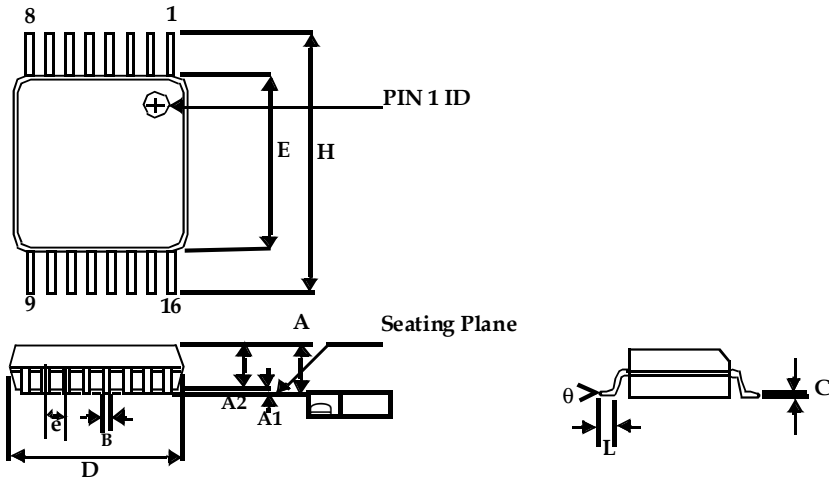
Package Information

8-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

16-lead TSSOP (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

Ordering Code

Ordering Code	Marking	Package Type	Temperature
P3P623S05BG-08TR	ADQ	8-pin 4.4-mm TSSOP – Tape & Reel, Green	0℃ to +70°

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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