APPLICATION NOTE

DRIVE CIRCUIT FOR INTEGRATION WITH IGBTS

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ABSTRACT

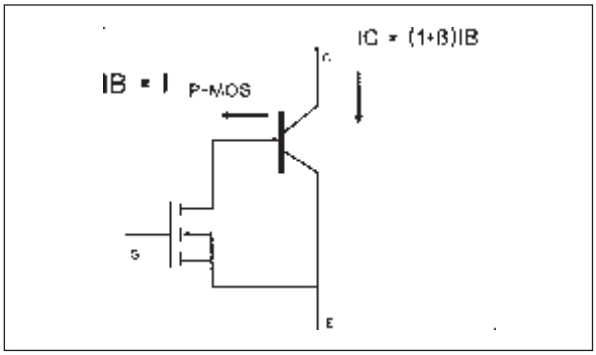
IGBT devices are increasingly used in power electronic equipment due their high power handling capability. The present paper deals with the problems that concern the turn-on, turn-off and short-circuit of these devices. An optimal new driving circuit is proposed that gives excellent device output performance. Experimental oscillogram traces of transient condition tests are given, which clearly demonstrate the advantages of using the new driving circuit. Finally, the suitability of the driving circuit for integration is analysed.

1. INTRODUCTION

Recent developments in industrial power electronic applications have demanded a concerted effort be made to produce new electronic devices, able to handle high currents, voltages and frequencies, as well as being easy to control. Among the innovative new electronic products, IGBTs are increasingly used in high voltage applications, > 500V up to frequencies of 20kHz to 30kHz. Essentially IGBT components have the following characteristics:

- Both turn-on and turn-off capability by means of an applied voltage to the gate requiring only low driving power, equivalent to that which is required by MOSFET structures.
- Low direct voltage drop and high current density like BJT devices.

Figure 1. Simplified equivalent circuit of an IGBT



The former is a very important point because it implies a loss reduction, hence costs decrease in making the driving stage, while the latter makes it suitable for high current applications.

IGBT structures can be represented by means of a simplified circuit using two devices, a MOSFET and a BJT, as shown in Figure 1. IGBTs are very “user-friendly” to drive, but in order to obtain the best performance they require suitable driving techniques [1] [2].

In this paper the most important phenomena occurring during the switching are discussed, with the aim of analysing and optimising the IGBT behaviour. In particular, an original driving circuit is proposed able to function during turn-on, turn-off and short-circuit conditions and is a powerful tool for improving IGBT performance. Moreover, the proposed driving circuit provides suitable protection for avoiding switch failure during stress conditions.

Extensive laboratory tests have been carried out to demonstrate the advantages of the new driving circuit in comparison to the more traditional ones.

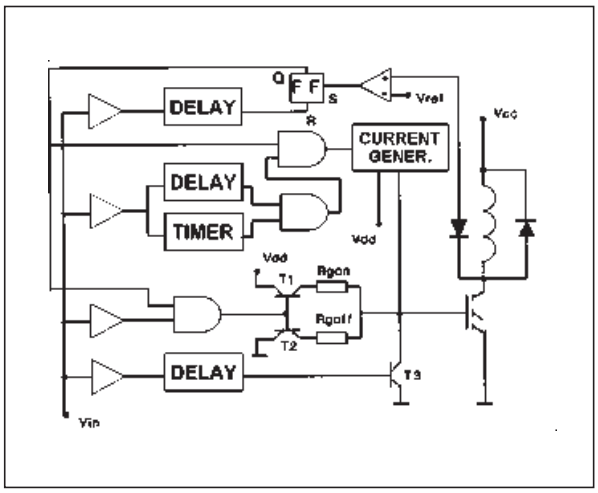
2. THE DRIVING CIRCUIT

The proposed circuit, shown in Figure 2, can be ideally split in three main functional blocks and an output stage. The output stage is a push-pull scheme with separated turn-on and turn-off paths for driving the gate terminal. The main functional blocks contain circuitry for improving turn-on, improving turn-off and providing short-circuit protection.

The following sections explain in more details the behaviour of IGBTs during the transients. A 30A, 500V IGBT was used in the laboratory tests. Its main characteristics are:

BV_{CES} > 500V @ I_C = 250µA
$V_{CE(sat)}$ < 3.3V @ I_C = 30A and V_g =15V
C_{iss} = 2500pF typical
C_{oss} = 330pF typical
C_{rss} = 80pF typical

Figure 2. Schematic of IGBT drive circuit



2.1 Turn-on

The dynamic behaviour of an IGBT is affected by the unavoidable parasitic capacitances of the structure, often referred to as C_{ge}, C_{ce} and C_{cg}. They are shown in Figure 3. Such parasitic capacitances together with stray inductances, gate bias, and driving impedance define the device performance in terms of switching speed and power losses.

The switching speed of a device having an insulated gate, i.e. voltage driven, is strictly related to the rate of supplying charge to the gate input capacitance [3]. This is true for lGBTs too, except during the falling edge of the collector current. The target of the device designer is to obtain a switching speed fast enough to reduce power losses without any increase in electromagnetic interference.

During turn-on in inductive load switching, the power losses mainly depend on both the di/dt, which influences the peak current due to the diode recovery, and the dynamic saturation voltage phenomenon. Moreover, the di/dt influences the EMI [4]. In the circuit of Figure 4, the voltage drop caused by the stray inductance L_{s1} of the emitter ground connection, reduces the drive current I_g that is defined by the equation:

$$I_g = (V_d - V_g - (L_{s1} \times di/dt))/R_g \qquad (1)$$

and moreover acts as a negative feedback during the current rise time. Taking into account the effect of L_{s1}, the di/dt gradient can be calculated by the relationship:

$$di/dt = V_d - V_{th} / (R_g C_{ge} / G_{fs}) + L_{s1}$$

where V_{th}, C_{ge}, and G_{fs} depend on the particular device; L_{s1}, and V_d are fixed by the circuit. The only way to manage the di/dt is to act on the gate resistance. In order to reduce the EMI it is better to reduce di/dt by increasing R_g, but that means reduction of the switching speed and hence increased power losses [5]. To solve the problem described above, the proposed circuit acts as follows. The initial gate current is fixed by adjusting $R_{g(on)}$ in agreement with both device electrical specifications and EMI requirements. When the collector current reaches its maximum value, the collector voltage starts to decrease and in this condition the circuit

Figure 3. Parasitic capacitances affecting the dynamic behaviour of IGBTs

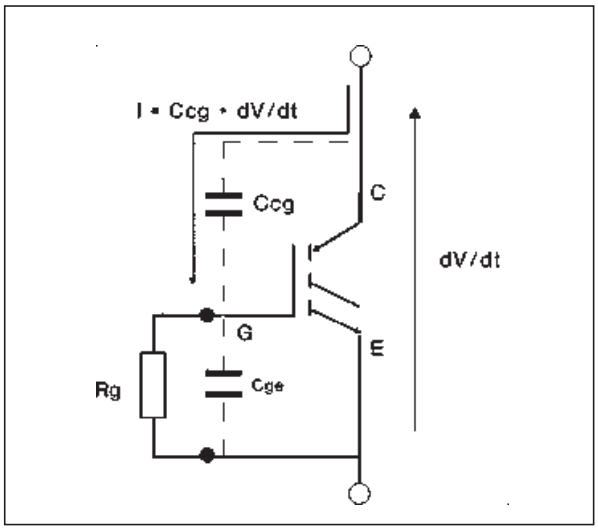
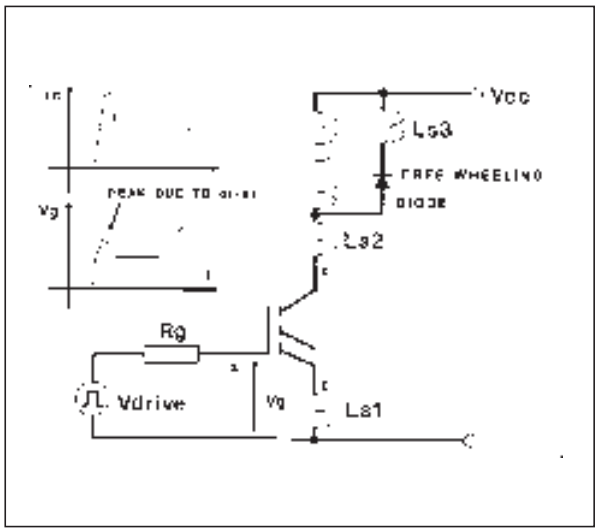


Figure 4. Parameters influencing di/dt at turn-on



enables a current generator. The current generator increases the gate current making the collector voltage fall faster and so eliminating the dynamic saturation voltage phenomenon. The delay between the positive edge of input signal and the duration of the enable signal of the current generator are both adjustable and so the best match between driving circuit and device is obtainable. Figure 5 shows the gate and collector waveforms at turn-on with traditional driving (i.e. only gate resistance), whereas figure 6 shows the same waveforms when the proposed driving circuit is used.

Note that the di/dt is the same, 200A/µs whilst the cross-over time is reduced by about 50%.

Figure 5. Turn-on with conventional drive circuit

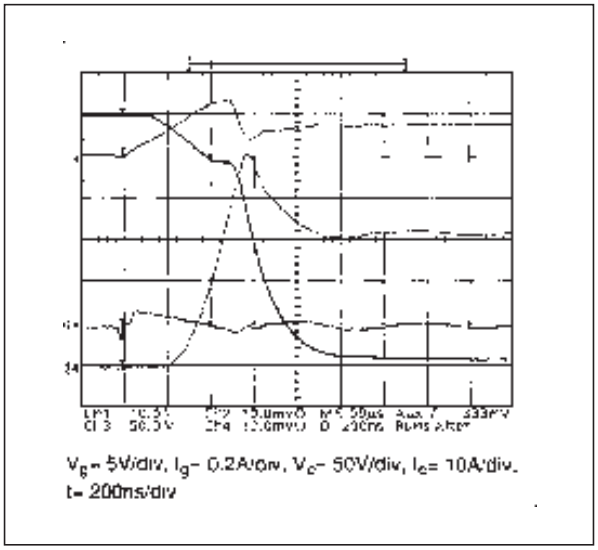
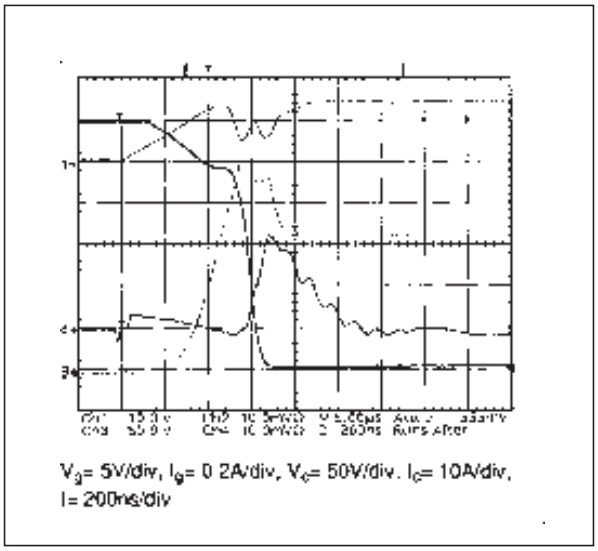


Figure 6. Turn-on with improved drive circuit



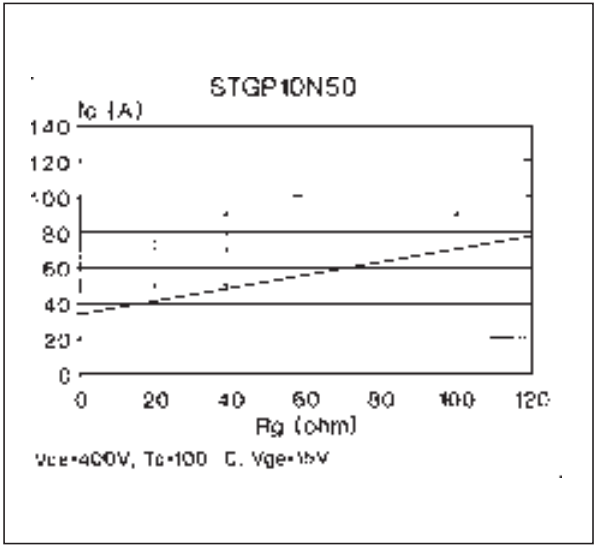
2.2 Turn-off

At turn-off the gate voltage starts to decrease from V_d until it reaches the "Miller" value. At the same time the collector voltage increases slightly as shown by the output characteristics with I_C = constant. At this point the collector voltage increases rapidly to its maximum value, causing the modulation of the collector-gate capacitance (Miller effect). During the Miller effect V_g is constant. Then, the collector current begins to fall quickly, due to the turn-off of the IGBT PMOS part and thereafter it continues with a tail due to the recombination of minority carriers in the substrate - this is the turn-off phase of the PNP transistor with open base. This tail, responsible for major losses, is strongly related to the device construction technology, and its effects cannot be reduced by means of the driving circuit.

Turn-off losses can be only controlled during both the Miller effect and the PMOS turn-off phases and with the aim being to reduce losses it is necessary to decrease the value of R_g [6]. As consequence of a reduction in gate resistance, dv/dt increases and so losses decrease, but it is necessary to take care not to exceed the RBSOA limits. In fact, the latching current and the RBSOA are strongly related to dv/dt, i.e. with the value of R_g. Figure 7 shows how the latching current depends on the gate resistance value. The manufacturer guarantees the RBSOA with a carefully specified R_g minimum value.

Based only on the above criteria, the gate impedance in bridge configurations has a high value, making

Figure 7. Latching current versus gate resistance



the circuit susceptible to spurious turn-on of the IGBTs, if an excessive dv/dt occurs across one of the devices in the off- state [7]. In fact, the voltage drop across the gate impedance, due to the current that flows through C_{CG}, figure 3, can reach the threshold voltage and so switch-on the device. Figure 8 shows the spurious turn-on phenomenon, when the device under test is subjected to a dv/dt of 2kV/µs. In this case the energy lost has been calculated as about 350µJ.

At turn-off the proposed circuit acts only through $R_{g\ off}$, that is fixed in agreement with the device electrical specifications. During the off-state phase, the proposed driving circuit avoids the spurious turn-on by reducing the gate impedance by a large amount, so preventing the gate voltage from reaching the threshold voltage. Such transient phenomenon is evident in Figure 9, which shows the IGBT improved waveforms under the same test conditions of figure 8, 2kV/µs. Note that the collector current trace shown in figure 9 is not due to spurious turn-on, but it is the unavoidable current necessary to charge the output capacitance of the device.

2.3 Short-Circuit

When a short-circuit occurs in the collector path, the current starts to increase until it reaches its maximum value, that is defined by the supply voltage, the gain of the device and the gate voltage. The devices that have good current performance, i.e. high gain, can fail under short circuit stresses and hence they need to be protected [8]. The presence of high voltage and high current simultaneously into the device, causes instantaneous very high power losses, consequently the device temperature increases. If the stress duration exceeds that specified in the data sheet, failure occurs. The proposed circuit operates by reducing the conduction time when a short circuit is detected by a high voltage, fast recovery diode that senses the IGBT desaturation [9]. An adjustable time delay inhibits the protection at turn-on, in order to allow for inrush currents. The relevant traces of current and various voltages during a short-circuit transient are shown in figure 10. From these it is evident how the protection block operates

Figure 8. Traces during spurious turn-on caused by 2kV/µs dv/dt

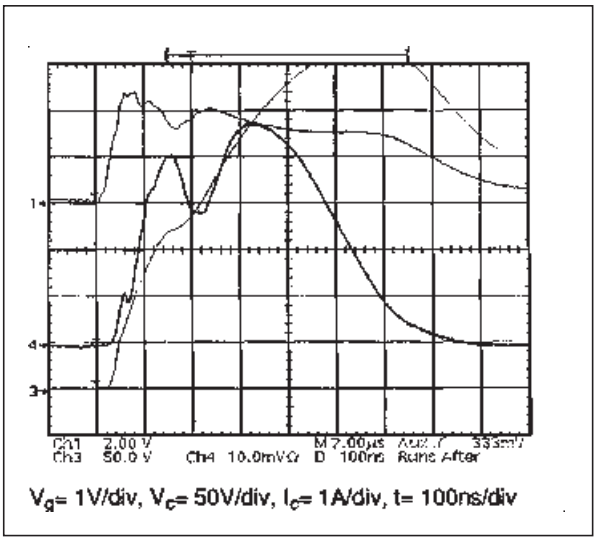


Figure 9. Improved behaviour with new drive circuit in prescence of di/dt

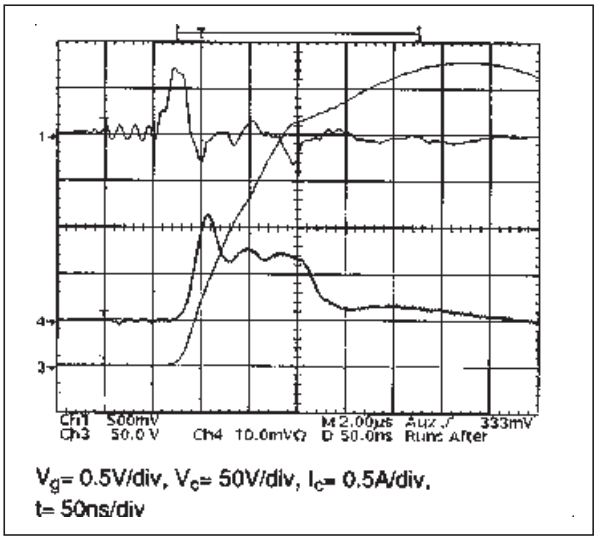
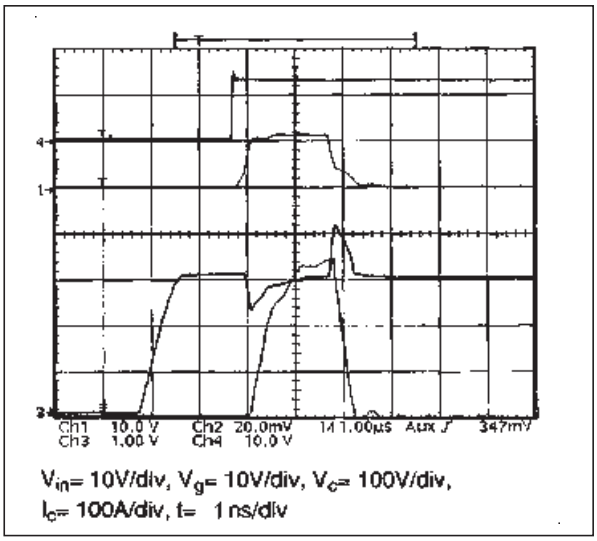


Figure 10. Traces during operation of short-circuit protection



preventing the fail condition. Note that the current peaks above 300A during the protection inhibit period due to the high current gain.

2.4 Integration

The proposed circuit has been developed having as the target its possible integration. In the case of driving circuit integration separated from the power device, bipolar or BCD technologies can be used, taking into account the necessity to provide external delay adjustments, in order to match it to several different devices. At the present time, integration of the driving circuit and power stage on the same chip is possible with VI Power technology using a Power MOSFET output stage. It has not yet been accomplished using lGBT output stages.

CONCLUSIONS

The characteristics of an optimal driving circuit for lGBT devices have been analysed. Experimental evaluation of IGBT performance has been carried out with both traditional and new driving circuits. The aim has been to demonstrate the advantages of the new proposals. The most important results obtained can be summarised as follows:

- in turn-on conditions the circuit provides separate control of the voltage and current gradients, so reducing both power losses and EMI,
- in turn-off conditions, the spurious triggering caused by sharp voltage gradients are avoided by means of a low impedance path offered by the driving circuit. Thus the power losses related to switching are reduced to a minimum value due to the output parasitic capacitance,
- in short-circuit conditions, the device is protected and turned-off in a preset time depending on the maximum time fixed by the manufacturer,

The new circuit can also be used to drive Power MOSFET devices with the same performance. Overall the results obtained have shown that the proposed driving circuit makes the lGBT perform in a manner that gives increased efficiency and higher reliability.

ACKNOWLEDGEMENTS

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