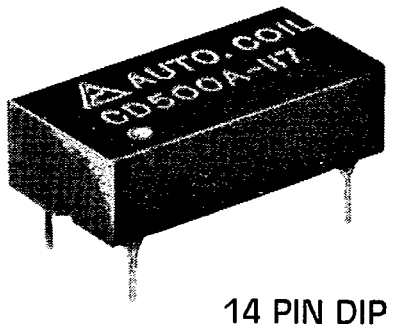
T-47-13

CA500 Series Military TTL Digital Delay Module, Single Delay

- Integrated circuits per Mil-Std-883B
- TTL input and output
- Precise and stable delay
- Reliable hybrid construction
- No external components required
- Fan out 10TTL loads
- Operating temperature −55°C +125°C
- Storage temperature −65°C to +150°C



14 PIN DIP

Electrical Characteristics:

VIH	(High level input voltage)	2.0 to 5.0V
IIH	(High level input current)	50 μA Max.
VIL	(Low level input voltage)	0.8 V Max.
IIL	(Low level input current)	−2 ma Max.
VOH	(High level output voltage)	2.5 V Min.
VOL	(Low level output voltage)	0.5 V Max.
VCC	(Supply voltage)	5.0 V±0.50VDC
ICC	(Supply current)	75 ma Max.

Mechanical Specifications:

Case: Epoxy filled D.A.P.
Leads: Alloy 42 or equiv. solder coated
Marking: White epoxy ink

Relscreening
10 cycles per method 1010 Cond B and 24 hrs. bake per method 1008 Cond B of Mil-Std-883

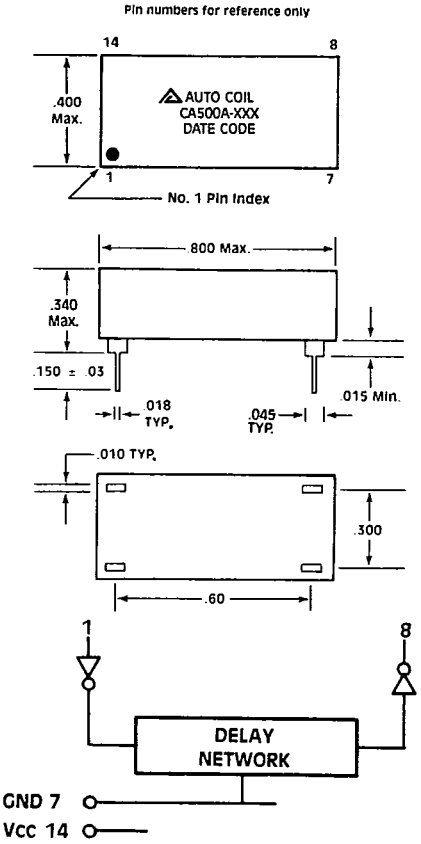
Also Available:

Intermediate delays
Tighter delay tolerances
Falling edge delay specifications
Tapped modules

Input & test conditions are not limiting parameters.
All digital delay modules can be operated at conditions other than specified.
Since accuracies may be slightly affected, we suggest that the module be evaluated under specific operating conditions.

All items comply with applicable portions of Group A and B requirements of Mil-D-23859

Specifications subject to change without notice.



Nominal Delays (In NS) ±2 NS or 5% Whichever is Greater			
Automatic Coil Part Number	PIN 1 to 8	Automatic Coil Part Number	PIN 1 to 8
CA500A-101	6	CA500A-118	60
CA500A-102	8	CA500A-119	70
CA500A-103	10	CA500A-120	80
CA500A-104	12	CA500A-121	90
CA500A-105	14	CA500A-122	100
CA500A-106	16	CA500A-123	110
CA500A-107	18	CA500A-124	120
CA500A-108	20	CA500A-125	130
CA500A-109	22	CA500A-126	140
CA500A-110	24	CA500A-127	150
CA500A-111	26	CA500A-128	200
CA500A-112	28	CA500A-129	250
CA500A-113	30	CA500A-130	300
CA500A-114	35	CA500A-131	350
CA500A-115	40	CA500A-132	400
CA500A-116	45	CA500A-133	450
CA500A-117	50	CA500A-134	500

Output rise time (TPLH) 4.0 NS max. (0.75 to 2.4 V level).

Test Conditions:

1) All measurements are made @ 25°C
2) VCC is maintained @ 5.0 VDC
3) All measurements are made with no loads on output
4) Delay measured @ 1.5V level
5) Delay & tolerance for leading edges only (TPLH) – falling edges (TPHL) closely matched to TPLH

Input Conditions:

1) Pulse amplitude: 3.20V
2) Input rise time 3.0 NS (10 to 90%)
3) Pulse width 2 × total delay
4) Duty cycle < 25%

Automatic Coil Corp.
3545 N.W. 71st Street, Miami, Florida 33147