PRELIMINARY

CY7C9689

TAXI™ Compatible HOTLink™ Transceiver

Features

- **Second-generation HOTLink™ technology**
- **AMD™ AM7968/7969 TAXIchip™ compatible**
- **8-bit 4B/5B or 10-bit 5B/6B NRZI encoded data transport**
- **10-bit or 12-bit NRZI pre-encoded (bypass) data transport**
- **Synchronous TTL parallel interface**
- **Embedded/Bypassable 256 character Transmit and Receive FIFOs**
- **50-to-200 MBaud serial signaling rate**
- **Internal PLLs with no external PLL components**
- **Dual differential PECL-compatible serial inputs and outputs**
- **Compatible with fiber-optic modules and copper cables**
- **Built-In Self-Test (BIST) for link testing**
- **Link Quality Indicator**
- **Single +5.0V ±10%supply**
- **100-pin TQFP**

Functional Description

The CY7C9689 HOTLink Transceiver is a point-to-point communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging between 50 and 200 MBaud. The transmit section accepts parallel data of selectable widths and converts it to serial data, while the receiver section accepts serial data and converts it to parallel data of selectable widths. *Figure 1* illustrates typical connections between two independent host systems and corresponding CY7C9689 parts. The CY7C9689 provides enhanced technology, increased functionality, a higher level of integration, higher data rates, and lower power dissipation over the AMD AM7968/7969 TAXIchip products.

The transmit section of the CY7C9689 HOTLink can be configured to accept either 8- or 10-bit data characters on each clock cycle, and stores the parallel data into an internal synchronous Transmit FIFO. Data is read from the Transmit FIFO and is encoded using embedded 4B/5B or 5B/6B encoders to improve its serial transmission characteristics. These encoded characters are then serialized, converted to NRZI, and output from two PECL compatible differential transmission line drivers at a bit-rate of either 10 or 20 times the input reference clock in 8-bit (or 10-bit bypass) mode, or 12 or 24 times the reference clock in 10-bit (or 12-bit bypass) mode.

The receive section of the CY7C9689 HOTLink accepts a serial bit-stream from one of two PECL compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit stream is converted from NRZI to NRZ, deserialized, framed into characters, 4B/5B or 5B/6B decoded, and checked for transmission errors. The recovered 8- or 10-bit decoded characters are then written to an internal Receive FIFO, and presented to the destination host system.

The integrated 4B/5B and 5B/6B encoder/decoder may be bypassed (disabled) for systems that present externally encoded or scrambled data at the parallel interface. With the encoder bypassed, the pre-encoded parallel data stream is converted to and from a serial NRZI stream. The embedded FIFOs may also be bypassed (disabled) to create a reference-locked serial transmission link. For those systems requiring even greater FIFO storage capability, external FIFOs may be directly coupled to the CY7C9689 through the parallel interface without the need for additional glue-logic.

The TTL parallel I/O interface may be configured as either a FIFO (configurable for depth expansion through external FIFOs) or as a pipeline register extender. The FIFO configurations are optimized for transport of time-independent (asynchronous) 8- or 10-bit character-oriented data across a link. A Built-In Self-Test (BIST) pattern generator and checker allows for testing of the high-speed serial data paths in both the transmit and receive sections, and across the interconnecting links.

HOTLink devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting workstations, backplanes, servers, mass storage, and video transmission equipment.

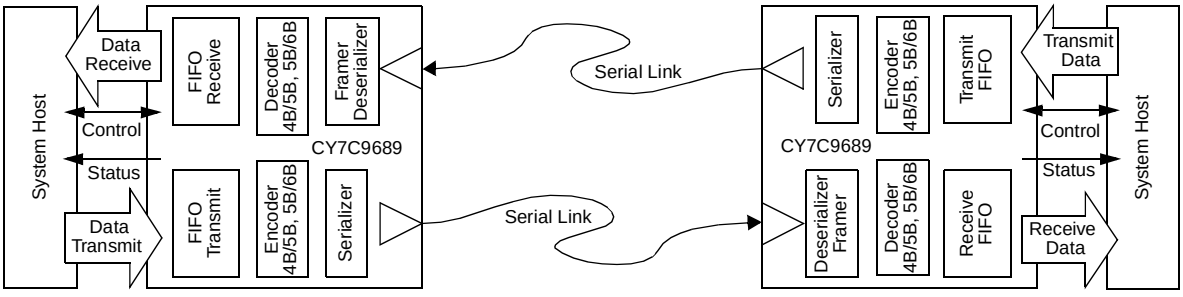
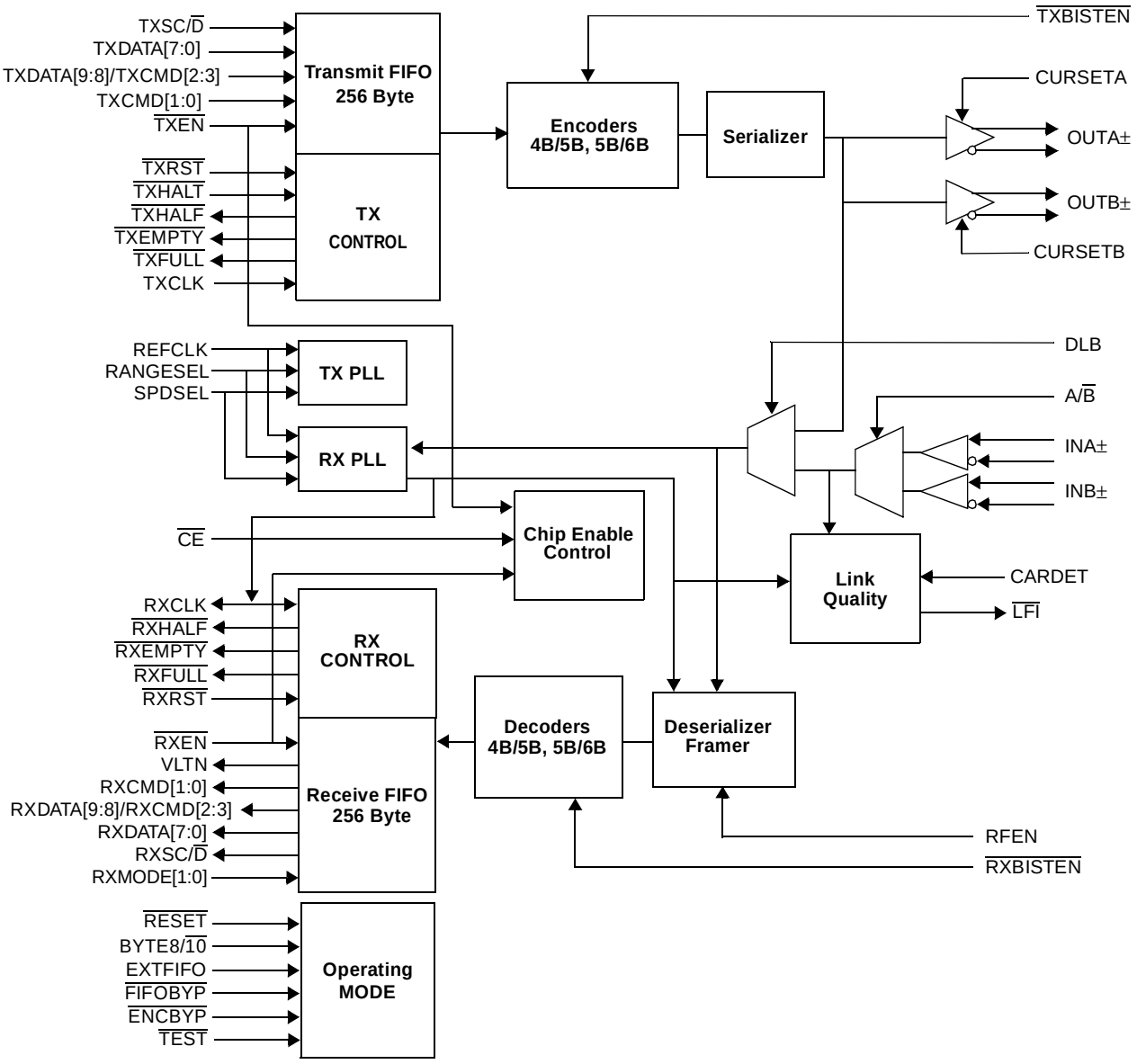
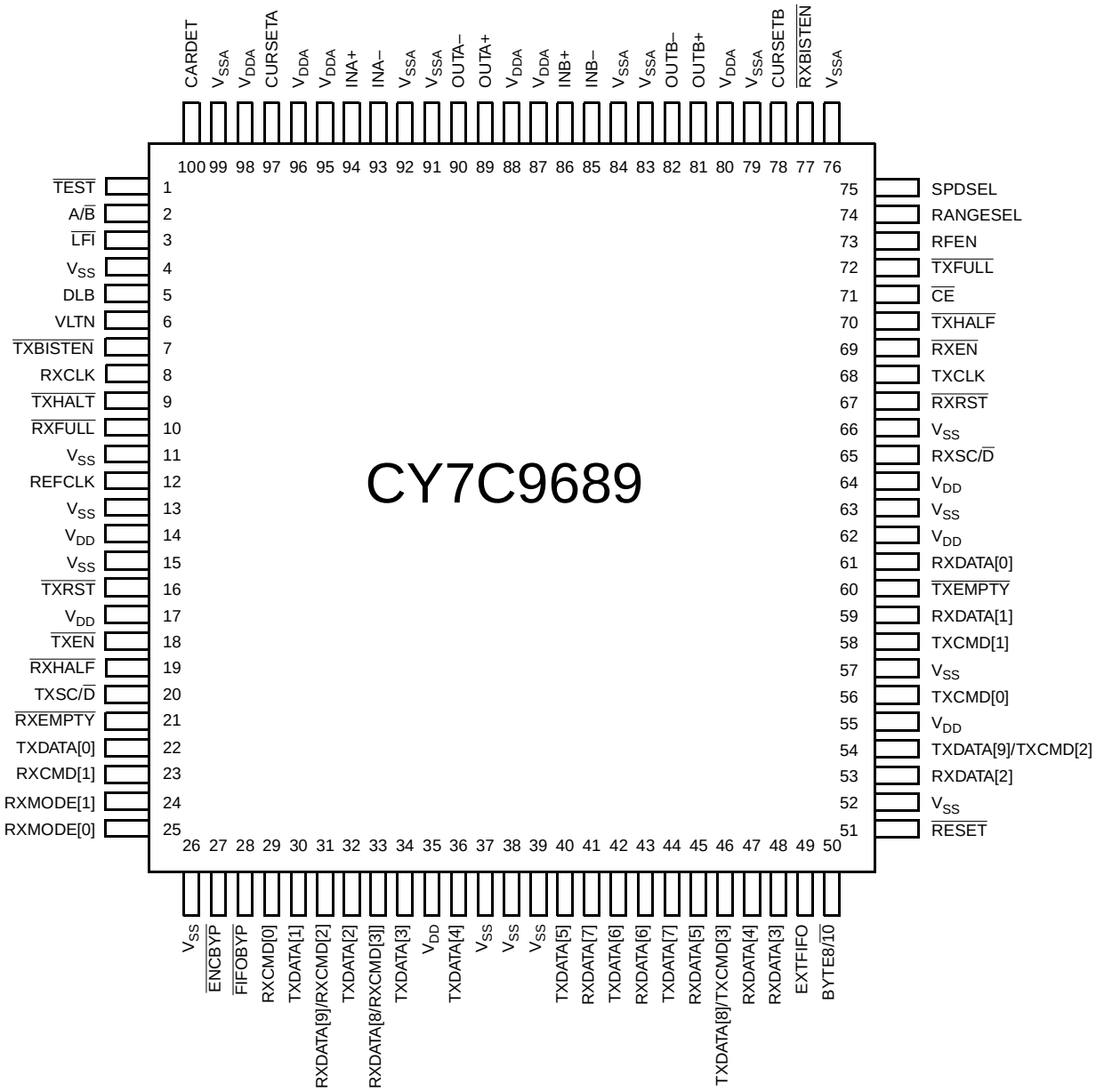


Figure 1. HOTLink System Connections

CY7C9689 HOTLink Logic Block Diagram



Pin Configuration



Pin Descriptions

Pin	Name	I/O Characteristics	Signal Description
Transmit Path Signals			
68	TXCLK	TTL clock input	Transmit FIFO Clock. Used to sample all Transmit FIFO and related interface signals.
44, 42, 40, 36, 34, 32, 30, 22	TXDATA[7:0]	TTL input, sampled on TXCLK↑ or REFCLK↑	Parallel Transmit DATA input. When selected ($\overline{CE}$=LOW and TXEN = asserted), information on these inputs is processed as DATA when TXSC/$\overline{D}$ is LOW and ignored otherwise. When the encoder is bypassed ($\overline{ENCBYP}$ is LOW), TXDATA[7:0] functions as the least significant eight bits of the 10- or 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled ($\overline{FIFOBYP}$ is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW) these inputs are captured on the rising edge of REFCLK.
54, 46	TXDATA[9:8]/ TXCMD[2:3]	TTL input, sampled on TXCLK↑ or REFCLK↑	Parallel Transmit DATA or COMMAND input. When selected, BYTE8/$\overline{10}$ is HIGH, and the encoder is enabled ($\overline{ENCBYP}$ is HIGH), information on these inputs are processed as TXCMD[2:3] if TXSC/$\overline{D}$ is HIGH and ignored otherwise. When selected, BYTE8/$\overline{10}$ is LOW, and the encoder is enabled ($\overline{ENCBYP}$ is HIGH), information on these inputs are processed as TXDATA[9:8] if TXSC/$\overline{D}$ is LOW and ignored otherwise. When the encoder is bypassed ($\overline{ENCBYP}$ is LOW), TXDATA[9:8] functions as the 9th and 10th bits of the 10- or 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled ($\overline{FIFOBYP}$ is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW), these inputs are captured on the rising edge of REFCLK.
58, 56	TXCMD[1:0]	TTL input, sampled on TXCLK↑ or REFCLK↑	Parallel Transmit COMMAND input. When selected and the encoder is enabled ($\overline{ENCBYP}$ is HIGH), information on these inputs is processed as a COMMAND when TXSC/$\overline{D}$ is HIGH and ignored otherwise. When BYTE8/$\overline{10}$ is HIGH and the encoder is bypassed ($\overline{ENCBYP}$ is LOW), the TXCMD[1:0] inputs are ignored. When BYTE8/$\overline{10}$ is LOW and when the encoder is bypassed ($\overline{ENCBYP}$ is LOW), the TXCMD[1:0] inputs function as the 11th and 12th (MSB) bits of the 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled ($\overline{FIFOBYP}$ is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW), these inputs are sampled on the rising edge of REFCLK.
20	TXSC/$\overline{D}$	TTL input, sampled on TXCLK↑ or REFCLK↑	COMMAND or DATA input selector. When selected, BYTE8/$\overline{10}$ is HIGH, and the encoder is enabled ($\overline{ENCBYP}$ is HIGH), this input selects if the DATA or COMMAND inputs are processed. If TXSC/$\overline{D}$ is HIGH, the value on TXCMD[3:0] is captured as one of sixteen possible COMMANDs, and the data on the TXDATA[7:0] bits are ignored. If TXSC/$\overline{D}$ is LOW, the information on TXDATA[7:0] is captured as one of 256 possible 8-bit DATA values, and the information on the TXCMD[3:0] bus is ignored. When BYTE8/$\overline{10}$ is LOW and the encoder is enabled ($\overline{ENCBYP}$ is HIGH) this input selects if the DATA or COMMAND inputs are processed. If TXSC/$\overline{D}$ is HIGH, the information on TXCMD[1:0] is captured as one of four possible COMMANDs, and the information on the TXDATA[9:0] bits are ignored. If TXSC/$\overline{D}$ is LOW, the information on TXDATA[9:0] is captured as one of 1024 possible 10-bit DATA values, and the information on the TXCMD[1:0] bus is ignored. When the encoder is bypassed ($\overline{ENCBYP}$ is LOW) TXSC/$\overline{D}$ is ignored

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
18	$\overline{\text{TXEN}}$	TTL input, sampled on TXCLK↑ or REFCLK↑	Transmit Enable. $\overline{\text{TXEN}}$ is sampled on the rising edge of the TXCLK or REFCLK input and enables parallel data bus write operations (when selected). The device is selected when $\overline{\text{TXEN}}$ is asserted during a clock cycle immediately following one in which $\overline{\text{CE}}$ is sampled LOW. Depending on the level on EXTFIFO, the asserted state for $\overline{\text{TXEN}}$ can be active HIGH or active LOW. If EXTFIFO is LOW, then $\overline{\text{TXEN}}$ is active LOW and data is captured on the same clock cycle where $\overline{\text{TXEN}}$ is sampled LOW. If EXTFIFO is HIGH, then TXEN is active HIGH and data is captured on the clock cycle following any clock edge when TXEN is sampled HIGH.
7	$\overline{\text{TXBISTEN}}$	TTL input, asynchronous	Transmitter BIST Enable. When $\overline{\text{TXBISTEN}}$ is LOW, the transmitter generates a 511-character repeating sequence, that can be used to validate link integrity. This 4B/5B BIST sequence is generated regardless of the state of other configuration inputs. The transmitter returns to normal operation when $\overline{\text{TXBISTEN}}$ is HIGH. All Transmit FIFO read operations are suspended when BIST is active.
16	$\overline{\text{TXRST}}$	TTL input, sampled on TXCLK↑	Reset Transmit FIFO. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), $\overline{\text{TXEN}}$ is deasserted, $\overline{\text{CE}}$ is asserted (LOW), and $\overline{\text{TXRST}}$ is sampled LOW by TXCLK for seven cycles, the Transmit FIFO begins its internal reset process. The Transmit FIFO $\overline{\text{TXFULL}}$ flag is asserted and the host interface counter and address pointer are zeroed. This reset propagates to the serial transmit side, any remaining counters and pointers. The $\overline{\text{TXFULL}}$ flag is asserted until both sides of the Transmit FIFO have reset. While $\overline{\text{TXRST}}$ remains asserted, the Transmit FIFO remains in reset and the $\overline{\text{TXFULL}}$ output remains asserted. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXRST}}$ is ignored.
9	$\overline{\text{TXHALT}}$	TTL input, sampled on TXCLK↑	Transmitter Halt control input. When $\overline{\text{TXHALT}}$ is asserted LOW, transmission of data is suspended and the HOTLink TAXI transmits SYNC characters. When $\overline{\text{TXHALT}}$ is deasserted HIGH, normal data processing proceeds. If the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), the interface is allowed to continue loading data into the Transmit FIFO while $\overline{\text{TXHALT}}$ is asserted.
72	$\overline{\text{TXFULL}}$	Three-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Full status flag. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH) and its flags are driven ($\overline{\text{CE}}$ is LOW), $\overline{\text{TXFULL}}$ is asserted when four or fewer characters can be written to the HOTLink Transmit FIFO. If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXFULL}}$ is asserted to enforce the full/unavailable status of the Transmit FIFO during reset. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), the $\overline{\text{TXFULL}}$ output changes after the rising edge of REFCLK. $\overline{\text{TXFULL}}$ is asserted when the transmitter is BUSY (not accepting a new data or command characters) and deasserted when new characters can be accepted. When the Transmit FIFO is bypassed and RANGESEL is HIGH or SPDSEL is LOW, $\overline{\text{TXFULL}}$ toggles at the character rate to provide a character rate reference control-indication since REFCLK is operating at twice of the data rate. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{TXFULL}}$ is active LOW. When EXTFIFO is HIGH, TXFULL is active HIGH.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
70	$\overline{\text{TXHALF}}$	Three-state TTL output, changes following TXCLK↑	Transmit FIFO Half-full status flag. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH and $\overline{\text{CE}}$ is LOW) $\overline{\text{TXHALF}}$ is asserted when the HOTLink Transmit FIFO is ≥ half full (128 characters is half full). If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXHALF}}$ is asserted to enforce the full/unavailable status of the Transmit FIFO during reset. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXHALF}}$ remains deasserted, having no logical function. $\overline{\text{TXHALF}}$ is forced to the High-Z state only during a "full-chip" reset (i.e., while $\overline{\text{RESET}}$ is LOW).
60	$\overline{\text{TXEMPTY}}$	Three-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Empty status flag. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH and $\overline{\text{CE}}$ is LOW), $\overline{\text{TXEMPTY}}$ is asserted when the HOTLink Transmit FIFO has no data to forward to the encoder. If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXEMPTY}}$ is deasserted and remains deasserted until the Transmit FIFO reset operation is complete. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXEMPTY}}$ is asserted to indicate that the transmitter can accept data. $\overline{\text{TXEMPTY}}$ is also used as a BIST progress indicator when $\overline{\text{TXBISTEN}}$ is asserted. When $\overline{\text{TXBISTEN}}$ is asserted LOW, $\overline{\text{TXEMPTY}}$ becomes the transmit BIST-loop counter indicator (regardless of the logic state of $\overline{\text{FIFOBYP}}$). In this mode $\overline{\text{TXEMPTY}}$ is asserted for one TXCLK or REFCLK period at the end of each transmitted BIST sequence. **NOTE:** During BIST operations, when the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), it is necessary to keep TXCLK operating, even though no data is loaded into the Transmit FIFO and TXEN is never asserted, to allow the $\overline{\text{TXEMPTY}}$ flag to respond to the BIST state changes. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{TXEMPTY}}$ is active LOW. When EXTFIFO is HIGH, TXEMPTY is active HIGH. If $\overline{\text{CE}}$ is sampled asserted (LOW), $\overline{\text{TXEMPTY}}$ is driven to an active state. If $\overline{\text{CE}}$ is sampled deasserted (HIGH), $\overline{\text{TXEMPTY}}$ is placed into a High-Z state.
Receive Path Signals			
8	RXCLK	Bidirectional TTL clock	Receive clock. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), this clock is the Receive interface *input* clock and is used to control Receive FIFO read and reset, operations. When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), this clock becomes the recovered Receive PLL character clock *output* which runs continuously at the character rate.
41, 43, 45, 47, 48, 53, 59,61	RXDATA[7:0]	Three-state TTL output, changes following RXCLK↑	Parallel Receive DATA outputs. When the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), the low-order eight bits of the decoded DATA character are presented on the RXDATA[7:0] outputs. COMMAND characters, when they are received, do not disturb these outputs. When the decoder is bypassed, the low order eight bits of the non-decoded character are presented on the RXDATA[7:0] outputs. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), these outputs change on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of RXCLK input. RXEN is the three-state control for RXDATA[7:0].

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
31, 33	RXDATA[9:8]/ RXCMD[2:3]	Three-state TTL output, changes following RXCLK↑	Parallel Receive DATA or COMMAND output. When BYTE8/$\overline{10}$ is HIGH and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH) these outputs reflects the value for the most recently received RXCMD[2:3]. When BYTE8/$\overline{10}$ is LOW and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH) these outputs reflects the value for the most recently received RXDATA[9:8]. When the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), RXDATA[9:8] functions as the 9th and 10th bits of the 10- or 12-bit non-decoded receive character. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), these outputs change on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of the RXCLK input. RXEN is a three-state control for RXDATA[9:8]/RXCMD[2:3].
23, 29	RXCMD[1:0]	Three-state TTL output, changes following RXCLK↑	Parallel Receive COMMAND outputs. When the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH) these outputs reflect the value for the most recently received RXCMD[1:0]. When BYTE8/$\overline{10}$ is HIGH and the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), these outputs have no meaning and are driven LOW. When BYTE8/$\overline{10}$ is LOW and the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), RXCMD[1:0] functions as the 11th and 12th (MSB) bits of the 12-bit non-decoded receive character. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), this output changes on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of the RXCLK input. RXEN is a three-state control for RXCMD[1:0].
69	$\overline{\text{RXEN}}$	TTL input, sampled on RXCLK↑	Receive Enable input. $\overline{\text{RXEN}}$ is a three-state control for the parallel data bus read operations. $\overline{\text{RXEN}}$ is sampled on the rising edge of the RXCLK input (or output) and enables parallel data bus read operations (when selected). The device is selected when $\overline{\text{RXEN}}$ is asserted during an RXCLK cycle immediately following one in which $\overline{\text{CE}}$ is sampled LOW. The parallel data pins are driven to active levels after the rising edge of RXCLK. When $\overline{\text{RXEN}}$ is de-asserted (ending the selection) the parallel data pins are High-Z after the rising edge of RXCLK. Depending on the level on EXTFIFO, this signal can be active HIGH or active LOW. If EXTFIFO is LOW, then $\overline{\text{RXEN}}$ is active LOW. If EXTFIFO is HIGH, then RXEN is active HIGH. Data is delivered on the clock cycle following any clock edge when RXEN is active.
65	RXSC/$\overline{\text{D}}$	Three-state TTL output, changes following RXCLK↑	COMMAND or DATA output indicator. When BYTE8/$\overline{10}$ is HIGH and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), this output indicates which group of outputs have been updated. If RXSC/$\overline{\text{D}}$ is HIGH, RXCMD[3:0] contains a new COMMAND. The DATA on the RXDATA[7:0] pins remain unchanged. If RXSC/$\overline{\text{D}}$ is LOW, RXDATA[7:0] contains a new DATA character. The COMMAND output on RXCMD[3:0] remain unchanged. When BYTE8/$\overline{10}$ is LOW and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), this output indicates which group of outputs have been updated. If RXSC/$\overline{\text{D}}$ is HIGH, RXCMD[1:0] contains a new COMMAND and the DATA on the RXDATA[9:0] remain unchanged. If RXSC/$\overline{\text{D}}$ is LOW, RXDATA[9:0] contains a new DATA character and the COMMAND output on RXCMD[1:0] remain unchanged. When the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW) RXSC/$\overline{\text{D}}$ is not used and may be left unconnected. RXEN is a three-state control for RXSC/$\overline{\text{D}}$.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
6	VLTN	Three-state TTL output, changes following RXCLK↑	Code rule violation detected. VLTN is asserted in response to detection of a 4B/5B or 5B/6B character that does not meet the coding rules of these characters. When VLTN is asserted, the values on the output DATA and COMMAND buses remain unchanged. VLTN remains asserted for one RXCLK period. VLTN is used to report character mismatches when $\overline{\text{RXBISTEN}}$ is driven LOW. VLTN is driven LOW when the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW). RXEN is a three-state control for VLTN.
67	$\overline{\text{RXRST}}$	TTL input, sampled on RXCLK↑	Receive FIFO Reset. Active LOW. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), $\overline{\text{RXEN}}$ is deasserted, $\overline{\text{CE}}$ is asserted (LOW), and $\overline{\text{RXRST}}$ is sampled while asserted (LOW) by RXCLK for seven cycles, the Receive FIFO begins its internal reset process. Once the reset operation is started, the $\overline{\text{RXEMPTY}}$ flag is asserted and the interface counters and address pointer are zeroed. The reset operation proceeds to clear out the internal write pointers and counters. The $\overline{\text{RXEMPTY}}$ output remains asserted through the reset operation and remains asserted until new data is written to the Receive FIFO. While $\overline{\text{RXRST}}$ remains asserted, the Receive FIFO remains in reset and cannot accept received characters. When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{RXRST}}$ is ignored.
24, 25	RXMODE[1:0]	Static control input TTL levels Normally wired HIGH or LOW	Receiver Discard Policy mode select. • 00b—allows all characters to be written into the Receive FIFO or output to the Receive data bus • 01b—discards all JK or LM sync characters except the “last” one of a string of sync characters. Single sync characters in a data stream are included in the data written into the Receive FIFO. • 1Xb—discards all JK or LM sync characters. The data stream written into the Receive FIFO does not include sync characters.
77	$\overline{\text{RXBISTEN}}$	TTL input, asynchronous	Receiver BIST enable. Active LOW. When LOW, the receiver is configured to perform a character-for-character match of the incoming data stream with a 511-character BIST sequence. The result of character mismatches are indicated on the VLTN pin. Completion of each 511-character BIST loop is accompanied by an assertion pulse on the $\overline{\text{RXFULL}}$ flag. The state of $\overline{\text{ENCBYP}}$, $\overline{\text{FIFOBYP}}$, and BYTE8/$\overline{10}$ have no effect on BIST operation.
73	RFEN	TTL input, asynchronous	Reframe Enable. Used to control when the framer is allowed to adjust the character boundaries based on detection of one or more framing characters in the data stream. When framing is enabled (RFEN is HIGH) the receive framer realigns the serial stream to the incoming 10-bit JK sync character (if BYTE8/$\overline{10}$ is HIGH) or the 12-bit LM sync character (if BYTE8/$\overline{10}$ is LOW). Framing is disabled when RFEN is LOW. The deassertion of RFEN freezes the character boundary relationship between the serial stream and character clock. RFEN is an asynchronous input, sampled by the internal Receive PLL character clock.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
10	$\overline{\text{RXFULL}}$	Three-state TTL output, changes following RXCLK↑	Receive FIFO Full flag. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH) and its flags are driven ($\overline{\text{CE}}$ is LOW), $\overline{\text{RXFULL}}$ is asserted when space is available for four or fewer characters to be written to the HOTLink Receive FIFO. If the RXCLK input is not continuous or the FIFO is accessed at a rate slower than data is being received, $\overline{\text{RXFULL}}$ may also indicate that some data has been lost because of FIFO overflow. When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{RXFULL}}$ is deasserted to indicate that valid data may be present. $\overline{\text{RXFULL}}$ is also used as a BIST progress indicator, and pulses once every pass through the 511 character BIST loop. When $\overline{\text{RXBISTEN}}$ is asserted (LOW), $\overline{\text{RXFULL}}$ becomes the receive BIST loop progress indicator (regardless of the logic state of $\overline{\text{FIFOBYP}}$). While $\overline{\text{RXBISTEN}}$ is asserted, $\overline{\text{RXFULL}}$ is asserted until the receiver detects the start of the BIST pattern. Then $\overline{\text{RXFULL}}$ is deasserted for the duration of the BIST pattern, pulsing asserted for one RXCLK period on the last symbol of each BIST loop. If 14 of 28 consecutive symbols are received in error, $\overline{\text{RXFULL}}$ returns to the asserted state until the start of a BIST pattern is again detected. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{RXFULL}}$ is active LOW. When EXTFIFO is HIGH, RXFULL is active HIGH.
19	$\overline{\text{RXHALF}}$	Three-state TTL output, changes following RXCLK↑	Receive FIFO Half-full flag. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH and $\overline{\text{CE}}$ is LOW) $\overline{\text{RXHALF}}$ is asserted when the HOTLink Receive FIFO is ≥ half full (128 characters is half full). If a Receive FIFO reset has been initiated ($\overline{\text{RXRST}}$ was sampled asserted for a minimum of seven RXCLK cycles), $\overline{\text{RXHALF}}$ is deasserted to enforce the empty/unavailable status of the Receive FIFO during reset. If $\overline{\text{FIFOBYP}}$ is LOW, $\overline{\text{RXHALF}}$ remains deasserted having no logical function. $\overline{\text{RXHALF}}$ is forced to the High-Z state only during a “full-chip” reset (i.e., while $\overline{\text{RESET}}$ is LOW).
21	$\overline{\text{RXEMPTY}}$	Three-state TTL output, changes following RXCLK↑	Receive FIFO Empty flag. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH) and its flags are driven ($\overline{\text{CE}}$ is LOW), $\overline{\text{RXEMPTY}}$ is asserted when the HOTLink Receive FIFO has no data to forward to the parallel interface. If a Receive FIFO reset has been initiated ($\overline{\text{RXRST}}$ was sampled asserted for a minimum of seven RXCLK cycles), $\overline{\text{RXEMPTY}}$ is asserted to enforce the empty/unavailable status of the Receive FIFO during reset. Any read operation occurring when $\overline{\text{RXEMPTY}}$ is asserted results in no change in the FIFO status, and the data from the last valid read remains on the RXDATA bus. When the Receive FIFO is bypassed but the decoder is enabled, $\overline{\text{RXEMPTY}}$ is used as a valid data indicator. When deasserted it indicates that valid data is present at the RXDATA or RXCMD outputs as indicated by RXSC/$\overline{\text{D}}$. When asserted it indicates that a SYNC character (JK or LM) is present on the RXCMD output pins. When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{RXEMPTY}}$ is deasserted whenever data is ready. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{RXEMPTY}}$ is active LOW. When EXTFIFO is HIGH, RXEMPTY is active HIGH.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
Control Signals			
71	$\overline{CE}$	TTL input sampled on TXCLK↑, RXCLK↑, or REFCLK↑	Chip Enable input. Active LOW. When $\overline{CE}$ is asserted and sampled LOW by RXCLK, the Receive FIFO status flags are driven to their active states. When this input is deasserted and sampled by RXCLK, the Receive FIFO status flags are placed in a High-Z state. When $\overline{CE}$ has been sampled LOW and $\overline{RXEN}$ changes from deasserted to asserted and is sampled by RXCLK, the RXSC/$\overline{D}$, RXDATA[7:0], RXDATA[9:8]/RXCMD[2:3] and VLTN output drivers are enabled and go to their driven levels. These pins remain driven until $\overline{RXEN}$ is sampled deasserted. When the Transmit FIFO is enabled ($\overline{FIFOBYP}$ is HIGH), and $\overline{CE}$ is asserted and sampled by TXCLK, the Transmit FIFO status flags are driven to their active states. When this input is deasserted and sampled by TXCLK, the Transmit FIFO status flags are placed in a High-Z state. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW), and $\overline{CE}$ is asserted and sampled by REFCLK, the Transmit FIFO status flags are driven to their active states. When this input is deasserted and sampled by REFCLK, the Transmit FIFO status flags are placed in a High-Z state. When the Transmit FIFO is enabled ($\overline{FIFOBYP}$ is HIGH), $\overline{CE}$ has been sampled LOW, and $\overline{TXEN}$ changes from deasserted to asserted and is sampled by TXCLK, the TXSC/$\overline{D}$, TXDATA[7:0], TXDATA[9:8]/RXCMD[2:3], and TXCMD[1:0] inputs are sampled and passed to the Transmit FIFO. These inputs are sampled on all consecutive TXCLK cycles until $\overline{TXEN}$ is sampled deasserted. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW), $\overline{CE}$ has been sampled LOW, and $\overline{TXEN}$ changes from deasserted to asserted and is sampled by REFCLK, the TXSC/$\overline{D}$, TXDATA[7:0], TXDATA[9:8]/RXCMD[2:3], and TXCMD[1:0] inputs are sampled and passed to the encoder or serializer as directed by other control inputs. These inputs are sampled on all consecutive REFCLK cycles until $\overline{TXEN}$ is sampled deasserted.
12	REFCLK	TTL clock input	PLL Frequency Reference clock. This clock input is used as the timing reference for the transmit and receive PLLs. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is HIGH), REFCLK is also used as the clock for the parallel transmit interface.
75	SPDSEL	Static control input TTL levels Normally wired HIGH or LOW	Speed select. Used to select from one of two operating serial rates for the CY7B9689. When SPDSEL is HIGH, the signaling rate is between 100 and 200 MBaud. When LOW, the signaling rate is between 50 and 100 MBaud. Used in combination with RANGESEL and BYTE8/$\overline{10}$ to configure the VCO multipliers and dividers.
74	RANGESEL	Static control input TTL levels Normally wired HIGH or LOW	Range select. Selects the proper prescaler for the REFCLK input. If RANGESEL is LOW, the REFCLK input is passed directly to the Transmit PLL clock multiplier. If RANGESEL is HIGH, REFLCK is divided by two before being sent to the Transmit PLL multiplier. When the Transmit FIFO is bypassed ($\overline{FIFOBYP}$ is LOW), with RANGESEL HIGH or SPDSEL LOW, $\overline{TXFULL}$ toggles at half the REFCLK rate to provide a character rate indication, and to show when data can be accepted.
51	$\overline{RESET}$	Asynchronous TTL input	Master Reset for internal logic. Pulsed LOW for one or more REFCLK cycles.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
28	$\overline{\text{FIFOBYP}}$	Static control input TTL levels Normally wired HIGH or LOW	FIFO Bypass enable. When asserted, the Transmit and Receive FIFOs are bypassed. In this mode TXCLK is not used. Instead all transmit data must be synchronous to REFCLK. Transmit FIFO status flags are synchronized to REFCLK. All received data is synchronous to RXCLK output. Receive FIFO status flags are synchronized to RXCLK (the recovered Receive PLL character clock). When not asserted, the Transmit and Receive FIFOs are enabled. In this mode all Transmit FIFO writes are synchronized to TXCLK, and all Receive FIFO reads are synchronous to the RXCLK input.
50	BYTE8/$\overline{10}$	Static control input TTL levels Normally wired HIGH or LOW	8/10-bit Parallel Data Size select. When set for 8-bit data (BYTE8/$\overline{10}$ is HIGH) and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), 8-bit DATA characters and 4-bit COMMAND characters are captured at the TXDATA[7:0] or TXCMD[3:0] inputs (selected by the TXSC/$\overline{D}$ input) and passed to the Transmit FIFO (if enabled) and encoder. Received characters are decoded, passed through the Receive FIFO (if enabled) and presented at either the RXDATA[7:0] or RXCMD[3:0] outputs and indicated by the RXSC/$\overline{D}$ output. When set for 8-bit data (BYTE8/$\overline{10}$ is HIGH) and the encoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), the internal data paths are set for 10-bit characters. Each received character is presented to the Receive FIFO (if enabled) and is passed to the RXDATA[9:0] outputs. When set for 10-bit data (BYTE8/$\overline{10}$ is LOW) and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), 10-bit DATA characters and 2-bit COMMAND characters are captured at the TXDATA[9:0] or TXCMD[1:0] inputs (selected by the TXSC/$\overline{D}$ input) and passed to the Transmit FIFO (if enabled) and encoder. Received characters are decoded, passed through the Receive FIFO (if enabled) and presented at either the RXDATA[9:0] or RXCMD[1:0] outputs and indicated by the RXSC/$\overline{D}$ output. When set for 10-bit data (BYTE8/$\overline{10}$ is LOW) and the encoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), the internal clock data paths are set for 12-bit characters. Each received character is presented to the Receive FIFO (if enabled) and is passed to the RXDATA[9:0] and the RXCMD[1:0] outputs.
49	EXTFIFO	Static control input TTL levels Normally wired HIGH or LOW	External FIFO mode. EXTFIFO modifies the active state of the $\overline{\text{RXEN}}$ and $\overline{\text{TXEN}}$ inputs and the timing of the Transmitter and Receiver data buses. When configured for external FIFOs (EXTFIFO is HIGH), TXEN is assumed to be driven by the empty flag of an attached CY7C42X5 FIFO, and RXEN is assumed to be driven by the almost full flag of an attached CY7C42X5 FIFO. In this mode the active data transition is in the clock following the clock edge that “enables” the data bus. When not configured for external FIFOs (EXTFIFO is LOW), $\overline{\text{TXEN}}$ is assumed to be driven as a pipeline register and $\overline{\text{RXEN}}$ is assumed to be driven by a controller for a pipeline register. In this mode the active data transition is within the same clock as the clock edge that “enables” the data bus. EXTFIFO also modifies the output state of the Receive and Transmit FIFO flags. When configured for external FIFOs (EXTFIFO is HIGH), the Full and EMPTY FIFO flags are active HIGH (the Half full flag is always active LOW). When not configured for external FIFOs (EXTFIFO is LOW), all of the FIFO flags are active LOW.
27	$\overline{\text{ENCBYP}}$	Static control input TTL levels Normally wired HIGH or LOW	Enable Encoder Bypass mode. When asserted, both the encoder and decoder are bypassed. Data is transmitted without 4B/5B or 5B/6B encoding (but with NRZI encoding), LSB first. Received data are presented as parallel characters to the parallel interface without decoding. When deasserted, data is passed through both the encoder in the Transmit path and the decoder in the Receive path.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
Analog I/O and Control			
89, 90, 81, 82	OUTA± OUTB±	PECL compatible differential output	Differential Serial Data outputs. These PECL-compatible differential outputs are capable of driving terminated transmission lines or commercial fiberoptic transmitter modules. To minimize the power dissipation of unused outputs, the outputs should be left unconnected and the associated CURSETA or CURSETB should be connected to V_{DD}.
85, 86, 93, 94	INA± INB±	PECL compatible differential input	Differential Serial Data inputs. These inputs accept the serial data stream for deserialization and decoding. Only one serial stream at a time may be fed to the receive PLL to extract the data content. This stream is selected using the A/$\overline{B}$ input.
97	CURSETA	Analog	Current-set resistor input for OUTA±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTA± differential driver.
78	CURSETB	Analog	Current-set resistor input for OUTB±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTB± differential driver.
100	CARDET	PECL input, asynchronous	Carrier detect input. Used to allow an external device to signify a valid signal is being presented to the high speed PECL input buffers, as is typical on an Optical Module. When CARDET is deasserted LOW, the $\overline{LFI}$ indicator asserts LOW signifying a Link Fault. This input can be tied HIGH for copper media applications.
2	A/$\overline{B}$	Asynchronous TTL input	Input A or Input B selector. When HIGH, input INA± is selected, when LOW, INB± is selected.
3	$\overline{LFI}$	Three-state TTL output, changes following RXCLK↑	Link Fault Indication output. Active LOW. $\overline{LFI}$ changes synchronous with RXCLK. This output is driven LOW when the serial link currently selected by A/$\overline{B}$ is not suitable for data recovery. This could be because: 1. Serial Data Amplitude is below acceptable levels 2. Input transition density is not sufficient for PLL clock recovery 3. Input Data stream is outside an acceptable frequency range of operation 4. CARDET is LOW
5	DLB	Asynchronous TTL input	Diagnostic Loop Back selector. When DLB is LOW, LOOP Mode is OFF. Output of the transmitter shifter is routed to both OUTA± and OUTB± and the serial input selected by A/$\overline{B}$ is routed to the receive PLL for data recovery. When DLB is HIGH, Diagnostic Loopback is Enabled. Output of the transmitter serial data is routed to the receive PLL for data recovery. Primarily used for System Diagnostic test. The serial inputs are ignored and OUTA± and OUTB± are both active.
1	$\overline{TEST}$	Asynchronous TTL input normally wired HIGH	Test Mode select. Used to force the part into a diagnostic test mode used for factory ATE test. This input must be tied HIGH during normal operation.
Power			
80, 87, 88, 95, 96	V_{DDA}		Power for PECL compatible I/O signals and internal circuits.
76, 79, 83, 84, 91, 92, 99	V_{SSA}		Ground for PECL compatible I/O signals and internal circuits.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
14, 17, 35, 55, 62, 64	V_{DD}		Power for TTL I/O signals and internal circuits.
4,11, 13, 15, 26, 37, 38, 39, 52, 57, 63, 66	V_{SS}		Ground for TTL I/O signals and internal circuits.

Table 1. Transmit Input Bus Signal Map

TXDATA Bus Input Bit	Transmit Encoder Mode[1]			
	Encoded 8-bit Character Stream[2]	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream[3]	Pre-encoded 12-bit Character Stream
TXSC/$\overline{D}$	TXSC/$\overline{D}$		TXSC/$\overline{D}$	
TXDATA[0]	TXDATA[0]	TXD[0][4]	TXDATA[0]	TXD[0][5]
TXDATA[1]	TXDATA[1]	TXD[1]	TXDATA[1]	TXD[1]
TXDATA[2]	TXDATA[2]	TXD[2]	TXDATA[2]	TXD[2]
TXDATA[3]	TXDATA[3]	TXD[3]	TXDATA[3]	TXD[3]
TXDATA[4]	TXDATA[4]	TXD[4]	TXDATA[4]	TXD[4]
TXDATA[5]	TXDATA[5]	TXD[5]	TXDATA[5]	TXD[5]
TXDATA[6]	TXDATA[6]	TXD[6]	TXDATA[6]	TXD[6]
TXDATA[7]	TXDATA[7]	TXD[7]	TXDATA[7]	TXD[7]
TXDATA[8]/TXCMD[3]	TXCMD[3]	TXD[8]	TXDATA[8]	TXD[8]
TXDATA[9]/TXCMD[2]	TXCMD[2]	TXD[9]	TXDATA[9][3]	TXD[9]
TXCMD[1]	TXCMD[1]		TXCMD[1]	TXD[10][5]
TXCMD[0]	TXCMD[0]		TXCMD[0]	TXD[11]

Notes:

1. All open cells are ignored.
2. When ENCBYP is HIGH and BYTE8/$\overline{10}$ is HIGH, transmitted bit order is the encoded form (MSB to LSB) of TXDATA[7,6,5,4] and TXDATA[3,2,1,0] or TXCMD[3,2,1,0] as selected by TXSC/$\overline{D}$.
3. When ENCBYP is HIGH and BYTE8/10 is LOW, transmitted bit order is the encoded form (MSB to LSB) of TXDATA[8,7,6,5,4] and TXDATA[9,3,2,1,0] or TXCMD[1,0] as selected by TXSC/D.
4. When $\overline{ENCBYP}$ is LOW and BYTE8/$\overline{10}$ is HIGH, the transmitted bit order is (LSB to MSB) TXD[0,1,2,3,4,5,6,7,8,9].
5. When ENCBYP is LOW and BYTE8/10 is LOW, the transmitted bit order is (LSB to MSB) TXD[0,1,2,3,4,5,6,7,8,9,11,10].

Table 2. Receiver Output Bus Signal Map

RXDATA Bus Output Bit	Receiver Decoder Mode[1]			
	Encoded 8-bit Character Stream[7]	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream[8]	Pre-encoded 12-bit Character Stream
RXSC/$\overline{D}$	RXSC/$\overline{D}$		RXSC/$\overline{D}$	
RXDATA[0]	RXDATA[0]	RXD[0][6, 9]	RXDATA[0]	RXD[0][6, 10]
RXDATA[1]	RXDATA[1]	RXD[1]	RXDATA[1]	RXD[1]
RXDATA[2]	RXDATA[2]	RXD[2]	RXDATA[2]	RXD[2]
RXDATA[3]	RXDATA[3]	RXD[3]	RXDATA[3]	RXD[3]
RXDATA[4]	RXDATA[4]	RXD[4]	RXDATA[4]	RXD[4]
RXDATA[5]	RXDATA[5]	RXD[5]	RXDATA[5]	RXD[5]
RXDATA[6]	RXDATA[6]	RXD[6]	RXDATA[6]	RXD[6]
RXDATA[7]	RXDATA[7]	RXD[7]	RXDATA[7]	RXD[7]
RXDATA[8]/RXCMD[3]	RXCMD[3]	RXD[8]	RXDATA[8]	RXD[8]
RXDATA[9]/RXCMD[2]	RXCMD[2]	RXD[9]	RXDATA[9][8]	RXD[9]
RXCMD[1]	RXCMD[1]		RXCMD[1]	RXD[10][10]
RXCMD[0]	RXCMD[0]		RXCMD[0]	RXD[11]
VLTN	VLTN		VLTN	

Notes:

6. First bit shifted into the receiver.
7. When BYTE8/10 is HIGH, received bit order is decoded form the serial stream and presented (MSB to LSB) at RXDATA[7,6,5,4] and RXDATA[3,2,1,0] or RXCMD[3,2,1,0] as indicated by RXSC/D
8. When BYTE8/10 is LOW, received bit order is decoded form the serial stream and presented (MSB to LSB) at RXDATA[8,7,6,5,4] and RXDATA[9,3,2,1,0] or RXCMD[1,0] as indicated by RXSC/D
9. When ENCBYP is LOW and BYTE8/10 is HIGH, the received bit order is (LSB to MSB) RXD[0,1,2,3,4,5,6,7,8,9].
10. When ENCBYP is LOW and BYTE8/10 is LOW, the received bit order is (LSB to MSB) RXD[0,1,2,3,4,5,6,7,8,9,11,10].

CY7C9689 HOTLink Operation

Overview

The CY7C9689 is designed to move parallel data across both short and long distances with minimal overhead or host system intervention. This is accomplished by converting the parallel characters into a serial bit-stream, transmitting these serial bits at high speed, and converting the received serial bits back into the original parallel data format.

The CY7C9689 offers a large feature set, allowing it to be used in a wide range of host systems. Some of the of configuration options are

- AMD TAXIchip 4B/5B & 5B/6B compatible encoder/decoder
- AMD TAXIchip compatible serial link
- AMD TAXIchip parallel COMMAND and DATA I/O bus architecture
- 8-bit or 10-bit character size
- User-definable data packet or frame structure
- Two-octave data rate range
- Asynchronous (FIFOed) or synchronous data interface
- Embedded or bypassable FIFO data storage
- Encoded or non-encoded
- Multi-PHY capability

This flexibility allows the CY7C9689 to meet the data transport needs of almost any system.

Transmit Data Path

Transmit Data Interface/Transmit Data FIFO

The transmit data interface to the host system is configurable as either an asynchronous buffered (FIFOed) parallel interface or as a synchronous pipeline register. The bus itself can be configured for operation with either 8-bit or 10-bit character widths.

When configured for asynchronous operation (where the host-bus interface clock operates asynchronous to the serial character and bit stream clocks), the host interface becomes that of a synchronous FIFO clocked by TXCLK. In this configuration an internal 256 character Transmit FIFO is enabled that allows the host interface to be written at any rate from DC to 50 MHz.

When configured for synchronous operation, the transmit interface is clocked by REFCLK and operates synchronous to the internal character and bit-stream clocks. The input register can be written at either 1/10th or 1/12th the serial bit rate. This interface can be clocked at up to 40 MHz when configured for 8-bit data width, and up to 33 MHz when configured for 10-bit data bus width. Actual clock rate depends on data rate as well as RANGESEL and SPDSEL logic levels.

Both asynchronous and synchronous interface operations support user control over the logical sense of the FIFO status flags. Full and empty flags on both the transmitter and receiver can be active HIGH or active LOW. This facilitates interfacing

with existing control logic or external FIFOs with minimal or no external glue logic.

Encoder

Data from the host interface or Transmit FIFO is next passed to an Encoder block. The CY7C9689 contains both 4B/5B and 5B/6B encoders that are used to improve the serial transport characteristics of the data. For those systems that contain their own encoder or scrambler, this Encoder may be bypassed.

Serializer/Line Driver

The data from the Encoder is passed to a Serializer. This Serializer operates at 10 or 12 times the character rate. With the internal FIFOs enabled, REFCLK can run at 1x, 2x, or 4x the character rate. With the FIFOs bypassed, REFCLK can operate at 1x or 2x the character rate. The serialized data is output in NRZI format from two PECL-compatible differential line drivers configured to drive transmission lines or optical modules.

Receive Data Interface

Line Receiver/Deserializer/Framer

Serial data is received at one of two PECL-compatible differential line receivers. The data is passed to both a Clock and Data Recovery Phase Locked Loop (PLL) and to a Deserializer that converts NRZI serial data into NRZ parallel characters. The Framer adjusts the boundaries of these characters to match those of the original transmitted characters.

Decoder

The parallel characters are passed through a pair of 5B/4B or 6B/5B Decoders and returned to their original form. For systems that make use of external decoding or descrambling, the decoder may be bypassed.

Receive Data Interface/Receive Data FIFO

Data from the decoder is passed either to a synchronous Receive FIFO or is passed directly to the output register. The output register can be configured for either 8-bit character or 10-bit character operation.

When configured for an asynchronous buffered (FIFOed) interface, the data is passed through a 256-character Receive FIFO that allows data to be read at any rate from DC to 50 MHz. When configured for synchronous operation (Receive FIFO is bypassed) data is clocked out of the Receive Output register at up to 20 MHz when configured for 8-bit characters, or 16.67 MHz when configured for 10-bit characters. The receive interface is also configurable for FIFO flags with either HIGH or LOW status indication

Oscillator Speed Selection

The CY7B9689 is designed to operate over a two-octave range of serial signaling rates, covering the 50- to 200-MBaud range. To cover this wide range, the PLLs are configured into various sub-regions using the SPDSEL and RANGESEL inputs, and to a limited extent the BYTE8/$\overline{10}$ input. These inputs are used to configure the various prescalers and clock dividers used with the transmit and receive PLLs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with (Power Applied) –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +6.5V

DC Voltage Applied to Outputs..... –0.5V to V_{DD}+0.5V

Output Current into TTL Outputs (LOW) ..... 30 mA

DC Input Voltage ..... –0.5V to V_{DD}+0.5V

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5.0V ± 10%
Industrial	–40°C to +85°C	5.0V ± 10%

CY7C9689 DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
TTL Outputs						
V_{OHT}	Output HIGH Voltage	I_{OH} = –2 mA, V_{DD} = Min		2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 8 mA, V_{DD} = Min			0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[11]		–30	–80	mA
TTL Inputs						
V_{IHT}	Input HIGH Voltage			2.0		V
V_{ILT}	Input LOW Voltage				0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{DD}			±40	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0V			± 40	µA
I_{ILPUT}	Input LOW Current with Internal Pull-Up	V_{IN} = 0.0V			–500	µA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA–, OUTB+, OUTB–						
V_{OHE}	Output HIGH Voltage (V_{DD} referenced)	Load = 50Ω to V_{DD} – 1.33V R_{CURSET}=TBD		V_{DD}–1.03	V_{DD}–0.83	V
V_{OLE}	Output LOW Voltage (V_{DD} referenced)	Load = 50Ω to V_{DD} – 1.33V R_{CURSET}=TBD		V_{DD}–2.0	V_{DD}–1.62	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	Load = 50 ohms to V_{DD} – 1.33V R_{CURSET}=TBDmin – TBDmax		600	1100	mV
Receiver Single-ended PECL-Compatible Input Pin: CARDET						
V_{IHE}	Input HIGH Voltage (V_{DD} referenced)			V_{DD}–1.165	V_{DD}	V
V_{ILE}	Input LOW Voltage (V_{DD} referenced)			2.5	V_{DD}–1.475	V
Receiver Differential Line Receiver Input Pins: INA+, INA–, INB+, INB–						
V_{DIFF}	Input Differential Voltage |(IN+) – (IN–)|			200	2500	mV
V_{IHH}	Highest Input HIGH Voltage				V_{DD}	V
V_{ILL}	Lowest Input LOW Voltage			2.5		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.			750	µA
I_{ILL}[12]	Input LOW Current	V_{IN} = V_{ILL} Min.		–200		µA
Miscellaneous				**Typ.**	**Max.**	
I_{DD}[13]	Power Supply Current	Freq. = Max.	Commercial	TBD	250	mA

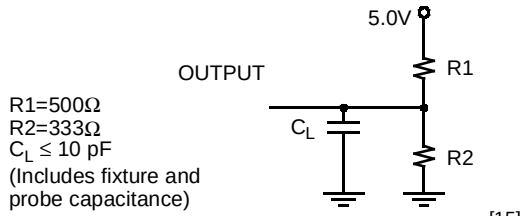
Capacitance[14]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{DD} = 5.0V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{DD} = 5.0V	4	pF

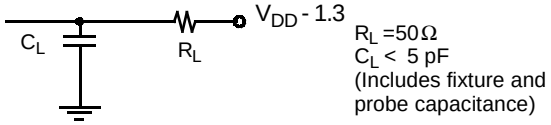
Notes:

11. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
12. To guarantee positive currents for all PECL voltages, an external pull-down resistor must be present.
13. Maximum I_{CC} is measured with V_{DD} = MAX, RFEN = LOW, and outputs unloaded. Typical I_{DD} is measured with V_{DD} = 5.0V, T_A = 25°C, RFEN = LOW, and outputs unloaded.
14. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.

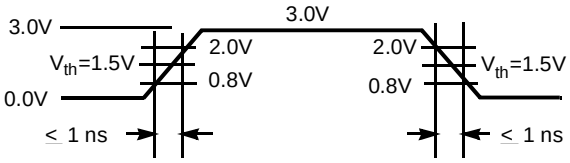
AC Test Loads and Waveforms



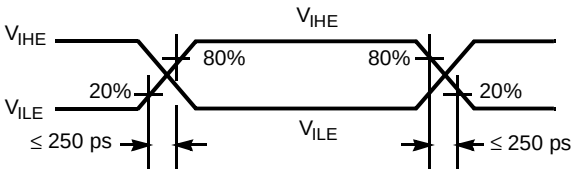
(a) TTL AC Test Load[15]



(b) PECL AC Test Load[15]



(c) TTL Input Test Waveform



(d) PECL Input Test Waveform

CY7C9689 Transmitter TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min.	Max	Unit
f_{TS}	TXCLK Clock Cycle Frequency With Transmit FIFO Enabled		50	MHz
t_{TXCLK}	TXCLK Period	20		ns
t_{TXCPWH}	TXCLK HIGH Time	6.5		ns
t_{TXCPWL}	TXCLK LOW Time	6.5		ns
t_{TXCLKR}	TXCLK Rise Time	0.7	5	ns
t_{TXCLKF}	TXCLK Fall Time	0.7	5	ns
t_{TXA}	Flag Access Time From TXCLK↑ to output	4	15	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLK↑	4		ns
t_{TXDH}	Transmit Data Hold Time from TXCLK↑	1		ns
t_{TXENS}	Transmit Enable Set-Up Time to TXCLK↑	4		ns
t_{TXENH}	Transmit Enable Hold Time from TXCLK↑	1		ns
t_{TXRSS}	Transmit FIFO Reset ($\overline{TXRST}$) Set-Up Time to TXCLK↑	4		ns
t_{TXRSH}	Transmit FIFO Reset ($\overline{TXRST}$ Hold Time from TXCLK↑	1		ns
t_{TXCES}	Transmit Chip Enable ($\overline{CE}$) Set-Up Time to TXCLK↑	4		ns
t_{TXCEH}	Transmit Chip Enable ($\overline{CE}$) Hold Time from TXCLK↑	1		ns
t_{TXZA}	Sample of $\overline{CE}$ LOW by TXCLK↑, Output High-Z to active HIGH or LOW	0		ns
t_{TXOE}	Sample of $\overline{CE}$ LOW by TXCLK↑ to Output Valid	2	20	ns
t_{TXAZ}	Sample of $\overline{CE}$ HIGH by TXCLK↑ to Output in High-Z	2	20	ns

Note:
15. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.

CY7C9689 Receiver TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min.	Max	Unit
f_{RIS}	RXCLK Clock Cycle Frequency With Receive FIFO Enabled		50	MHz
$t_{RXCLKIP}$	RXCLK Input Period	20		ns
t_{RXCPWH}	RXCLK Input HIGH Time	6.5		ns
t_{RXCPWL}	RXCLK Input LOW Time	6.5		ns
$t_{RXCLKIR}$	RXCLK Input Rise Time	0.7	5	ns
$t_{RXCLKIF}$	RXCLK Input Fall Time	0.7	5	ns
t_{RXENS}	Receive Enable Set-Up Time to RXCLK↑	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK↑	1		ns
t_{RXRSS}	Receive FIFO Reset ($\overline{RXRXT}$) Set-Up Time to RXCLK↑	4		ns
t_{RXRSH}	Receive FIFO Reset ($\overline{RXRXT}$) Hold Time from RXCLK↑	1		ns
t_{RXCES}	Receive Chip Enable ($\overline{CE}$) Set-Up Time to RXCLK↑	4		ns
t_{RXCEH}	Receive Chip Enable ($\overline{CE}$) Hold Time from RXCLK↑	1		ns
t_{RXA}	Flag and Data Access Time From RXCLK↑ to Output	4	15	ns
t_{RXZA}	Sample of $\overline{CE}$ LOW by RXCLK↑, Output High-Z to Active HIGH or LOW,[16] or Sample of RXEN Asserted by RXCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{RXOE}	Sample of $\overline{CE}$ LOW by RXCLK↑ to Output Valid,[16] or Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs Valid	2	20	ns
t_{RXZA}	Sample of $\overline{CE}$ HIGH by RXCLK↑ to Output in High-Z,[16] or Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs in High-Z	2	20	ns

Note:
16. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

CY7C9689 Transmitter TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max	Unit
t_{TRA}	Flag Access Time From REFCLK↑ to Output	4	15	ns
t_{REFDS}	Write Data Set-Up Time to REFCLK↑	4		ns
t_{REFDH}	Write Data Hold Time from REFCLK↑	1		ns
t_{REFENS}	Transmit Enable Set-Up Time to REFCLK↑	4		ns
t_{REFENH}	Transmit Enable Hold Time from REFCLK↑	1		ns
t_{REFCES}	Transmit Chip Enable ($\overline{CE}$) Set-Up Time to REFCLK↑	4		ns
t_{REFCEH}	Transmit Chip Enable ($\overline{CE}$) Hold Time from REFCLK↑	1		ns
t_{REFZA}	Sample of $\overline{CE}$ LOW by REFCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{REFOE}	Sample of $\overline{CE}$ LOW by REFCLK↑ to Flag Output Valid	2	20	ns
t_{REFAZ}	Sample of $\overline{CE}$ HIGH by REFCLK↑ to Flag Output High-Z	2	20	ns

CY7C9689 Receiver TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max	Unit
f_{ROS}[17]	RXCLK Clock Output Frequency—100 to 200 MBaud 8-bit Operation (SPDSEL is HIGH and BYTE8/$\overline{10}$ is HIGH)	10	20	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud 8-bit Operation (SPDSEL is LOW and BYTE8/$\overline{10}$ is HIGH)	5	10	MHz
	RXCLK Clock Output Frequency—100 to 200 MBaud 10-bit Operation (SPDSEL is HIGH and BYTE8/$\overline{10}$ is LOW)	8.33	16.67	MHz
	RXCLK Clock Output Frequency—50 to 100 MBaud 10-bit Operation (SPDSEL is LOW and BYTE8/$\overline{10}$ is LOW)	4.16	8.33	MHz
$t_{RXCLKOP}$	RXCLK Output Period	25	240	ns
$t_{RXCLKOD}$	RXCLK Output Duty Cycle	40	60	%
$t_{RXCLKOR}$	RXCLK Output Rise Time	0.5	2	ns
$t_{RXCLKOF}$	RXCLK Output Fall Time	0.5	2	ns
t_{RXENS}	Receive Enable Set-Up Time to RXCLK↑	4		ns
t_{RXENH}	Receive Enable Hold Time from RXCLK↑	1		ns
t_{RXZA}	Sample of $\overline{CE}$ LOW by RXCLK↑, Outputs High-Z to Active Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs High-Z to Active	0		ns
t_{RXOE}	Sample of $\overline{CE}$ LOW by RXCLK↑ to Flag Output Valid Sample of RXEN Asserted by RXCLK↑ to RXDATA Output Low-Z	2	20	ns
t_{RXAZ}	Sample of $\overline{CE}$ HIGH by RXCLK↑ to Flag Output High-Z Sample of RXEN Deasserted by RXCLK↑ to RXDATA Output High-Z	2	20	ns

Notes:

17. The period of t_{ROS} will match the period of the transmitter PLL reference (REFCLK) when receiving serial data. When data is interrupted, RXCLK may drift to REFCLK ±0.2%.

CY7C9689 REFCLK Input Switching Characteristics Over the Operating Range

Parameter	Description	Conditions			Min.	Max	Unit
		SPD-SEL	RANGE-SEL	BYTE8/$\overline{10}$			
f_{REF}	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit Mode, REFCLK = 2x Character Rate	0	0	0	8.33	16.67	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit Mode, REFCLK = 2x Character Rate	0	0	1	10	20	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 10-bit Mode, REFCLK = 4x Character Rate	0	1[18]	0	16.67	33.3	MHz
	REFCLK Clock Frequency—50 to 100 MBaud, 8-bit Mode, REFCLK = 4x Character Rate	0	1[18]	1	20	40	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit Mode, REFCLK = Character Rate	1	0	0	20	40	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit Mode, REFCLK = Character Rate	1	0	1	10	20	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 10-bit Mode, REFCLK = 2x Character Rate	1	1	0	16.67	33.3	MHz
	REFCLK Clock Frequency—100 to 200 MBaud, 8-bit Mode, REFCLK = 2x Character Rate	1	1	1	8.33	16.67	MHz
t_{REFCLK}	REFCLK Period				25	120	ns
t_{REFH}	REFCLK HIGH Time				6.5		ns
t_{REFL}	REFCLK LOW Time				6.5		ns
t_{REFRX}	REFCLK Frequency Referenced to Received Clock Period[19]				–0.04	+0.04	%

CY7C9689 PECL Input/Output Switching Characteristics Over the Operating Range

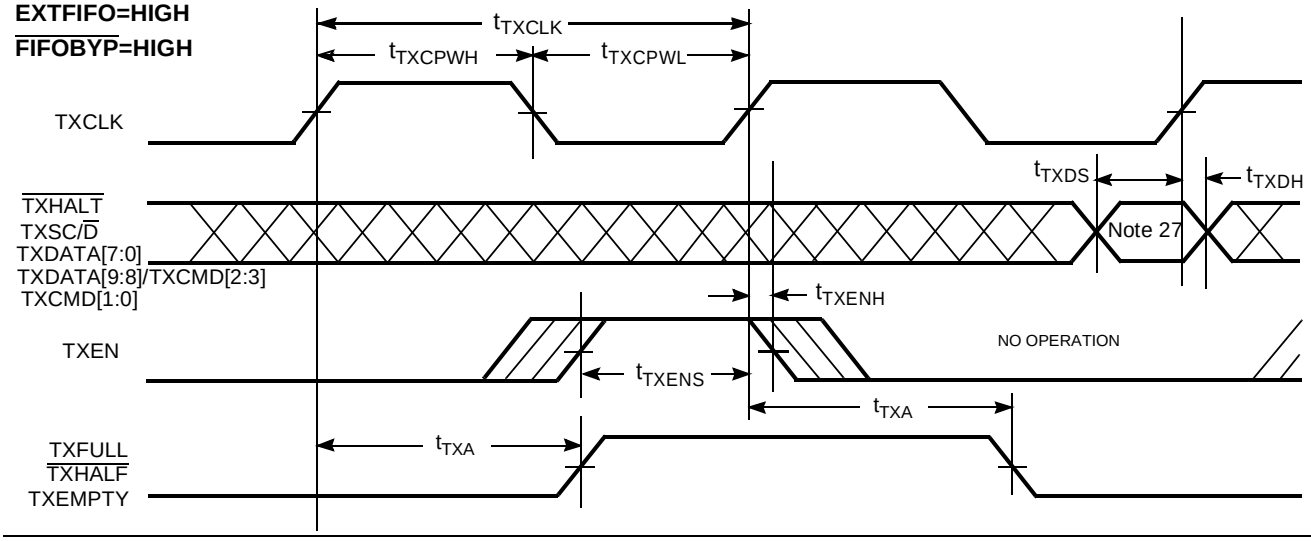
Parameter	Description	Min.	Max	Unit
t_B	Bit Time	20.0	5.0	ns
t_{SA}	Static Alignment[14, 23]	TBD	TBD	ps
t_{EFW}	Error Free Window[14, 20, 24]	0.75		UI
t_{RISE}	PECL Output Rise Time 20–80% (PECL Test Load)[14]	200	1700	ps
t_{FALL}	PECL Output Fall Time 80–20% (PECL Test Load)[14]	200	1700	ps
t_{DJ}	Deterministic Jitter (peak-peak)[14, 25]		TBD	ps
t_{RJ}	Random Jitter (σ) [14, 26]		TBD	ps
t_{JT}	Transmitter Total Output Jitter (peak-peak)[14]		TBD	ps

Notes:

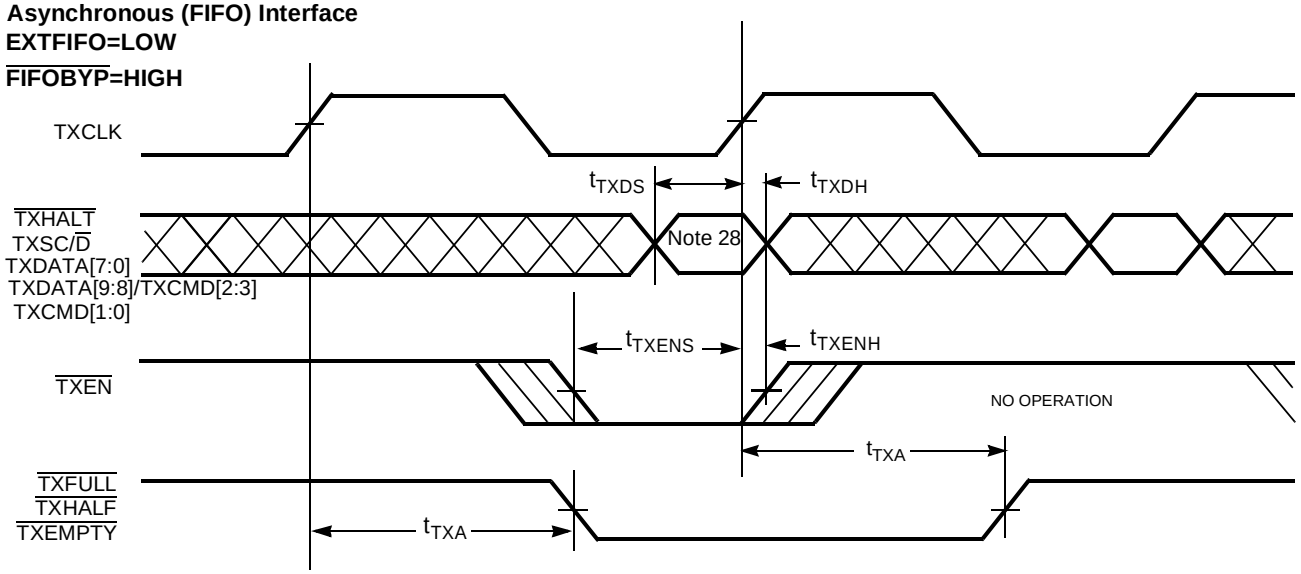
18. When configured for synchronous operation with the FIFOs bypassed ($\overline{\text{FIFOBYP}}$ is LOW), if RANGESEL is HIGH the SPDSEL input is ignored and operation is forced to the 100–200 MBaud range
19. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±0.04% of the transmitter PLL reference (REFCLK) frequency, necessitating a ±200-PPM crystal.
20. Receiver UI (Unit Interval) is calculated as ($1/f_{REF}$) if no data is being received, or ($1/f_{REF}$) of the remote transmitter if data is being received. In an operating link this is equivalent to 10 * t_B.
21. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.
22. The PECL switching threshold is the midpoint between the PECL– V_{OH}, and V_{OL} specification (approximately V_{DD} – 1.33V).
23. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a character error occurs.
24. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.
25. While sending continuous JK, outputs loaded to 50Ω to V_{DD}–1.3V, over the operating range.
26. While sending continuous HH, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.

CY7C9689 HOTLink Transmitter Switching Waveforms

Write Cycle
Asynchronous (FIFO) Interface
EXTFIFO=HIGH
$\overline{\text{FIFOBYP}}$=HIGH



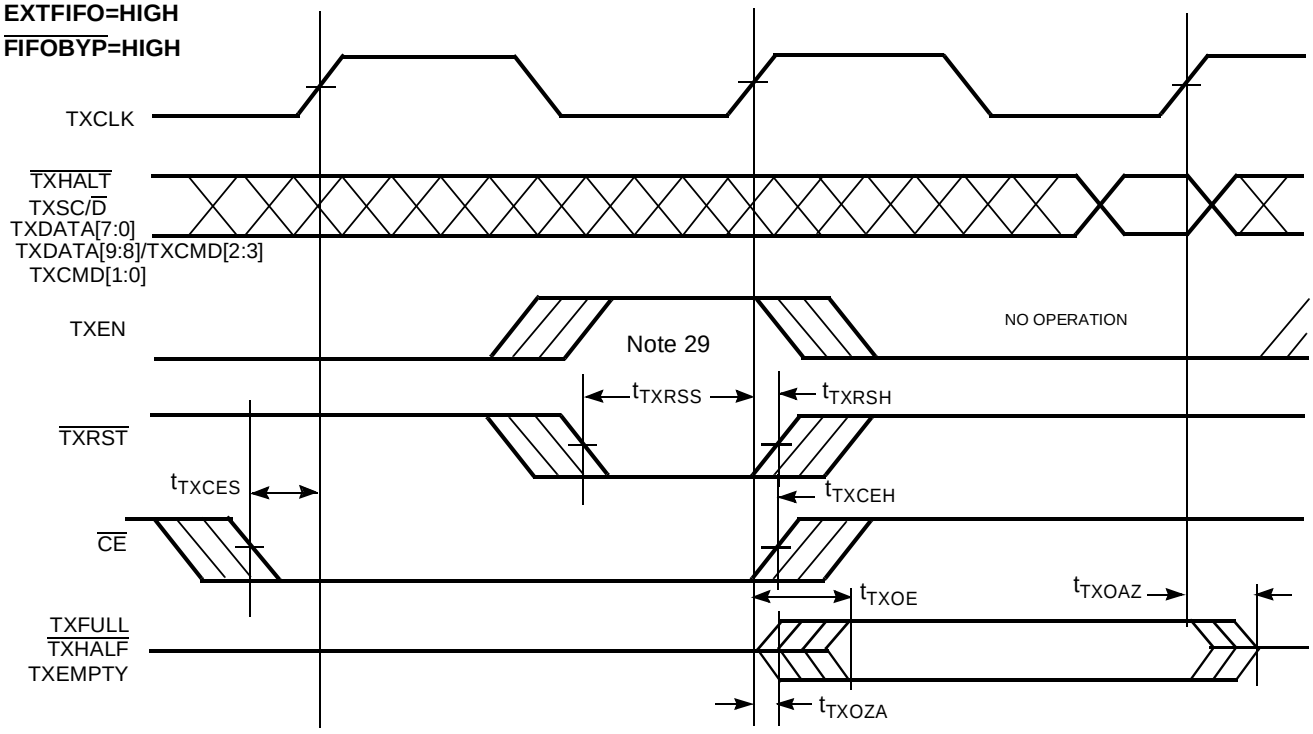
Write Cycle
Asynchronous (FIFO) Interface
EXTFIFO=LOW
$\overline{\text{FIFOBYP}}$=HIGH



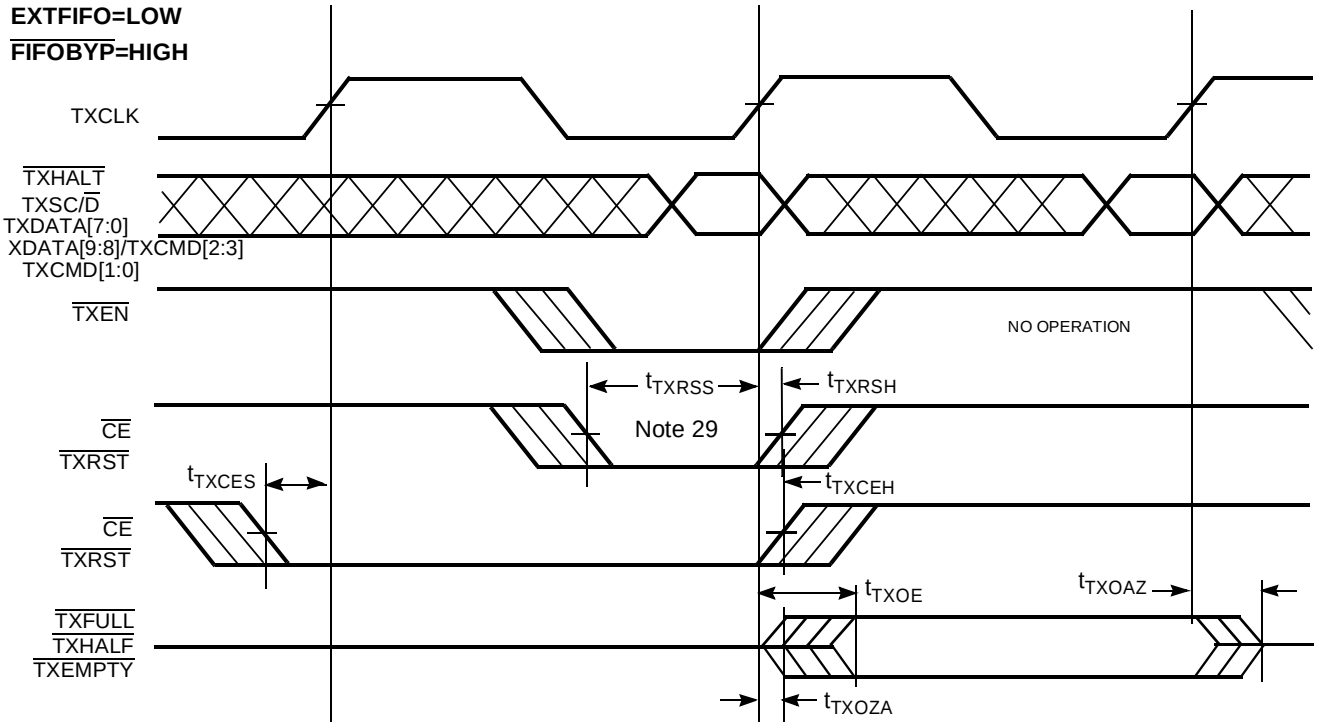
Notes:
27. When EXTFIFO is HIGH, the write data is captured on the clock cycle following TXEN = HIGH.
28. When EXTFIFO is LOW, the write data is captured on the same clock cycle as the TXEN=LOW.

CY7C9689 HOTLink Transmitter Switching Waveforms (continued)

OUTPUT ENABLE Timing
Asynchronous (FIFO) Interface
EXTFIFO=HIGH
$\overline{\text{FIFOBYP}}$=HIGH



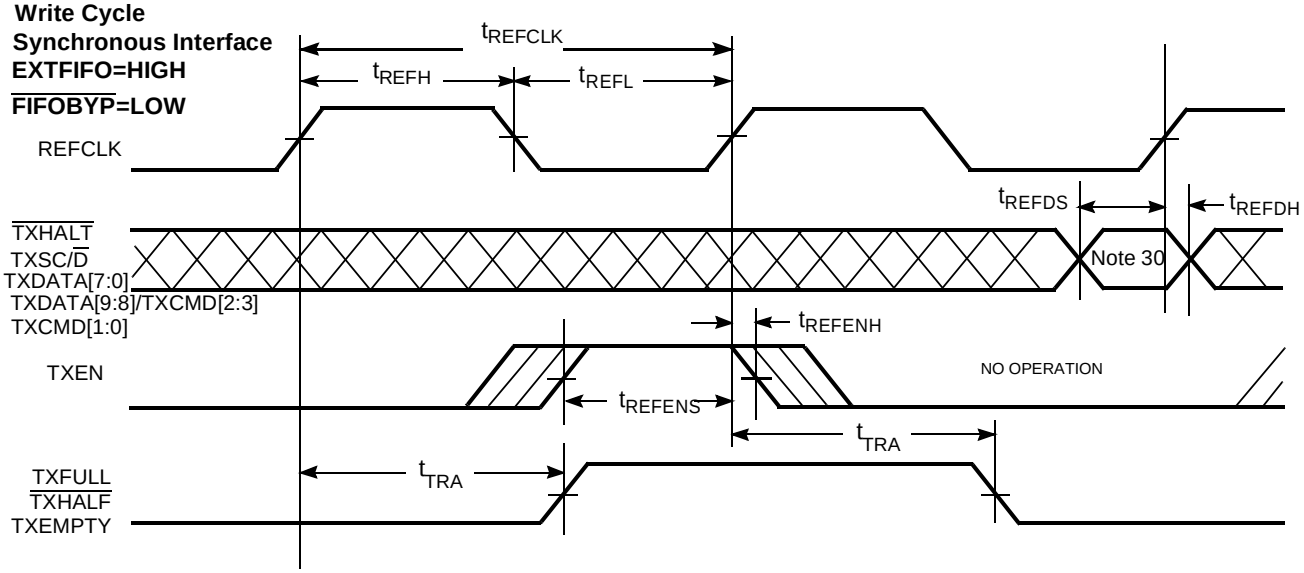
OUTPUT ENABLE Timing
Asynchronous (FIFO) Interface
EXTFIFO=LOW
$\overline{\text{FIFOBYP}}$=HIGH



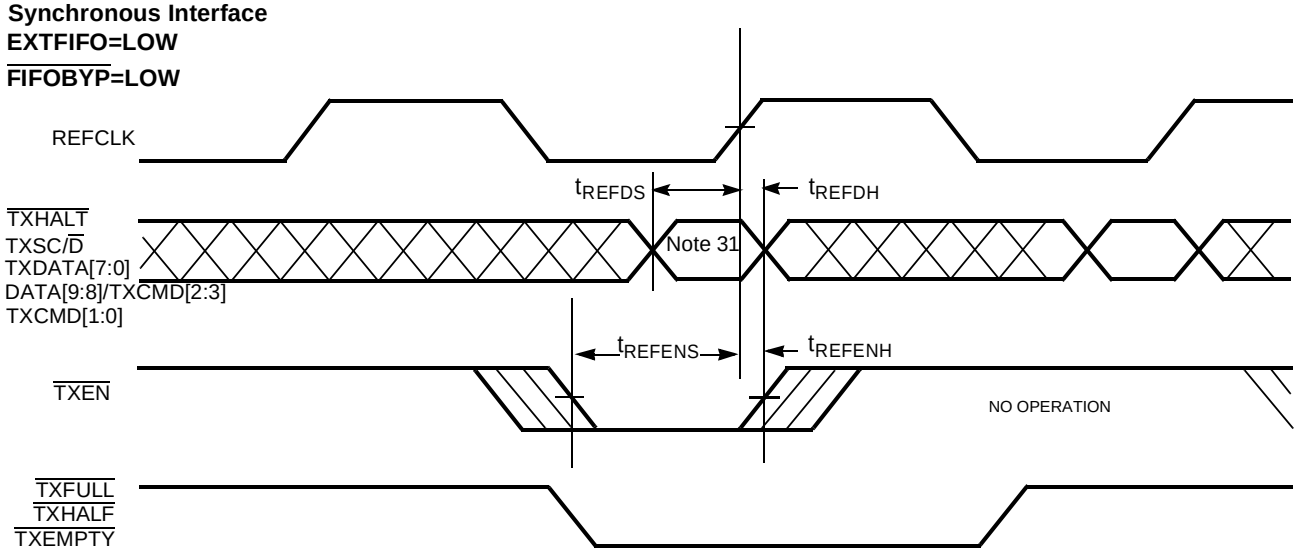
Note:
29. Illustrates timing only. TXEN and $\overline{\text{TXRST}}$ not usually active in same time period.

CY7C9689 HOTLink Transmitter Switching Waveforms (continued)

Write Cycle
Synchronous Interface
EXTFIFO=HIGH
$\overline{\text{FIFOBYP}}$=LOW



Write Cycle
Synchronous Interface
EXTFIFO=LOW
$\overline{\text{FIFOBYP}}$=LOW

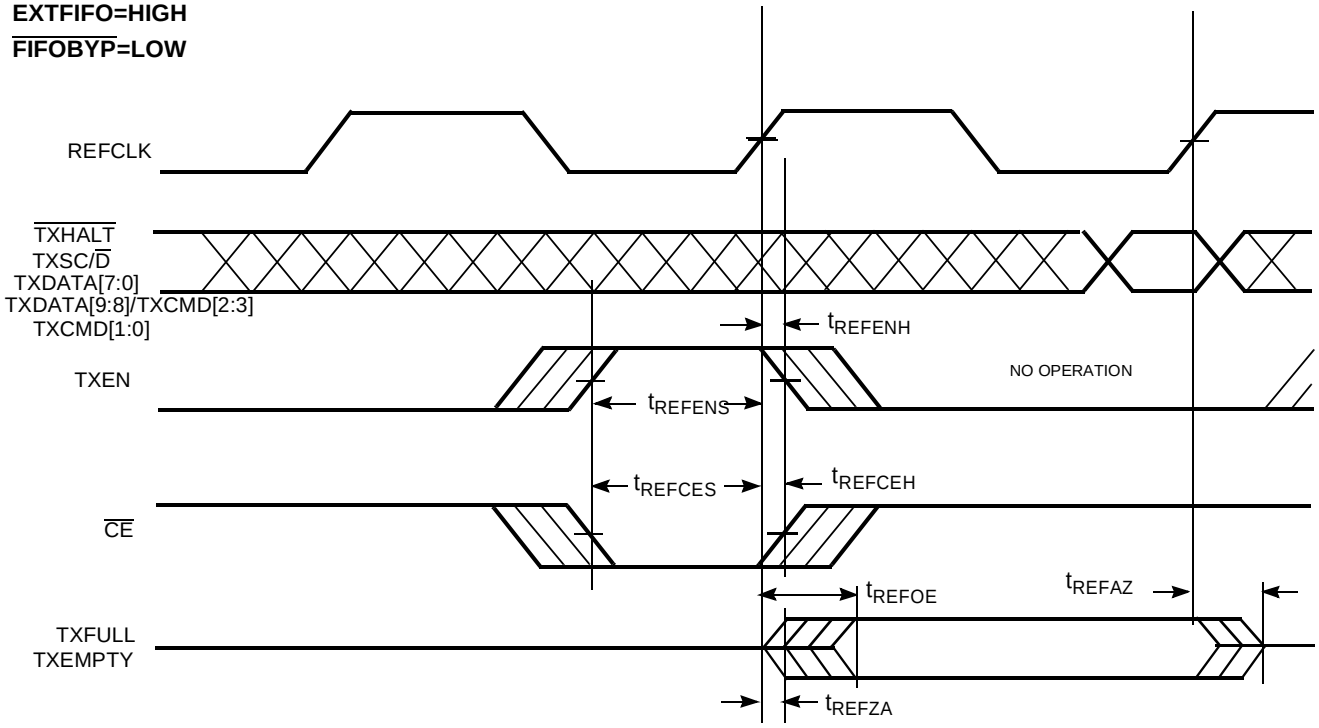


Notes:

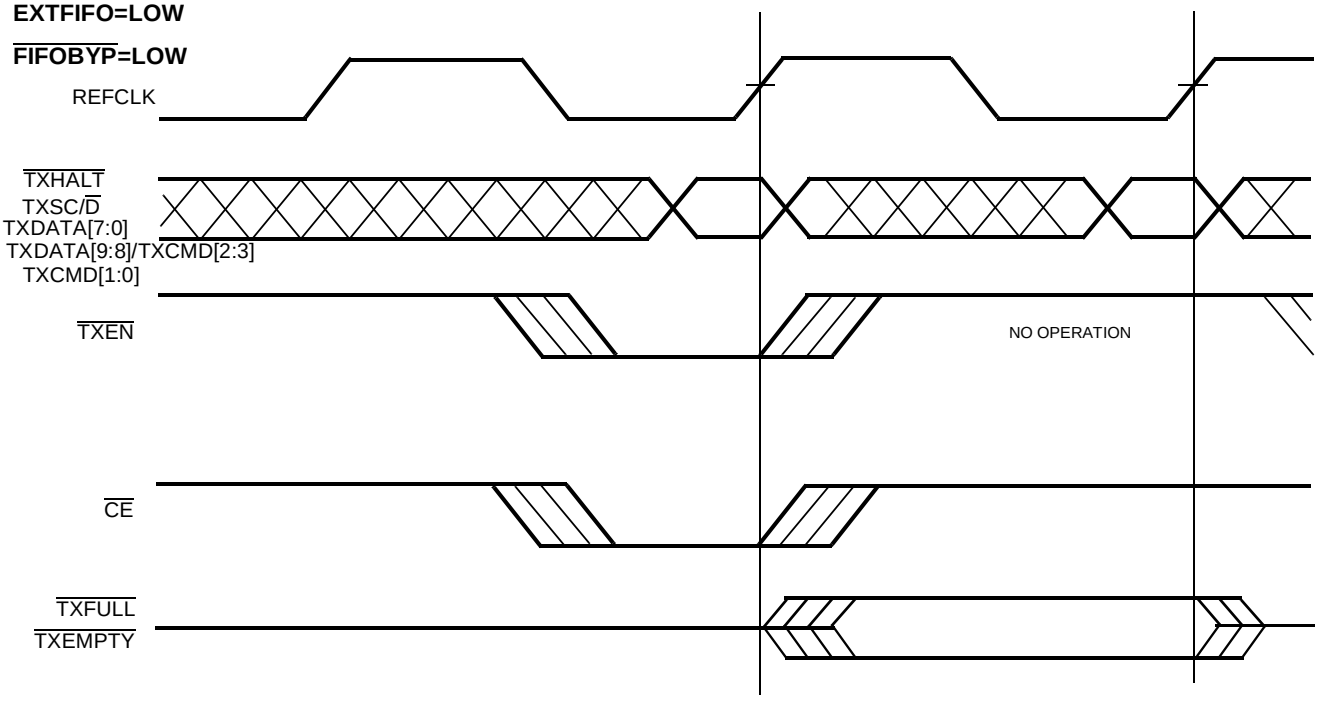
30. When transferring data to the Transmitter input from a depth expanded external FIFO, the data is captured from the external FIFO one clock cycle following the actual enable (TXEN = HIGH).
31. When transferring data to the Transmitter input from a synchronous external controller, the data is captured in the same clock cycle as the actual enable (TXEN = LOW).

CY7C9689 HOTLink Transmitter Switching Waveforms (continued)

OUTPUT ENABLE Timing
Synchronous Interface
EXTFIFO=HIGH
$\overline{\text{FIFOBYP}}$=LOW

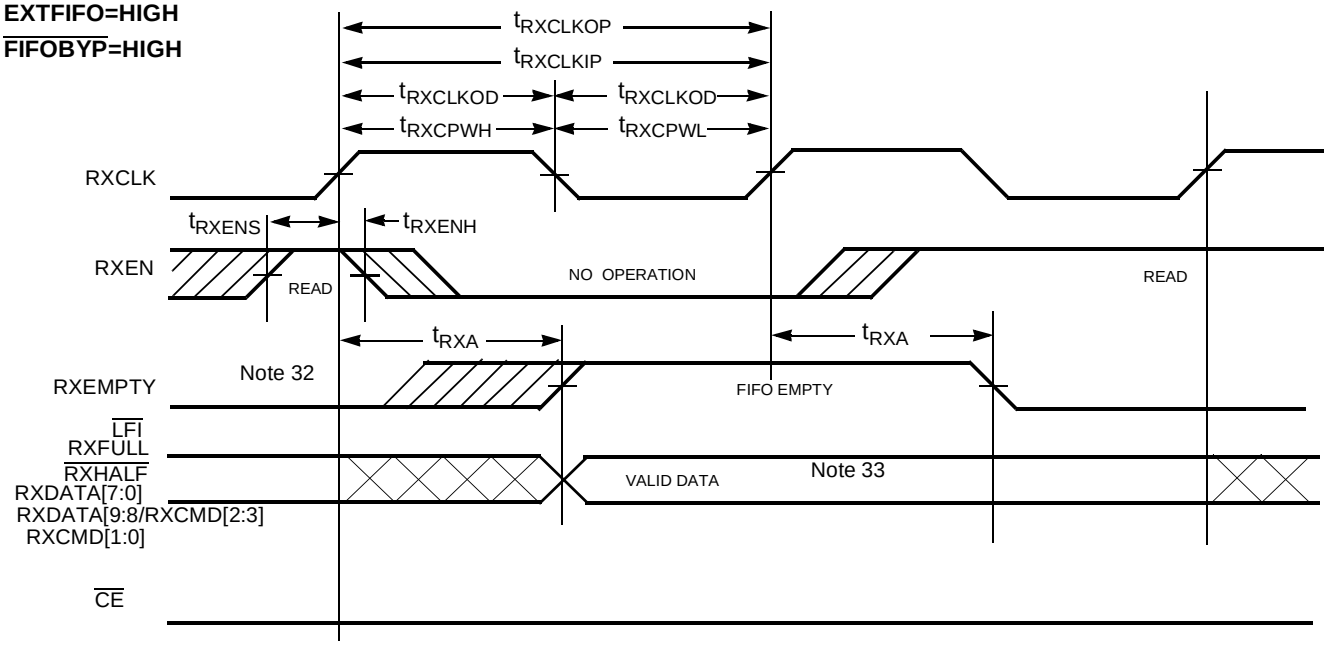


OUTPUT ENABLE Timing
Synchronous Interface
EXTFIFO=LOW
$\overline{\text{FIFOBYP}}$=LOW

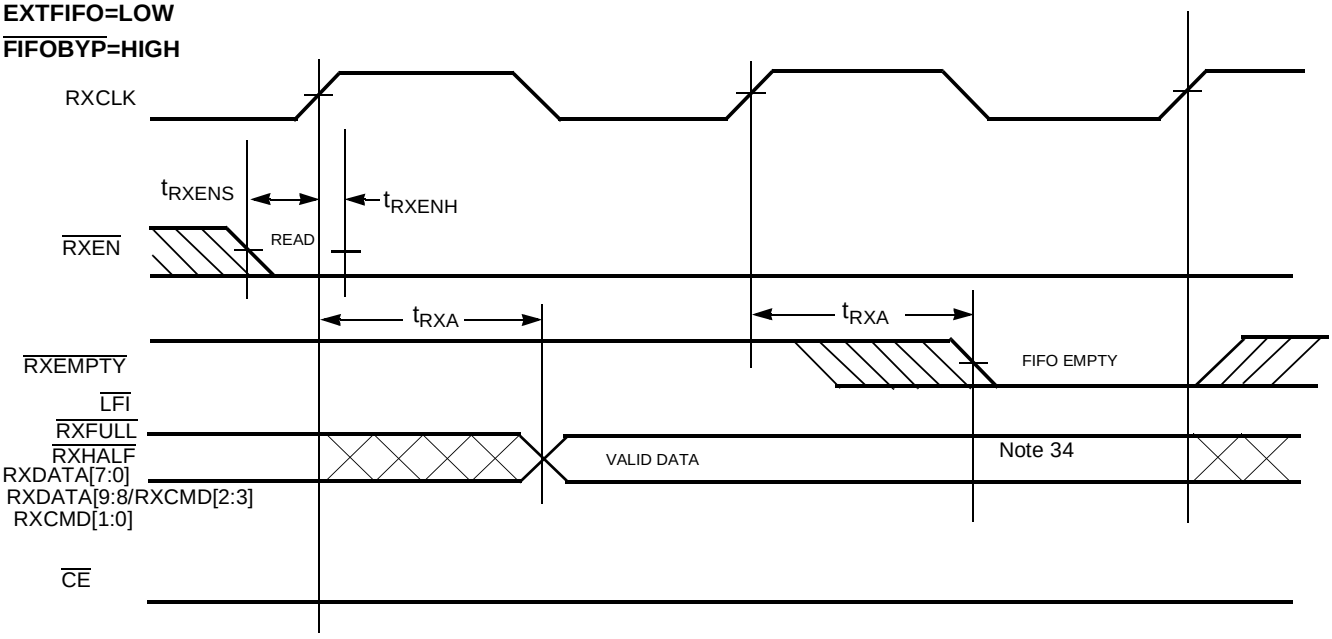


CY7C9689 HOTLink Receiver Switching Waveforms

Read Cycle
Asynchronous (FIFO) Interface
EXTFIFO=HIGH
$\overline{\text{FIFOBYP}}$=HIGH



Read Cycle
Asynchronous (FIFO) Interface
EXTFIFO=LOW
$\overline{\text{FIFOBYP}}$=HIGH

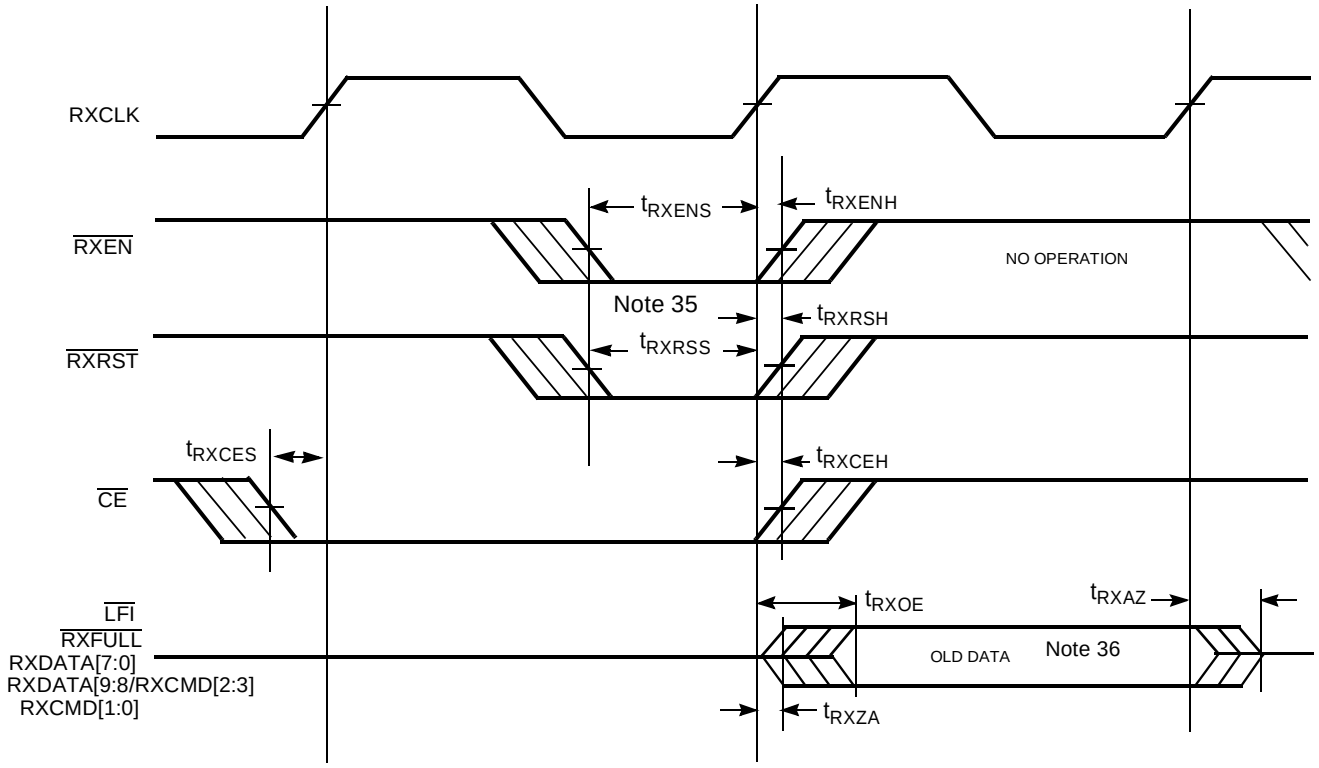


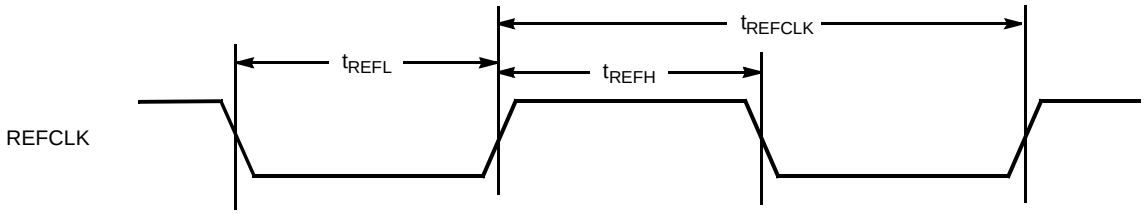
Notes:

32. When transferring data from the Receive FIFO to a depth expanded external FIFO, the data is sent to the external FIFO on the same clock cycle that RXEN=HIGH. RXEMPTY=LOW indicates that data is available.
33. On inhibited reads, or if the Receive FIFO goes empty, the data outputs do not change.
34. When reading data from synchronous data interface, the data is captured on any clock cycle that $\overline{\text{RXEN}}$=LOW. $\overline{\text{RXEMPTY}}$=HIGH indicates data is available. $\overline{\text{RXEMPTY}}$=LOW indicates that the FIFO is empty.

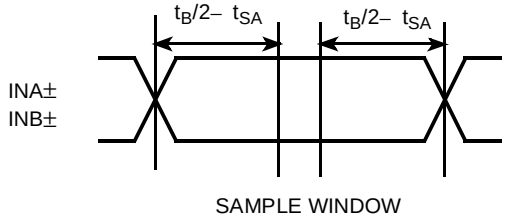
CY7C9689 HOTLink Receiver Switching Waveforms (continued)

Output Enable Timing

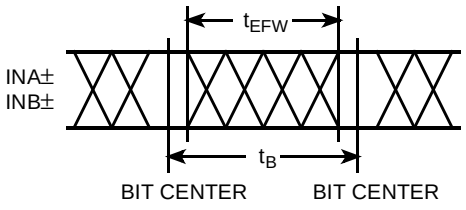




Static Alignment



Error-Free Window



Notes:
35. Illustrates timing only. RXEN and $\overline{\text{RXRST}}$ not usually active in same time period.
36. Receive FIFO Reads are inhibited while the outputs are High-Z.

Table 3. HOTLink TAXI Compatible Encoder Patterns

4B/5B Encoder			5B/6B Encoder		
HEX Data	4-bit Binary Data[37]	5-bit Encoded Symbol[38,39]	HEX Data	5-bit Binary Data[37]	6-bit Encoded Symbol[38,39]
0	0000	11110	00	00000	110110
1	0001	01001	01	00001	010001
2	0010	10100	02	00010	100100
3	0011	10101	03	00011	100101
4	0100	01010	04	00100	010010
5	0101	01011	05	00101	010011
6	0110	01110	06	00110	010110
7	0111	01111	07	00111	010111
8	1000	10010	08	01000	100010
9	1001	10011	09	01001	110001
A	1010	10110	0A	01010	110111
B	1011	10111	0B	01011	100111
C	1100	11010	0C	01100	110010
D	1101	11011	0D	01101	110011
E	1110	11100	0E	01110	110100
F	1111	11101	0F	01111	110101
			10	10000	111110
			11	10001	011001
			12	10010	101001
			13	10011	101101
			14	10100	011010
			15	10101	011011
			16	10110	011110
			17	10111	011111
			18	10001	101010
			19	11001	101011
			1A	11010	101110
			1B	11011	101111
			1C	11100	111010
			1D	11101	111011
			1E	11110	111100
			1F	11111	111101

Notes:

37. Binary Input Data is the parallel input data which is input to the Transmitter and output from the Receiver. Binary bits are listed from left to right in the following order:
    8-Bit mode (BYTE8/$\overline{10}$ is HIGH and TXSC/$\overline{D}$ or RXSC/$\overline{D}$ is LOW)—TXDATA/RXDATA[7], [6], [5], [4], and TXDATA/RXDATA[3], [2], [1], [0].
    10-Bit mode (BYTE8/$\overline{10}$ is LOW and TXSC/$\overline{D}$ or RXSC/$\overline{D}$ is LOW)—TXDATA/RXDATA[8], [7], [6], [5], [4], and TXDATA/RXDATA[9], [3], [2], [1], [0].
38. The ENCODED Symbols are shown here as “ones and zeros”, but are converted to and from an NRZI stream at the transmitter output and receiver input. NRZI represents a “one” as a state transition (either LOW-to-HIGH or HIGH-to-LOW) and a “zero” as no transition within the bit interval.
39. Encoded Serial Symbol bits are shifted out with the most significant bit (Left-most) of the most significant nibble coming out first.

Table 4. HOTLink TAXI Compatible Command Symbols

CY7C9689 (Transmitter) Command Input TXCMD[3:0]				CY7C9689 (Receiver) Command Output RXCMD[3:0]	
HEX	**Binary CMD[40]**	**Encoded Symbol[38, 39]**	**Mnemonic**	**HEX**	**Binary CMD[40]**
8-bit mode (BYTE8/$\overline{10}$ is HIGH)					
0	0000	11000 10001	JK (8-bit SYNC)	0	0000
1	0001	11111 11111	II	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	IH	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8[41]	1000	00100 00100	HH	8	1000
9[41]	1001	00100 11111	HI	9	1001
A[41]	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D[41]	1101	00000 00100	QH	D	1101
E[41]	1110	00000 11111	QI	E	1110
F[41]	1111	00000 00000	QQ	F	1111
10-bit mode (BYTE8/$\overline{10}$ is LOW)					
0	00	011000 100011	LM (10-bit SYNC)	0	00
1	01	111111 111111	I'I'	1	01
2	10	011101 011101	T'T'	2	10
3	11	011101 111001	T'S'	3	11

Notes:

40. Binary CMD is the parallel input data which is input to the Transmitter and output from the Receiver. Binary bits are listed from left to right in the following order:
    8-Bit mode (BYTE8/$\overline{10}$ is HIGH and TXSC/$\overline{D}$ or RXSC/$\overline{D}$ is HIGH)—TXCMD/RXCMD[3], [2], [1], [0].
    10-Bit mode (BYTE8/10 is LOW and TXSC/$\overline{D}$ or RXSC/$\overline{D}$ is HIGH)—TXCMD/RXCMD[1], [0].
41. While these Commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

Functional Description

Transmit FIFO Reset Sequence

On power-up, the Transmitter and Receiver FIFOs may contain random data. The Transmitter FIFO will empty automatically as the Transmitter sends the random data (assuming that $\overline{TXHALT}$ is not LOW) within the first 256 character-times after power is applied. The Receiver FIFO will retain any random data stored in it at power-up, and will accumulate all the random data being received from any attached transmitter as it is powered up. This random received data can be "flushed" by reading it, or the Receive FIFO can be "reset" to remove the unwanted data.

The Transmit FIFO reset sequence (see *Figure 2*) is started when $\overline{TXRST}$ and $\overline{CE}$ are first sampled LOW by the rising edge of TXCLK. Because a Tx_RstMatch condition is present, the Transmit FIFO flags are asserted and can be used to track the status of any Transmit FIFO reset in progress. Once the reset sequence has reached its maximum count (seven TXCLK cycles), the Transmit FIFO flags are asserted to indicate a FULL condition ($\overline{TXEMPTY}$ is deasserted, and both $\overline{TXHALF}$ and $\overline{TXFULL}$ are asserted). This indicates that the Transmit FIFO reset has been recognized by the Transmit Control State Machine and that a reset has been started. However, if the $\overline{TXEN}$ is asserted prior to or during the assertion and sampling of $\overline{TXRST}$, the reset sequence is inhibited until $\overline{TXEN}$ is removed.

NOTE: The FIFO FULL state forced by the reset operation is different from a FULL state caused by normal FIFO data writes. For normal FIFO write operations, when FULL is first asserted, the Transmit FIFO must still accept up to four additional writes of data. When a FULL state is asserted due to a Transmit FIFO reset operation, the FIFO will not accept any additional data.

The Transmit FIFO reset does not complete until the external reset condition is removed. This can be removed by deassertion of either $\overline{TXRST}$ or $\overline{CE}$. If $\overline{CE}$ is deasserted (HIGH) to

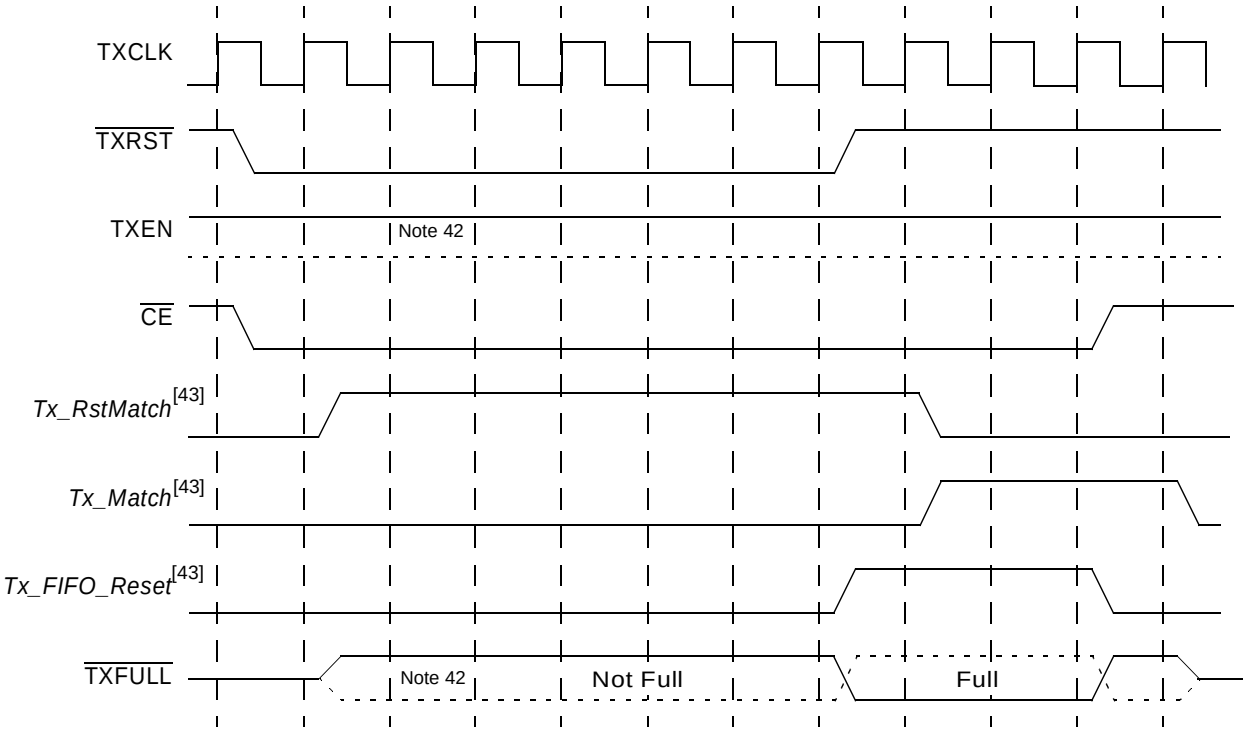


Figure 2. Transmit FIFO Reset Sequence

remove the reset condition, the Transmit FIFO flag's drivers are disabled, and the Transmit FIFO must be addressed at a later time to validate completion of the Transmit FIFO reset. If TXRST is deasserted (HIGH) to remove the reset condition, the Tx_RstMatch is changed to a Tx_Match, and the Transmit FIFO status flags remain driven. The Transmit FIFO reset operation is complete when the Transmit FIFO flags indicate an EMPTY state (TXEMPTY is asserted and both TXHALF and TXFULL are deasserted). A valid Transmit FIFO reset sequence is shown in *Figure 2*.

Here the TXRST and CE are asserted (LOW) at the same time. When these signals are both sampled LOW by TXCLK, a Tx_RstMatch condition is present. With TXEN deasserted (HIGH), the Transmit FIFO is not selected for data transfers. This Tx_RstMatch condition must remain for seven TXCLK cycles to initiate the Tx_FIFO_Reset. Following this the TXFULL FIFO status flag is asserted to indicate that the Transmit FIFO reset sequence has completed and that a Transmit FIFO reset is in progress.

When the TXRST signal is deasserted (HIGH), CE remains LOW to allow the FIFO status flags to be driven. This allows the completion of the reset operation to be monitored. To allow better multi-tasking on multi-PHY implementations, it is possible to deassert CE (HIGH) as soon as the FULL state is indicated. The FIFO reset operation will complete and the EMPTY state (indicating completion of the reset operation) can be detected during a separate polling operation.

For those links implemented with a single PHY, it is possible to hardwire CE LOW and still perform normal accesses and reset operations. This is shown in *Figure 3*. In a single-PHY implementation, a Transmit FIFO reset can never be initiated with TXEN asserted at the same time as TXRST. Since CE is always LOW, any assertion of TXEN causes the Transmit FIFO to be selected, clearing the reset counter.

Figure 4 shows a sequence of input signals which will not produce a FIFO reset. In this case TXEN was asserted to select a Transmit FIFO for data transfers. Because TXEN remains active, the assertion of CE and TXRST does not initiate a reset operation. This is shown by the TXFULL flag remaining HIGH (deasserted) following what would be the normal expiration of the seven-state reset counter.

Receive FIFO Reset Sequence

The Receive FIFO reset sequence operates (for the most part) the same as the Transmit FIFO reset sequence. The same requirements exist for the assertion state of RXRST and selection of the interface. A sample Receive FIFO reset sequence is shown in *Figure 5*. Upon recognition of a Receive FIFO reset, the Receive FIFO flags are forced to indicate an EMPTY state to prohibit additional reads from the FIFO. Unlike the Transmit FIFO, where the internal completion of the reset operation is shown by first going FULL and later going EMPTY when the internal reset is complete, there is no secondary indication of the completion of the internal reset of the Receive FIFO. The Receive FIFO is usable as soon as new data is placed into it by the Receive Control State Machine.

Notes:

42. Signals shown as dotted lines indicate timing and levels when configured for external FIFOs (EXTFIFO is HIGH).
43. Signal names listed in italics are internal signals, shown for reference only.

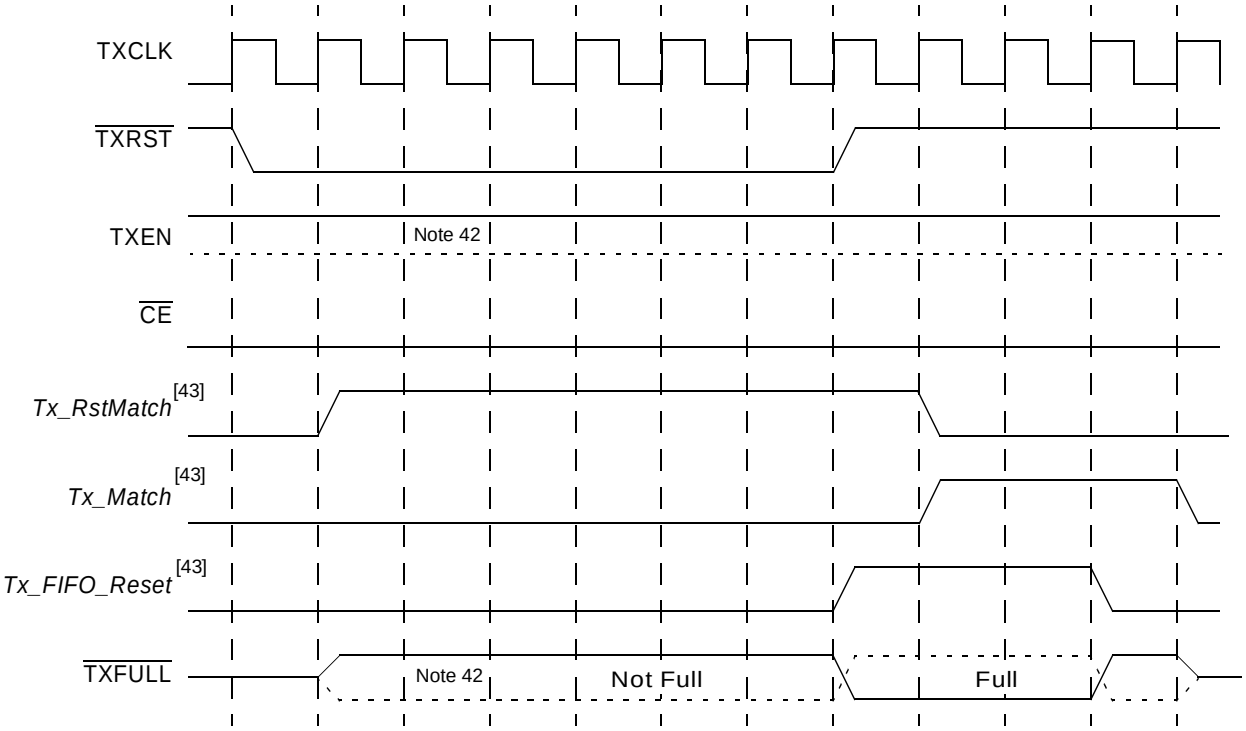


Figure 3. Transmit FIFO Reset Sequence with Constant $\overline{CE}$

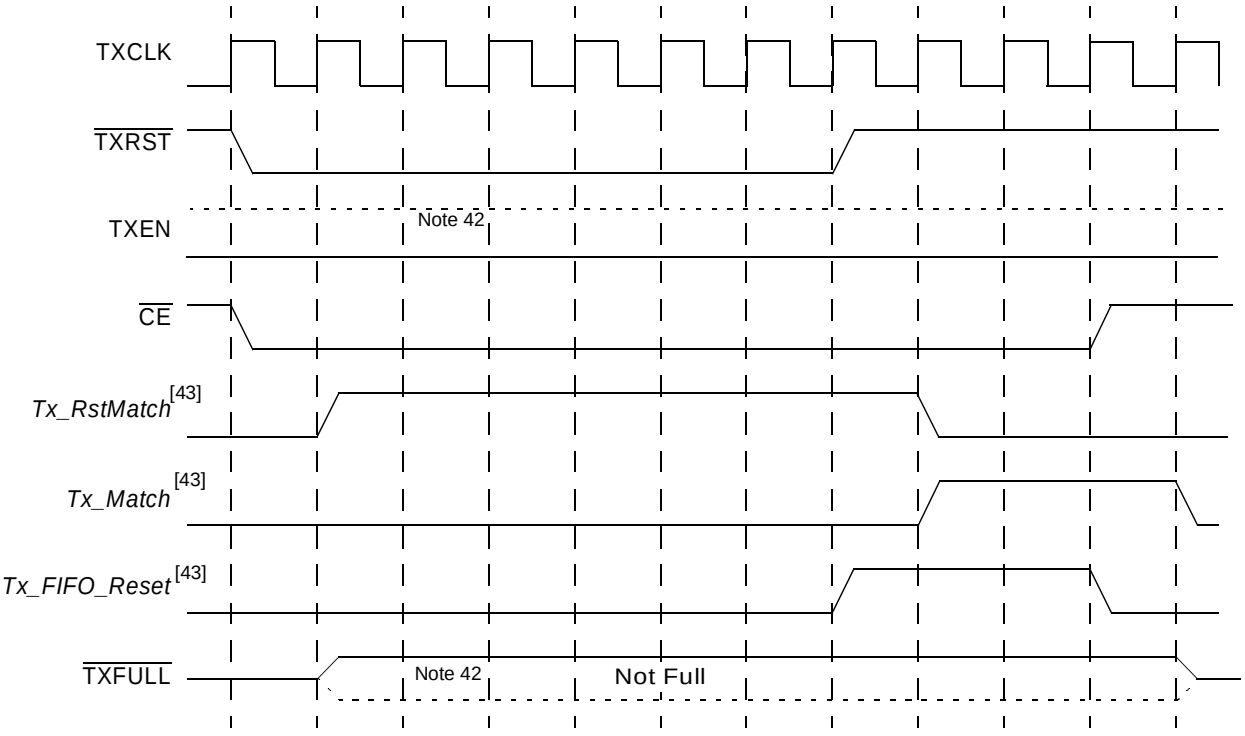


Figure 4. Invalid Transmit FIFO Reset Sequence with $\overline{TXEN}$ Asserted

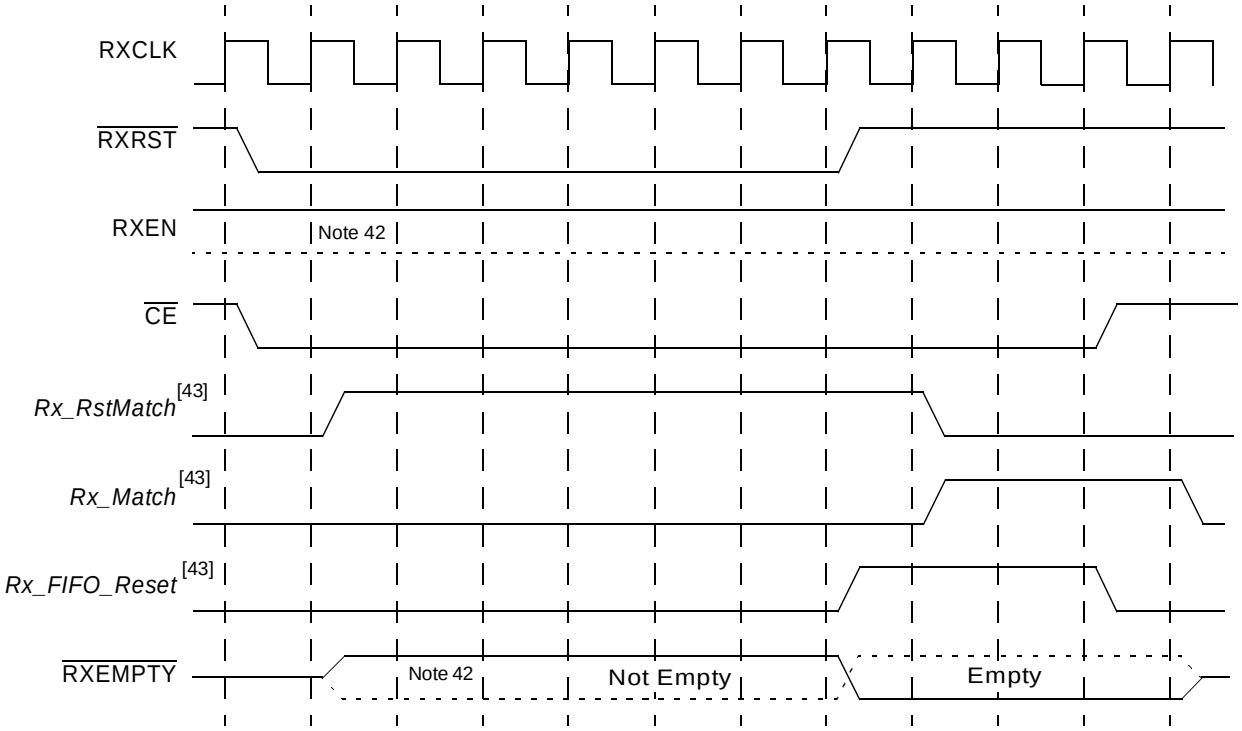
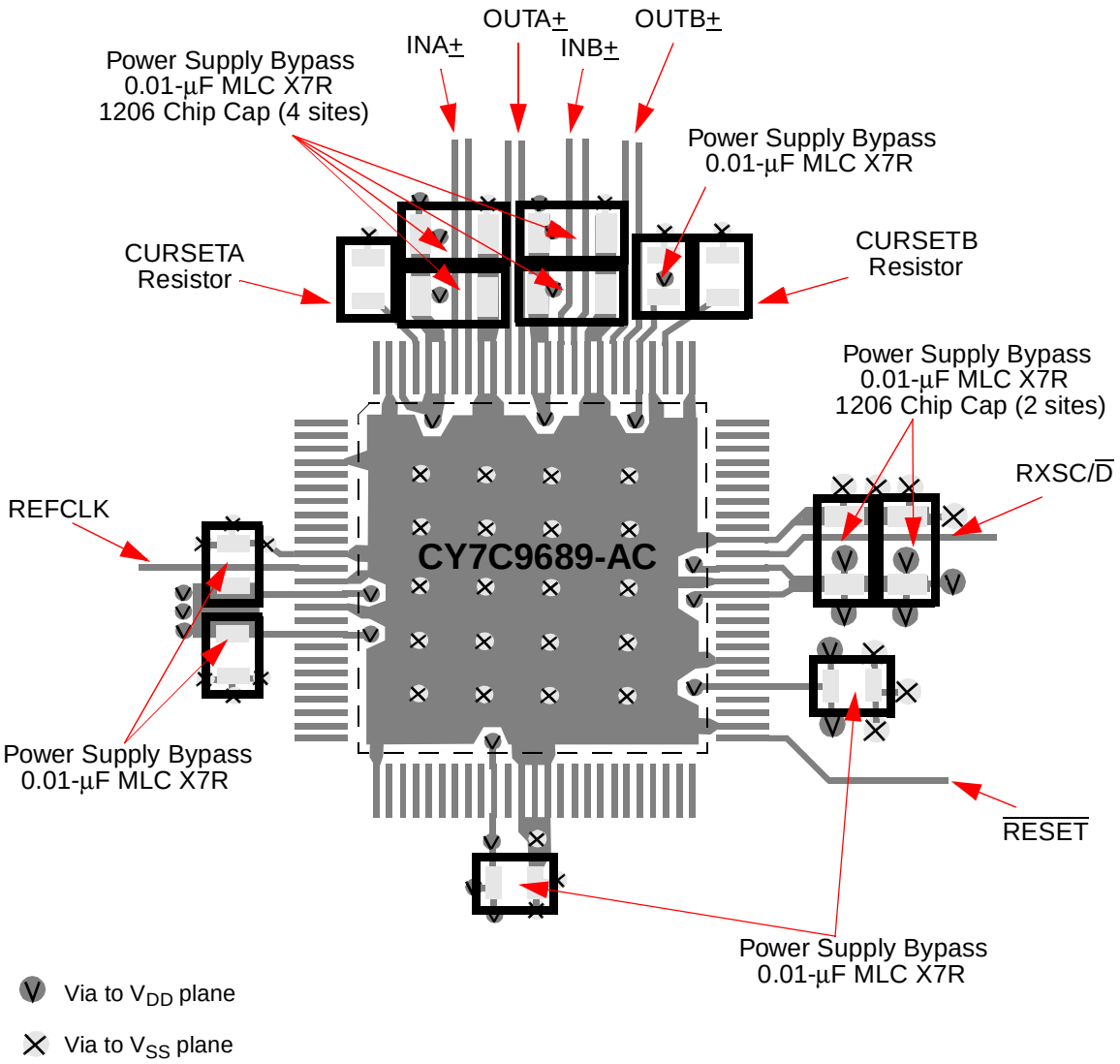


Figure 5. Receive FIFO Reset Sequence

Printed Circuit Board Layout Suggestions



This is a typical printed circuit board layout showing example placement of power supply bypass components and other components mounted on the same side as the CY7C9689.

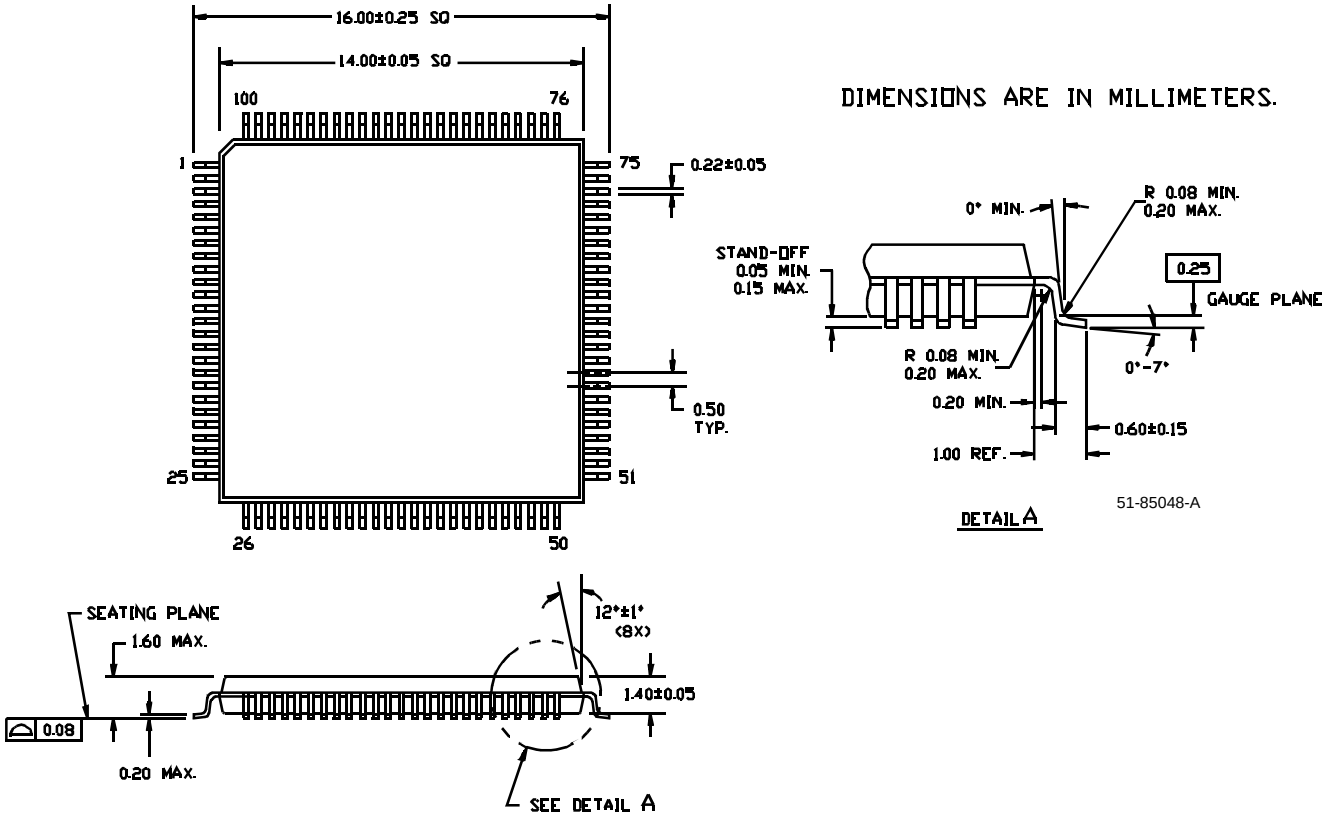
Other layouts, including cases with components mounted on the reverse side would work as well.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7C9689-AC	A100	100-Lead Thin Quad Flat Pack	Commercial
CY7C9689-AI	A100	100-Lead Thin Quad Flat Pack	Industrial

Package Diagram

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



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