Description

μPD71082 and μPD71083 are CMOS 8-bit transparent latches with three-state output buffers. They are used as bus buffers or bus multiplexers in microprocessor systems. Their high-drive capability makes them suitable for data latch, buffer, or I/O port applications.

Features

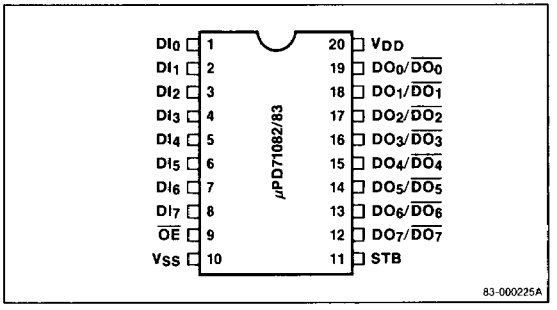
- CMOS technology
- 8-bit parallel data register
- Three-state output buffer
- High drive capability output buffer (I_{OL} = 12 mA)
- μPD8085A, 8048, 8086, 8088, μPD70108/116, and μPD70208/216 system compatible
- μPD71082 — non-inverted output; μPD71083 — inverted output
- Single +5 V ±10% power supply
- Transparent operation
- Industrial temperature range: −40 to +85°C

Ordering Information

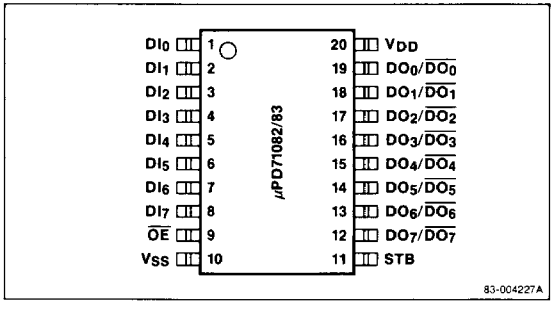
Part Number	Package	Output
μPD71082C	20-pin plastic DIP	Non-inverted
μPD71082G	20-pin plastic SOP	
μPD71083C	20-pin plastic DIP	Inverted
μPD71083G	20-pin plastic SOP	

Pin Configurations

20-Pin Plastic DIP



20-Pin Plastic SOP



Pin Identification

Symbol	Function
DI_0-DI_7	Data input, bits 0-7
DO_0-DO_7/ $\overline{DO_0}$-$\overline{DO_7}$	Data output, bits 0-7; non-inverted (μPD71082) or inverted (μPD71083)
STB	Strobe input
$\overline{OE}$	Output enable input
V_{DD}	+5 V power supply
V_{SS}	Ground

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PIN FUNCTIONS

DI_0-DI_7 (Data Input)

DI_0-DI_7 are data input lines to the 8-bit data latch. Data on DI lines passes through the latch while STB is high. The data is latched to DO/$\overline{DO}$ with the falling edge of STB.

DO_0-DO_7/$\overline{DO}_0$-$\overline{DO}_7$ (Data Output)

DO_0-DO_7/$\overline{DO}_0$-$\overline{DO}_7$ are the three-state data output lines from the 8-bit data latch. When $\overline{OE}$ is high, these lines go into the high-impedance state. When $\overline{OE}$ is low, data from the latch is output, either non-inverted (μPD71082) or inverted (μPD71083).

STB (Strobe)

STB is the input strobe signal for the 8-bit latch. When STB is high, data on the DI lines passes through the 8-bit latch. Data is latched on the falling edge of STB. When STB is low, the DO_0-DO_7/$\overline{DO}_0$-$\overline{DO}_7$ outputs do not change.

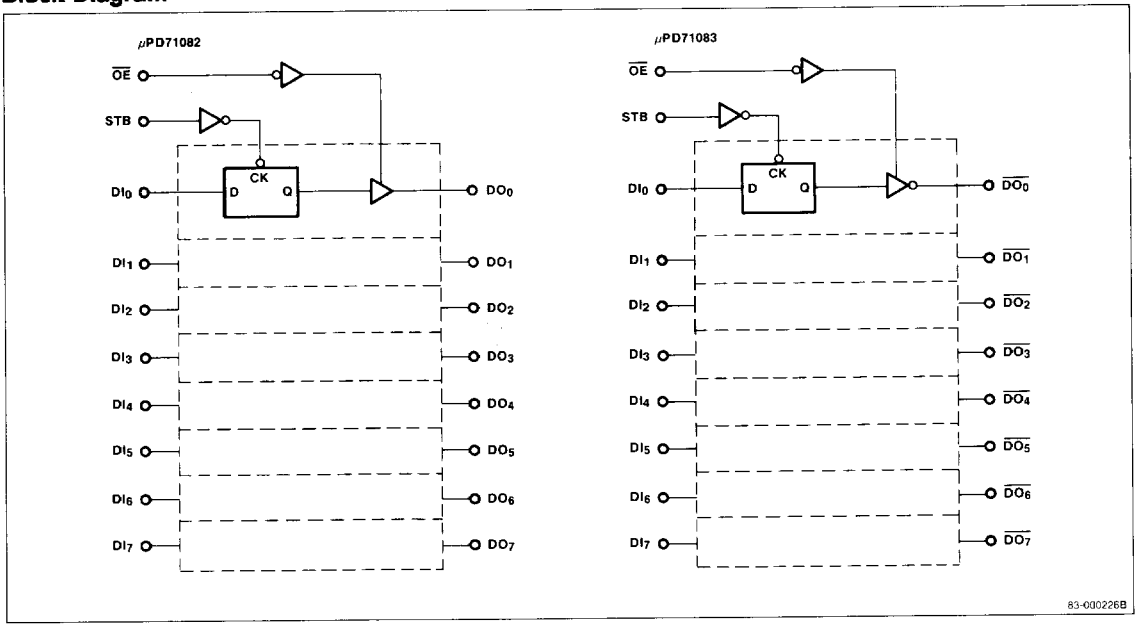
$\overline{OE}$ (Output Enable)

$\overline{OE}$ input is the output enable signal for the three-state DO/$\overline{DO}$ lines. When $\overline{OE}$ is high, DO/$\overline{DO}$ lines are high impedance. When $\overline{OE}$ is low, data from the 8-bit latch is output to DO_0-DO_7/$\overline{DO}_0$-$\overline{DO}_7$. See table 1.

Table 1. Latch Operation

STB	$\overline{OE}$	DO_0-DO_7/$\overline{DO}_0$-$\overline{DO}_7$	8-Bit Data Latch
Low	Low	Latched data from 8-bit data latch is enabled	DI line data has been latched with falling edge of STB (high to low)
	High	High impedance	
High	Low	Data on DI_0-DI_7	DI passed through to DO/$\overline{DO}$
	High	High impedance	

Block Diagram



FUNCTIONAL DESCRIPTION

The μPD71082 and μPD71083 are 8-bit data latches strobed by the STB signal. They have high-drive capability output buffers controlled by the $\overline{OE}$ signal. Data on the DI lines is latched by the trailing edge of STB (high to low). When STB is high, data passes through the latch. When $\overline{OE}$ is high, DO lines are high impedance. When $\overline{OE}$ is low, the contents of the latches are output on DO_0-DO_7. The DO lines are isolated from $\overline{OE}$ switching noise.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C; V_{SS} = 0 V

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−1.0 to V_{DD} + 1 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Power dissipation, P_{DMAX}, DIP	500 mW
Power dissipation, P_{DMAX}, SO	200 mW
Operating temperature, T_{opt}	−40 to +85°C
Storage temperature, T_{stg}	−65 to +150°C

Exposing the device to stresses above those listed in the absolute maximum ratings could cause permanent damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Symbol	Min	Max	Units	Conditions
Input voltage, high	V_{IH}	2.2		V	V_{OL} = 0.45 V V_{OH} = V_{DD} − 0.8 V
Input voltage, low	V_{IL}		0.8	V	V_{OL} = 0.45 V V_{OH} = V_{DD} − 0.8 V
Output voltage, high	V_{OH}	V_{DD} − 0.8		V	I_{OH} = −4 mA
Output voltage, low	V_{OL}		0.45	V	I_{OL} = 12 mA
Input current	I_I	−1.0	1.0	μA	V_I = V_{DD}, V_{SS}
Leakage current, high impedance	I_{OFF}	−10	10	μA	$\overline{OE}$ = V_{DD}
Power supply current (static)	I_{DD}		80	μA	V_I = V_{DD}, V_{SS}
Power supply current (dynamic)	I_{DDdyn}		20	mA	f_{in} = 10 MHz C = 200 pF

Capacitance

T_A = 25°C; V_{DD} = +5 V

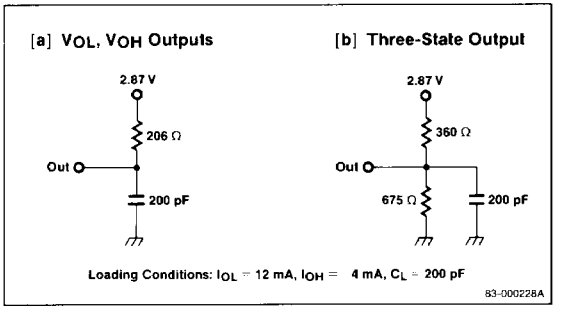
Parameter	Symbol	Min	Max	Units	Conditions
Input capacitance	C_{in}		12	pF	f = 1 MHz

AC Characteristics

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Symbol	Min	Max	Units	Conditions
Input to output delay	t_{DIO}	5	40	ns	Loading circuit (a)
STB to output delay	t_{DSTBO}	10	60	ns	
Data float time from $\overline{OE}$ high	t_{FCTO}	5	30	ns	Loading circuit (b)
Data output delay from $\overline{OE}$ low	t_{DCTO}	10	40	ns	
Input to STB setup time	t_{SISTB}	0		ns	Loading circuit (a)
Input to STB hold time	t_{HSTBI}	25		ns	
STB high pulse width	t_{PWSTB}	20		ns	
Signal rise time	t_{LH}		20	ns	0.8 to 2.0 V
Signal fall time	t_{HL}		12	ns	2.0 to 0.8 V

Loading Circuits for AC Testing



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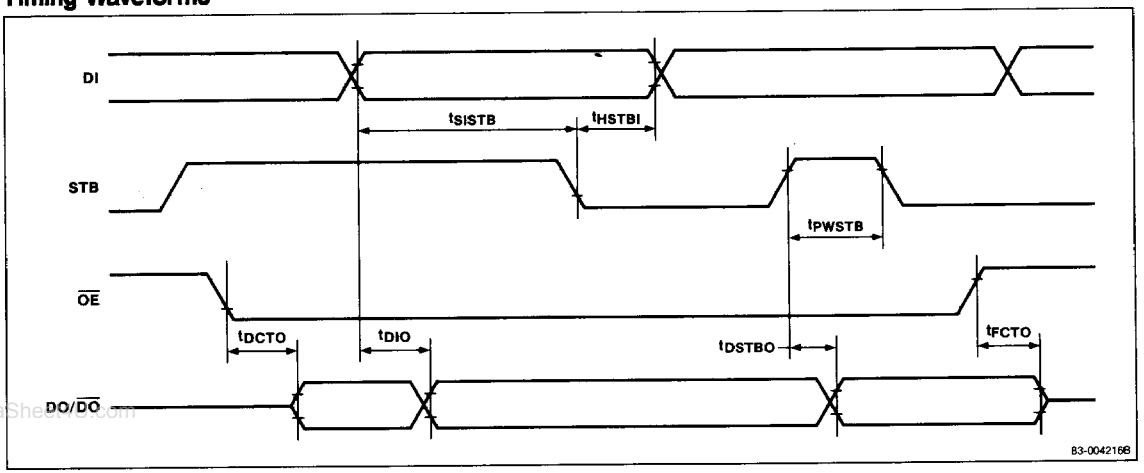
Timing Waveforms



Timing Measurement Points