

HYB18T1G400AF
HYB18T1G800AF
HYB18T1G160AF

1-Gbit Double-Data-Rate-Two SDRAM

DDR2 SDRAM

RoHS Compliant Products

Memory Products



N e v e r s t o p t h i n k i n g .

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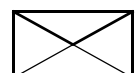


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1 Overview

This chapter gives an overview of the 1-Gbit Double-Data-Rate-Two SDRAM product family and describes its main characteristics.

1.1 Features

The 1-Gbit Double-Data-Rate-Two SDRAM offers the following key features:

- 1.8 V \pm 0.1 V Power Supply
- 1.8 V \pm 0.1 V (SSTL_18) compatible I/O
- DRAM organisations with 4, 8 and 16 data in/outputs
- Double Data Rate architecture: two data transfers per clock cycle, eight internal banks for concurrent operation
- CAS Latency: 3, 4 and 5
- Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- $\overline{\text{DQS}}$ can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality.
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Average Refresh Period 7.8 μs at a T_{CASE} lower than 85 °C, 3.9 μs between 85 °C and 95 °C
- Strong and Weak Strength Data-Output Drivers
- 1K page size for $\times 4$ & $\times 8$, 2K page size for $\times 16$
- Packages:
P-TFBGA-68 for $\times 4$ & $\times 8$ components
P-TFBGA-92 for $\times 16$ components
- RoHS Compliant Products¹⁾

Table 1 High Performance

| Product Type Speed Code | | | -3.7 | -5 | Unit |
|-------------------------|------|------------------|----------------|----------------|------|
| Speed Grade | | | DDR2-533 4-4-4 | DDR2-400 3-3-3 | — |
| max. Clock Frequency | @CL5 | f_{CK5} | 266 | 200 | MHz |
| | @CL4 | f_{CK4} | 266 | 200 | MHz |
| | @CL3 | f_{CK3} | 200 | 200 | MHz |
| min. RAS-CAS-Delay | | t_{RCD} | 15 | 15 | ns |
| min. Row Precharge Time | | t_{RP} | 15 | 15 | ns |
| min. Row Active Time | | t_{RAS} | 45 | 40 | ns |
| min. Row Cycle Time | | t_{RC} | 60 | 55 | ns |

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The 1-Gb DDR2 DRAM is a high-speed Double-Data-Rate-2 CMOS Synchronous DRAM device containing 1,073,741,824 bits and internally configured as an octal-bank DRAM. The 1-Gb device is organized as either 32 Mbit × 4 I/O × 8 banks, 16 Mbit × 8 I/O × 8 banks or 8 Mbit × 16 I/O × 8 banks chip. These synchronous devices achieve high speed transfer rates starting at 400 Mb/sec/pin for general applications. See **Table 1** for performance figures.

The device is designed to comply with all DDR2 DRAM key features:

1. posted CAS with additive latency,
2. write latency = read latency - 1,
3. normal and weak strength data-output driver,
4. Off-Chip Driver (OCD) impedance adjustment
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks.

Inputs are latched at the cross point of differential clocks (CK rising and \overline{CK} falling). All I/Os are synchronized with a single ended DQS or differential DQS- \overline{DQS} pair in a source synchronous fashion.

A 17 bit address bus for ×4 and ×8 organised components and a 16 bit address bus for ×16 components is used to convey row, column and bank address information in a RAS-CAS multiplexing style.

The DDR2 device operates with a 1.8 V ± 0.1 V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in P-TFBGA package.

1.3 Ordering Information

Table 2 Ordering information for RoHS Compliant Products



| Part Number | Org. | Speed | CAS ¹⁾ -RCD ²⁾ -RP ³⁾ Latencies | Clock (MHz) | CAS ¹⁾ -RCD ²⁾ -RP ³⁾ Latencies | Clock (MHz) | Package |
|-------------------|------|----------|---|----------------|---|----------------|------------|
| HYB18T1G400AF-5 | x4 | DDR2-400 | 3-3-3 | 200 | — | — | P-TFBGA-68 |
| HYB18T1G800AF-5 | x8 | | | | | | P-TFBGA-92 |
| HYB18T1G160AF-5 | x16 | | | | | | P-TFBGA-92 |
| HYB18T1G400AF-3.7 | x4 | DDR2-533 | 4-4-4 | 266 | 3-3-3 | 200 | P-TFBGA-68 |
| HYB18T1G800AF-3.7 | x8 | | | | | | P-TFBGA-92 |
| HYB18T1G160AF-3.7 | x16 | | | | | | P-TFBGA-92 |

1) CAS: Column Address Strobe

2) RCD: Row Column Delay

3) RP: Row Precharge

Note: For product nomenclature see **Chapter 10** of this data sheet

1.4 Pin Configuration

The pin configuration of a DDR2 SDRAM is listed by function in [Table 3](#). The abbreviations used in the Pin#/Buffer Type columns are explained in [Table 4](#) and [Table 5](#) respectively. The pin numbering for the FBGA package is depicted in [Figure 1](#) for ×4, [Figure 2](#) for ×8 and [Figure 3](#) for ×16.

Table 3 Pin Configuration of DDR SDRAM

| Ball#/Pin# | Name | Pin Type | Buffer Type | Function |
|--|-------------------------|----------|-------------|-----------------------------------|
| Clock Signals ×4/×8 organizations | | | | |
| J8 | CK | I | SSTL | Clock Signal |
| K8 | $\overline{\text{CK}}$ | I | SSTL | Complementary Clock Signal |
| K2 | CKE | I | SSTL | Clock Enable |
| Clock Signals ×16 organization | | | | |
| M8 | CK | I | SSTL | Clock Signal |
| N8 | $\overline{\text{CK}}$ | I | SSTL | Complementary Clock Signal |
| N2 | CKE | I | SSTL | Clock Enable |
| Control Signals ×4/×8 organizations | | | | |
| K7 | $\overline{\text{RAS}}$ | I | SSTL | Row Address Strobe |
| L7 | $\overline{\text{CAS}}$ | I | SSTL | Column Address Strobe |
| K3 | $\overline{\text{WE}}$ | I | SSTL | Write Enable |
| L8 | $\overline{\text{CS}}$ | I | SSTL | Chip Select |
| Control Signals ×16 organization | | | | |
| N7 | $\overline{\text{RAS}}$ | I | SSTL | Row Address Strobe |
| P7 | $\overline{\text{CAS}}$ | I | SSTL | Column Address Strobe |
| N3 | $\overline{\text{WE}}$ | I | SSTL | Write Enable |
| P8 | $\overline{\text{CS}}$ | I | SSTL | Chip Select |
| Address Signals ×4/×8 organizations | | | | |
| L2 | BA0 | I | SSTL | Bank Address Bus 2:0 |
| L3 | BA1 | I | SSTL | |
| L1 | BA2 | I | SSTL | |
| M8 | A0 | I | SSTL | Address Signal 12:0 |
| M3 | A1 | I | SSTL | |
| M7 | A2 | I | SSTL | |
| N2 | A3 | I | SSTL | |
| N8 | A4 | I | SSTL | |
| N3 | A5 | I | SSTL | |
| N7 | A6 | I | SSTL | |
| P2 | A7 | I | SSTL | |
| P8 | A8 | I | SSTL | |
| P3 | A9 | I | SSTL | |
| M2 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| P7 | A11 | I | SSTL | |
| R2 | A12 | I | SSTL | |

Table 3 Pin Configuration of DDR SDRAM

| Ball#/Pin# | Name | Pin Type | Buffer Type | Function |
|---|------|----------|-------------|----------------------|
| R8 | A13 | I | SSTL | Address Signal 13 |
| Address Signals ×16 organization | | | | |
| P2 | BA0 | I | SSTL | Bank Address Bus 2:0 |
| P3 | BA1 | I | SSTL | |
| P1 | BA2 | I | SSTL | |
| R8 | A0 | I | SSTL | Address Signal 12:0 |
| R3 | A1 | I | SSTL | |
| R7 | A2 | I | SSTL | |
| T2 | A3 | I | SSTL | |
| T8 | A4 | I | SSTL | |
| T3 | A5 | I | SSTL | |
| T7 | A6 | I | SSTL | |
| U2 | A7 | I | SSTL | |
| U8 | A8 | I | SSTL | |
| U3 | A9 | I | SSTL | |
| R2 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| U7 | A11 | I | SSTL | |
| V2 | A12 | I | SSTL | |
| Data Signals ×4/×8 organizations | | | | |
| G8 | DQ0 | I/O | SSTL | Data Signal 0 |
| G2 | DQ1 | I/O | SSTL | Data Signal 1 |
| H7 | DQ2 | I/O | SSTL | Data Signal 2 |
| H3 | DQ3 | I/O | SSTL | Data Signal 3 |
| Data Signals ×8 organization | | | | |
| H1 | DQ4 | I/O | SSTL | Data Signal 4 |
| H9 | DQ5 | I/O | SSTL | Data Signal 5 |
| F1 | DQ6 | I/O | SSTL | Data Signal 6 |
| F9 | DQ7 | I/O | SSTL | Data Signal 7 |
| Data Signals ×16 organization | | | | |
| K8 | DQ0 | I/O | SSTL | Data Signal 0 |
| K2 | DQ1 | I/O | SSTL | Data Signal 1 |
| L7 | DQ2 | I/O | SSTL | Data Signal 2 |
| L3 | DQ3 | I/O | SSTL | Data Signal 3 |
| L1 | DQ4 | I/O | SSTL | Data Signal 4 |
| L9 | DQ5 | I/O | SSTL | Data Signal 5 |
| J1 | DQ6 | I/O | SSTL | Data Signal 6 |
| J9 | DQ7 | I/O | SSTL | Data Signal 7 |
| F8 | DQ8 | I/O | SSTL | Data Signal 8 |
| F2 | DQ9 | I/O | SSTL | Data Signal 9 |

Table 3 Pin Configuration of DDR SDRAM

| Ball#/Pin# | Name | Pin Type | Buffer Type | Function |
|---|--------------------------|----------|-------------|-------------------------|
| G7 | DQ10 | I/O | SSTL | Data Signal 10 |
| G3 | DQ11 | I/O | SSTL | Data Signal 11 |
| G1 | DQ12 | I/O | SSTL | Data Signal 12 |
| G9 | DQ13 | I/O | SSTL | Data Signal 13 |
| E1 | DQ14 | I/O | SSTL | Data Signal 14 |
| E9 | DQ15 | I/O | SSTL | Data Signal 15 |
| Data Strobe ×4/×8 organisations | | | | |
| F7 | DQS | I/O | SSTL | Data Strobe |
| E8 | $\overline{\text{DQS}}$ | I/O | SSTL | Data Strobe |
| Data Strobe ×8 organisations | | | | |
| F3 | RDQS | I/O | SSTL | Read Data Strobe |
| E2 | $\overline{\text{RDQS}}$ | I/O | SSTL | Read Data Strobe |
| Data Strobe ×16 organization | | | | |
| E7 | UDQS | I/O | SSTL | Data Strobe Upper Byte |
| D8 | $\overline{\text{UDQS}}$ | I/O | SSTL | Data Strobe Upper Byte |
| J7 | LDQS | I/O | SSTL | Data Strobe Lower Byte |
| H8 | $\overline{\text{LDQS}}$ | I/O | SSTL | Data Strobe Lower Byte |
| Data Mask ×4/×8 organizations | | | | |
| E3 | DM | I | SSTL | Data Mask |
| Data Mask ×16 organization | | | | |
| F3 | UDM | I | SSTL | Data Mask Upper Byte |
| J3 | LDM | I | SSTL | Data Mask Lower Byte |
| Power Supplies ×4/×8 organizations | | | | |
| E9,G1,G3,G7,G9 | V_{DDQ} | PWR | — | I/O Driver Power Supply |
| E1,J9,M9,R1 | V_{DD} | PWR | — | Power Supply |
| E7,F2,F8,H2,H8 | V_{SSQ} | PWR | — | Power Supply |
| E3,J3;N1,P9 | V_{SS} | PWR | — | Power Supply |
| J2 | V_{REF} | AI | — | I/O Reference Voltage |
| J1 | V_{DDL} | PWR | — | Power Supply |
| J7 | V_{SSDL} | PWR | — | Power Supply |
| Power Supplies ×16 organization | | | | |
| J2 | V_{REF} | AI | — | I/O Reference Voltage |
| E9, G1, G3, G7, G9 | V_{DDQ} | PWR | — | I/O Driver Power Supply |
| M1 | V_{DDL} | PWR | — | Power Supply |
| D1,H1,M9,R9,V1 | V_{DD} | PWR | — | Power Supply |

Table 3 Pin Configuration of DDR SDRAM

| Ball#/Pin# | Name | Pin Type | Buffer Type | Function |
|--|-------------------|----------|-------------|----------------------------|
| D7,E2,G2,E8, G8,H7,J2,J8,L 2,L8 | V _{SSQ} | PWR | — | Power Supply |
| M7 | V _{SSDL} | PWR | — | Power Supply |
| D3,H3,M3,T1, U9 | V _{SS} | PWR | — | Power Supply |
| Not Connected ×4 organization | | | | |
| A1,A2,A8,A9, E2,F9,H1,F1, R7,H9,W1,W2 ,W8,W9,R3 | NC | NC | — | Not Connected |
| Not Connected ×8 organization | | | | |
| A1,A2,A8,A9, R7,W2,W3,W 8,W9,R3 | NC | NC | — | Not Connected |
| Not Connected ×16 organization | | | | |
| A1,A2,A8,A9, D2,H2,V3,V7, V8,AA1,AA2,A A8,AA9 | NC | NC | — | Not Connected |
| Other Pins ×4/×8 organizations | | | | |
| K9 | ODT | I | SSTL | On-Die Termination Control |
| Other Pins ×16 organization | | | | |
| N9 | ODT | I | SSTL | On-Die Termination Control |

Table 4 Abbreviations for Pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

Table 5 Abbreviations for Buffer Type

| Abbreviation | Description |
|--------------|---|
| SSTL | Serial Stub Terminated Logic (SSTL_18) |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

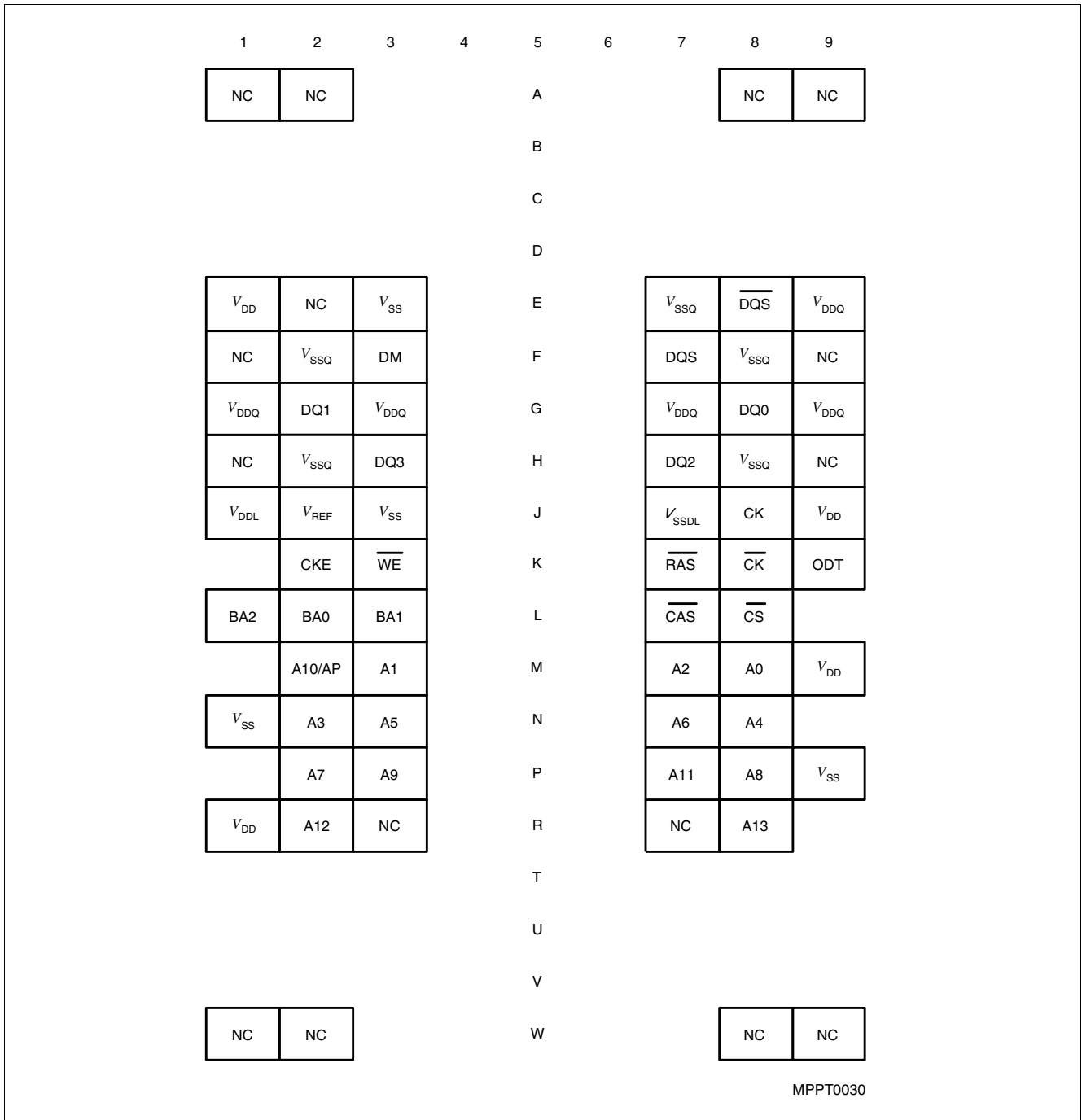


Figure 1 Pin Configuration P-TFBGA-68 (x4) Top View, see the balls through the package

Note: V_{DDL} and V_{SSDL} are power and ground for the DLL. They are connected on the device to V_{DD} and V_{SS}

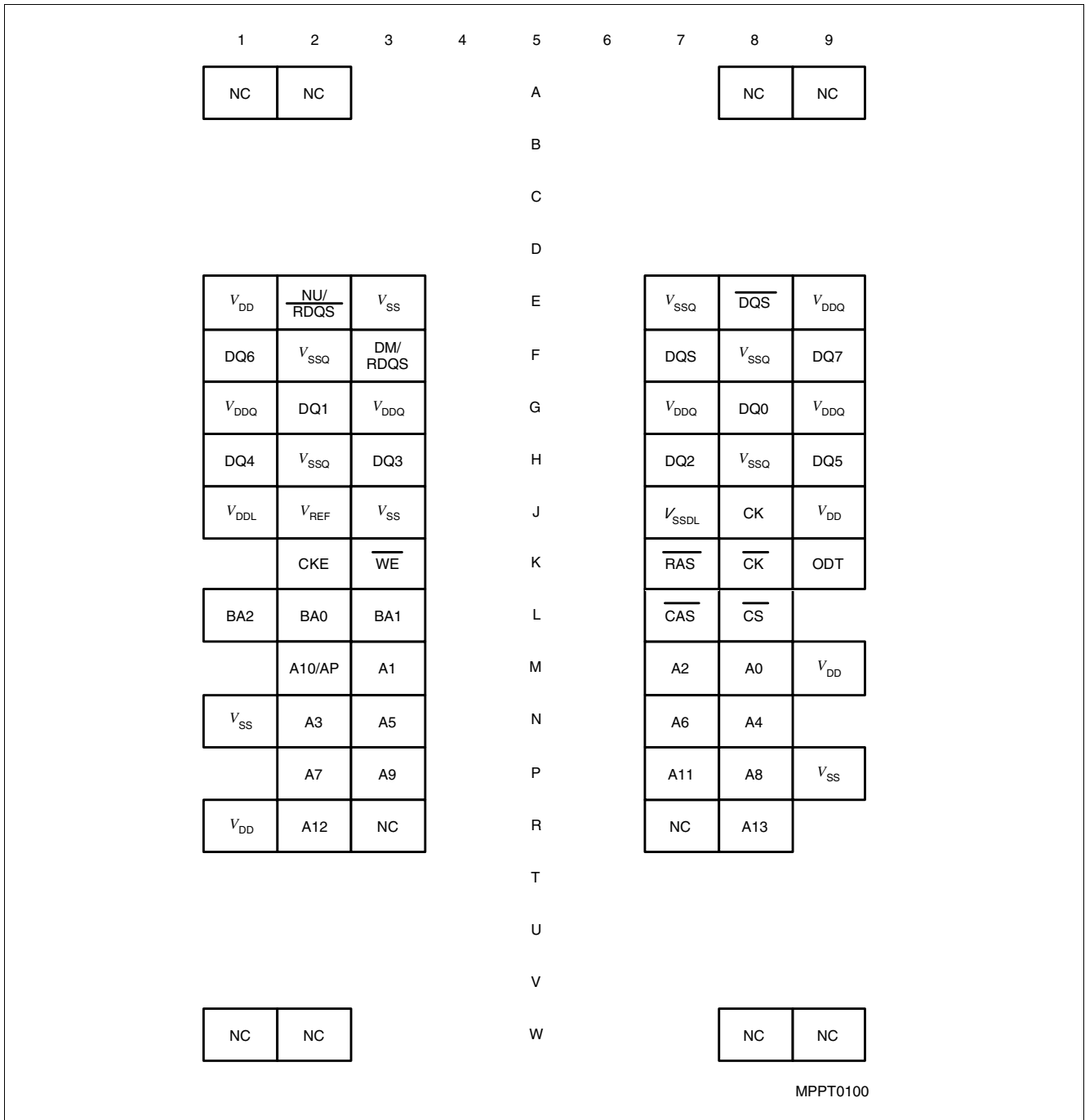
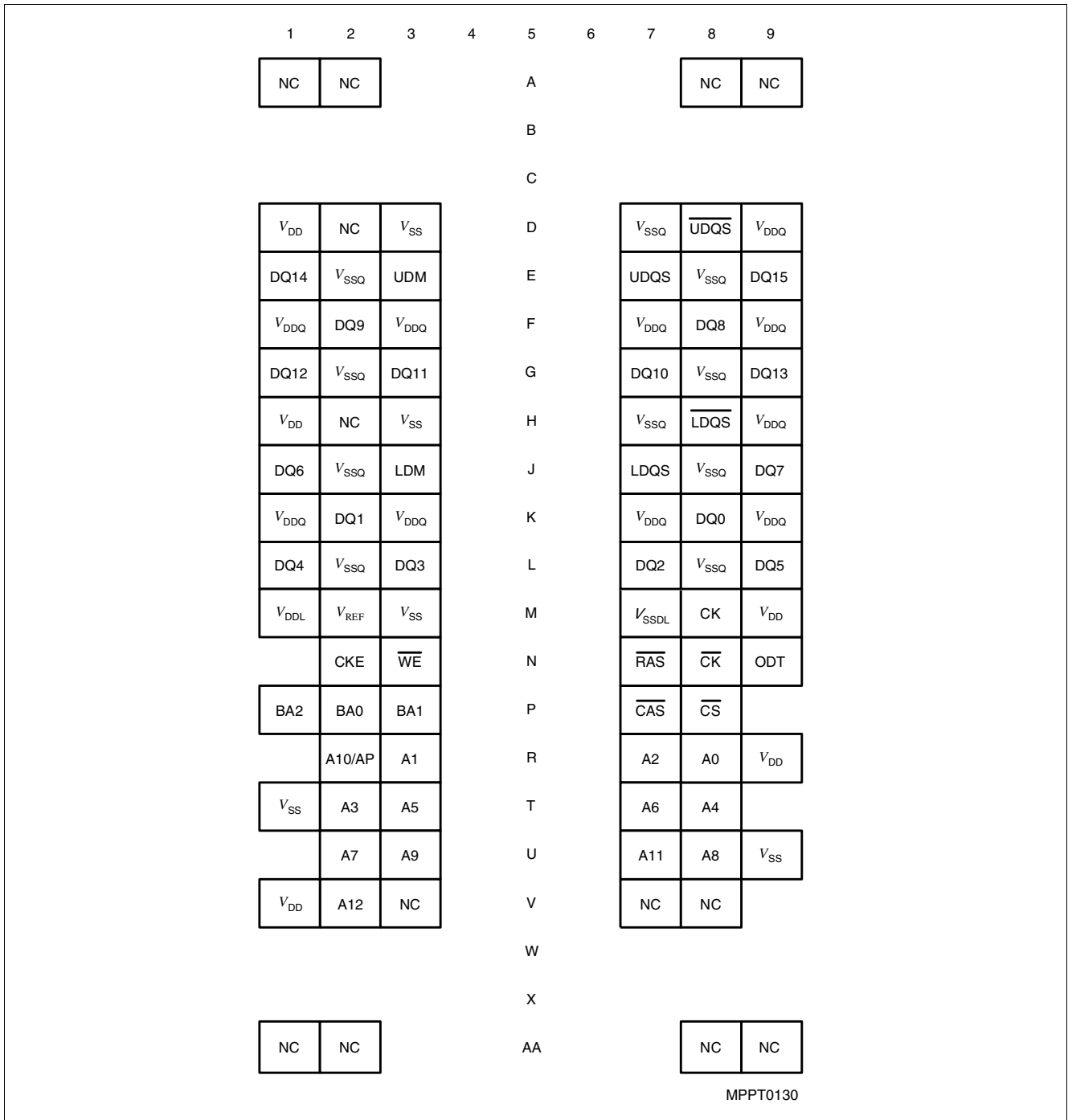


Figure 2 Pin Configuration P-TFBGA-68 (x8) Top View, see the balls through the package

Note

1. \overline{RDQS} / \overline{RDQS} are enabled by EMRS(1) command.
2. If \overline{RDQS} / \overline{RDQS} is enabled, the DM function is disabled
3. When enabled, \overline{RDQS} & \overline{RDQS} are used as strobe signals during reads.
4. V_{DDL} and V_{SSDL} are power and ground for the DLL. They are connected on the device to V_{DD} and V_{SS}



1.5 1Gbit DDR2 Addressing

Table 6 1 Gbit DDR2 Addressing

| Configuration | 256 Mb x 4 | 128 Mb x 8 | 64 Mb x 16 | Note |
|-------------------------------|-------------|------------|------------|------|
| Number of Banks | 8 | 8 | 8 | |
| Bank Address | BA[2:0] | BA[2:0] | BA[2:0] | |
| Auto-Precharge | A10 / AP | A10 / AP | A10 / AP | |
| Row Address | A[13:0] | A[13:0] | A[12:0] | |
| Column Address | A11, A[9:0] | A[9:0] | A[9:0] | |
| Number of Column Address Bits | 11 | 10 | 10 | 1) |
| Number of I/Os | 4 | 8 | 16 | 2) |
| Page Size [Bytes] | 1024 (1K) | 1024 (1K) | 2048 (2K) | 3) |

1) Referred to as 'colbits'

2) Referred to as 'org'

3) $PageSize = 2^{colbits} \times \frac{org}{8}$ [Bytes]

1.6 Input/Output Functional Description

Table 7 Input/Output Functional Description

| Symbol | Type | Function |
|---|-------|---|
| CK, \overline{CK} | Input | Clock: CK and \overline{CK} are differential system clock inputs. All address and control inputs are sampled on the crossing of the positive edge of \overline{CK} and negative edge of CK. Output (read) data is referenced to the crossing of CK and \overline{CK} (both direction of crossing) |
| CKE | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for self-refresh entry. Input buffers excluding CKE are disabled during self-refresh. CKE is used asynchronously to detect self-refresh exit condition. Self-refresh termination itself is synchronous. After V_{REF} has become stable during power-on and initialisation sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, \overline{CK} , ODT and CKE are disabled during power-down. |
| \overline{CS} | Input | Chip Select: All command are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external rank selection on systems with multiple memory ranks. \overline{CS} is considered part of the command code. |
| \overline{RAS} , \overline{CAS} , \overline{WE} | Input | Command Inputs: \overline{RAS} , \overline{CAS} and \overline{WE} (along with \overline{CS}) define the command being entered. |
| DM, LDM, UDM | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM and UDM are the input mask signals for x16 components and control the lower or upper bytes. For x8 components the data mask function is disabled, when RDQS / \overline{RQDS} are enabled by EMRS(1) command. |

Table 7 Input/Output Functional Description

| Symbol | Type | Function |
|---|----------------|--|
| BA0, BA1, BA2 | Input | Bank Address Inputs: BA0, BA1, BA2 define to which of the 8 internal memory banks an Activate, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle. |
| A[9:0], A10/AP, A[13:11] | Input | Address Inputs: Provides the row address for Activate commands and the column address and Auto-Precharge bit A10 (=AP) for Read/Write commands to select one location out of the memory array in the respective bank. A10(=AP) is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10=LOW) or all banks (A10=HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1 and BA2. The address inputs also provide the op-code during Mode Register Set commands. Row address A13 is used on x4 and x8 components only. |
| DQx | Input / Output | Data Inputs/Output: Bi-directional data bus. DQ[3:0] for x4 components, DQ[7:0] for x8 components and DQ[15:0] for x16 components |
| DQS, (\overline{DQS}) LDQS, (\overline{LDQS}) UDQS, (\overline{UDQS}) | Input / Output | Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. The datastrobes DQS, LDQS, UDQS may be used in single ended mode or paired with the optional complementary signals \overline{DQS} , \overline{LDQS} , \overline{UDQS} to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals. |
| RDQS, (\overline{RDQS}) | Input / Output | Read Data Strobe: For the x8 components a RDQS, \overline{RDQS} pair can be enabled via the EMRS(1) for read timing. RDQS, \overline{RDQS} is not supported on x4 and x16 components. RDQS, \overline{RDQS} are edge-aligned with read data. If RDQS, \overline{RDQS} is enabled, the DM function is disabled on x8 components. |
| ODT | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, \overline{DQS} and DM signal for x4 and DQ, DQS, \overline{DQS} , RDQS, \overline{RDQS} and DM for x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS, \overline{UDQS} , LDQS, \overline{LDQS} , UDM and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT. |
| NC | — | No Connect: No internal electrical connection is present |
| V _{DDQ} | Supply | DQ Power Supply: 1.8 V |
| V _{SSQ} | Supply | DQ Ground |
| V _{DDL} | Supply | DLL Power Supply: 1.8 V |
| V _{SSDL} | Supply | DLL Ground |
| V _{DD} | Supply | Power Supply: 1.8 V |
| V _{SS} | Supply | Ground |
| V _{REF} | Supply | Reference Voltage: 0.9 V ($V_{DDQ}/2$) |

1.7 Block Diagrams

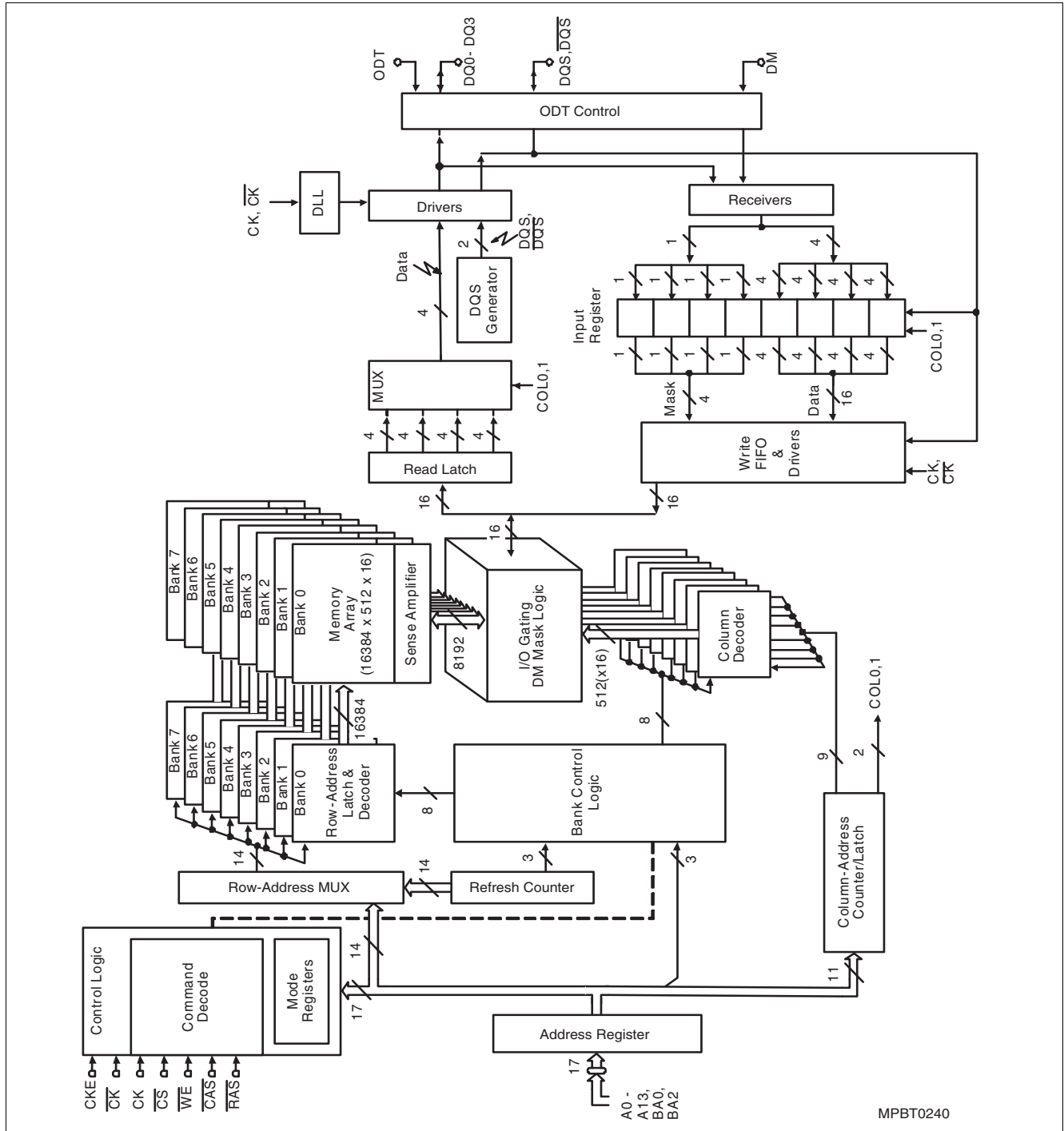


Figure 4 Block Diagram 32Mbit x 4 I/O x 8 banks

Notes

1. 256Mb x 4 Organisation with 14 Row, 3 Bank and 11 Column External Addresses
2. This Functional Block Diagram is intended to facilitate user understanding of the operation of the

device; it does not represent an actual circuit implementation.

3. DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

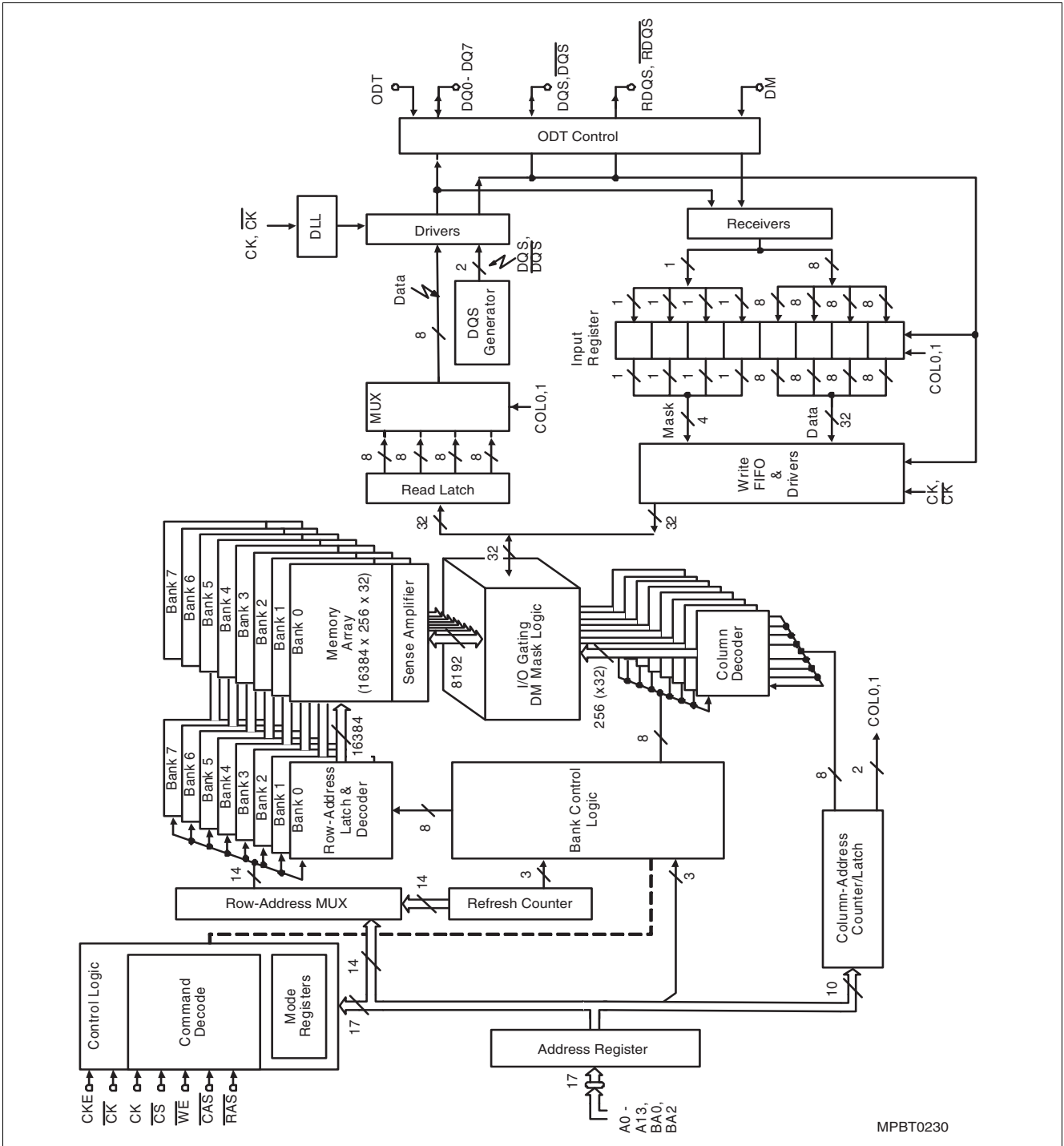


Figure 5 Block Diagram 16Mbit x 8 I/O x 8 banks

Notes

1. 128Mb x 8 Organisation with 14 Row, 3 Bank and 10 Column External Addresses
2. This Functional Block Diagram is intended to facilitate user understanding of the operation of the

3. DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

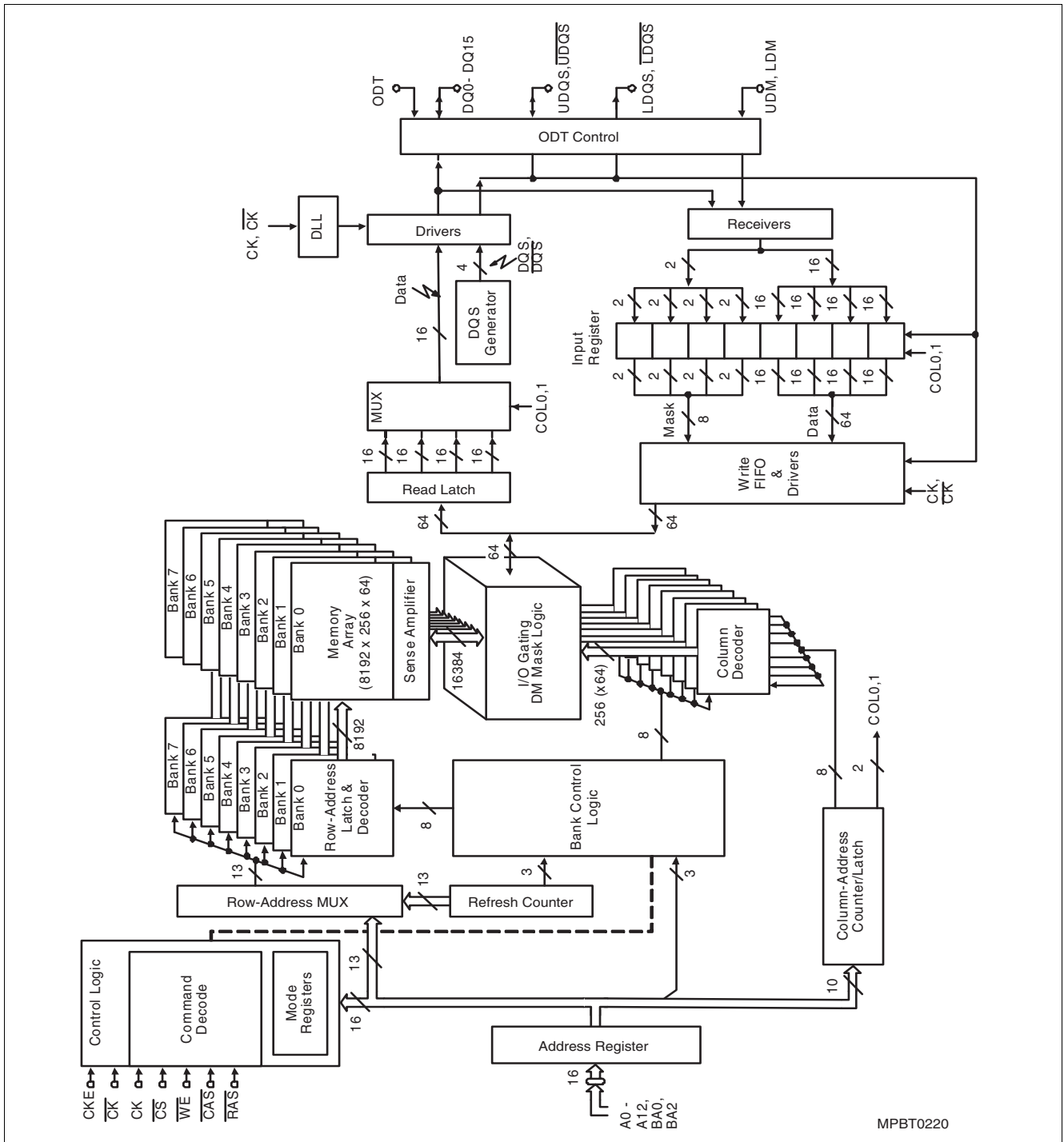


Figure 6 Block Diagram 8Mbit x 16 I/O x 8 banks

Notes

- 64Mb x 16 Organisation with 13 Row, 3 Bank and 10 Column External Addresses
- This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.
- UDM, LDM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional LDQS and UDQS signals.

2 Functional Description

2.1 Simplified State Diagram

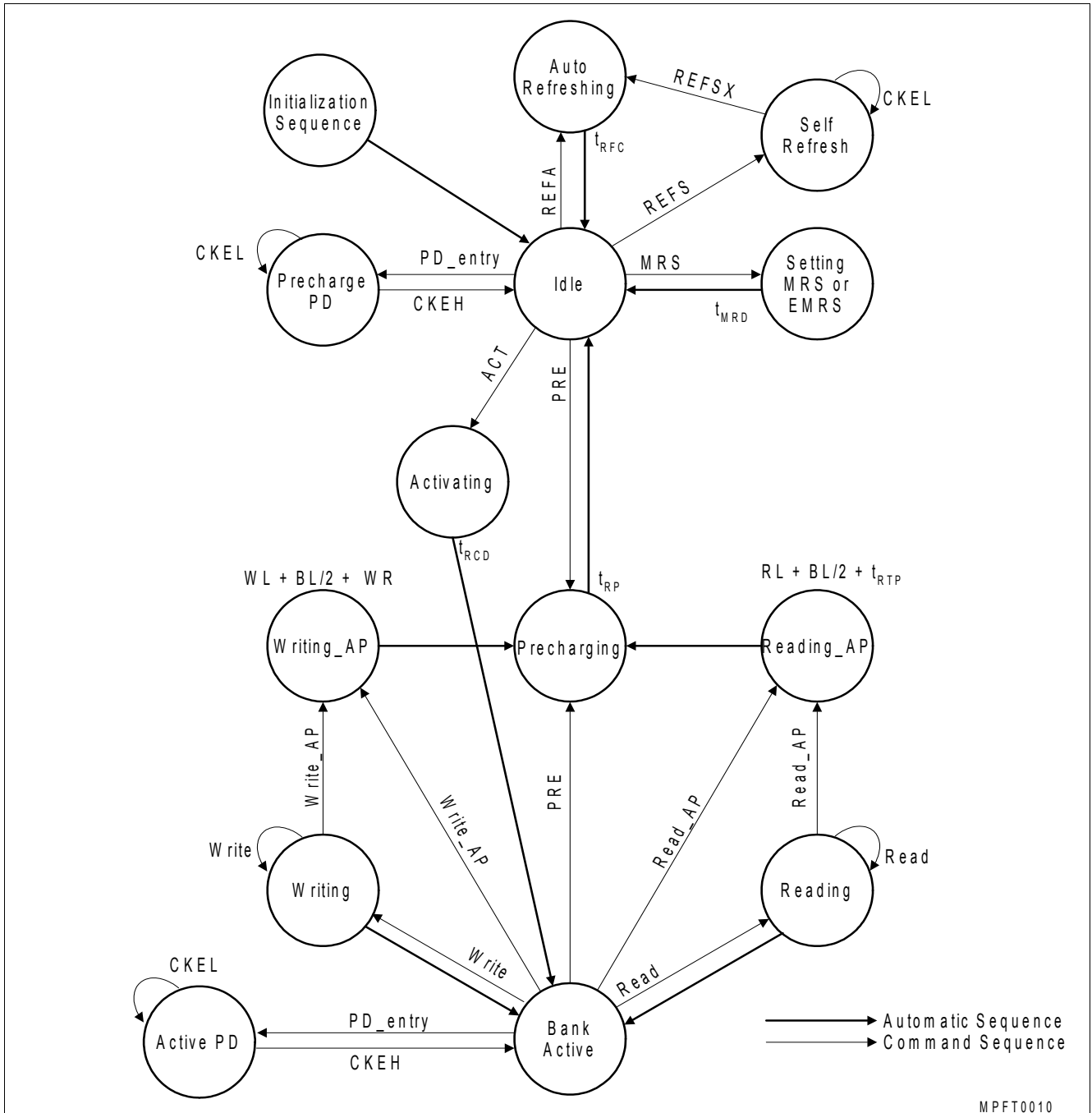


Figure 7 Simplified State Diagram

Note: This Simplified State Diagram is intended to provide a floorplan of the possible state transitions and the commands to control them. In particular situations involving more than one

bank, enabling / disabling on-die termination, Power-Down entry / exit - among other things - are not captured in full detail.

2.2 Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence.

Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accessed.

The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

2.2.1 Power On and Initialization

DDR2 SDRAM's must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below $0.2 \times V_{DDQ}$ and ODT at a low state (all other inputs may be undefined). To guarantee ODT off, V_{REF} must be valid and a low level must be applied to the ODT pin. Maximum power up interval for V_{DD} / V_{DDQ} is specified as 10.0 ms. The power interval is defined as the amount of time it takes for V_{DD} / V_{DDQ} to power-up from 0 V to $1.8 \text{ V} \pm 100 \text{ mV}$. At least one of these two sets of conditions must be met:
 - V_{DD} , V_{DDL} and V_{DDQ} are driven from a single power converter output, AND
 - V_{TT} is limited to 0.95 V max, AND
 - V_{ref} tracks $V_{DDQ}/2$

or

 - Apply V_{DD} before or at the same time as V_{DDQ} .
 - Apply V_{DDQ} before or at the same time as V_{TT} & V_{ref} .
2. Start clock (CK, \overline{CK}) and maintain stable power and clock condition for a minimum of 200 μs .
3. Apply NOP or Deselect commands and take CKE high.
4. Continue NOP or Deselect Commands for 400 ns, then issue a Precharge All command.
5. Issue EMRS(2) command.
6. Issue EMRS(3) command.
7. Issue EMRS(1) command to enable DLL.
8. Issue a MRS command for "DLL reset".
9. Issue Precharge-all command.
10. Issue 2 or more Auto-refresh commands.
11. Issue the final MRS command to turn the DLL on and to set the necessary operating parameter.
12. At least 200 clocks after step 8, issue EMRS(1) commands to either execute the OCD calibration or select the OCD default. Issue the final EMRS(1) command to exit OCD calibration mode and set the necessary operating parameters.
13. The DDR2 SDRAM is now ready for normal operation.

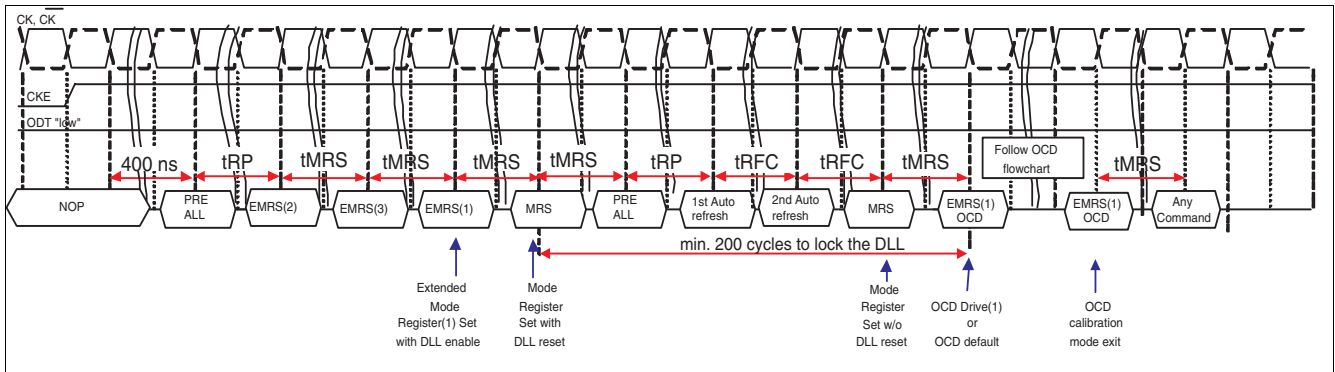


Figure 8 Initialization Sequence after Power Up

2.2.2 Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive $\overline{\text{CAS}}$ latency, driver impedance, On Die Termination (ODT), single-ended strobe and Off Chip Driver impedance adjustment (OCD) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command.

Contents of the Mode Register (MR) or Extended Mode Registers (EMR(1, 2, 3)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MR or EMR variables, all variables must be redefined when the MRS or EMRS commands are issued.

After initial power up, all MRS and EMRS Commands must be issued before read or write cycles may begin.

All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Either MRS or EMRS Commands are activated by the low signals of $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ at the positive edge of the clock.

When all bank addresses BA[2:0] are 0, the DDR2 SDRAM enables the MRS command. When the bank addresses BA0 is 1 and BA[2:1] are 0, the DDR2 SDRAM enables the EMRS(1) command.

The address input data during this cycle defines the parameters to be set as shown in the MRS and EMRS tables. A new command may be issued after the mode register set command cycle time (t_{MRD}).

MRS, EMRS and DLL Reset do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

2.2.2.1 DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs $\overline{\text{CAS}}$ latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications.

The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA[2:0], while controlling the state of address pins A[13:0]. The DDR2 SDRAM should be in all bank precharged (idle) mode with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command

and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality.

Burst length is defined by A[2:0] with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and $\overline{\text{CAS}}$ latency is defined by A[6:4]. A7 is used for test mode and must be set to 0 for normal DRAM operation. A8 is used for DLL reset. A[11:9] are used for write recovery time (WR) definition for Auto-Precharge mode. With address bit A12 two Power-Down modes can be selected, a "standard mode" and a "low-power" Power-Down mode, where the DLL is disabled. Address bit A13 and all "higher" address bits (including BA2) have to be set to 0 for compatibility with other DDR2 memory products with higher memory densities.

Functional Description

MR

Mode Register Definition

(BA[2:0] = 000_B)

| | | | | | | | | | | | | | | | | |
|-----------|-----|-----|-----------------|-----|-----|-----|----|-----|----|----|----|----|----|----|----|----|
| BA2 | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 0 | 0 | 0 | 0 ¹⁾ | PD | | WR | | DLL | TM | | CL | | BT | | BL | |
| reg. addr | | | | w | | w | | w | w | | w | | w | | w | |

1) A13 is only available for x4 and x8 configuration

| Field | Bits | Type ¹⁾ | Description |
|-------|--------|--------------------|---|
| BL | [2:0] | w | Burst Length 010 4 011 8 |
| BT | 3 | w | Burst Type 0 Sequential 1 Interleaved |
| CL | [6:4] | w | CAS Latency <i>Note: All other bit combinations are illegal.</i> 010 2 ²⁾ 011 3 100 4 101 5 |
| TM | 7 | w | Test Mode 0 Normal mode 1 Vendor specific test mode |
| DLL | 8 | w | DLL Reset 0 No 1 Yes |
| WR | [11:9] | w | Write Recovery³⁾ <i>Note: All other bit combinations are illegal.</i> 001 2 010 3 011 4 100 5 101 6 |
| PD | 12 | w | Active Power-Down Mode Select 0 Fast exit 1 Slow exit |

1) w = write only register bits

2) CAS Latency 2 is optional for Jedec compliant devices. This option is implemented in this device but is neither tested nor guaranteed.

3) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer:

$$WR[\text{cycles}] \geq t_{WR}(\text{ns}) / t_{CK}(\text{ns})$$

The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing. W_{Rmin} is determined by t_{CKmax} and W_{Rmax} is determined by t_{CKmin} .

2.2.3 DDR2 SDRAM Extended Mode Register Set (EMRS(1))

The Extended Mode Register EMR(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, \overline{DQS} and output buffers disable, RQDS and \overline{RDQS} enable. The default value of the extended mode register EMR(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on \overline{CS} , RAS, CAS, \overline{WE} , BA[2:1] and high

on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMR(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

EMR(1)

Extended Mode Register Definition (BA[2:0] = 001_B)

| BA2 | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----------|-----|-----|-----------------|-----------|------|------------------|-------------|----|----|-----|----|----|----|-----|-----|-----|
| 0 | 0 | 1 | 0 ¹⁾ | Q_{off} | RDQS | \overline{DQS} | OCD Program | | | Rtt | AL | | | Rtt | DIC | DLL |
| reg. addr | | | | w | w | | w | | w | | w | | w | w | w | |

1) A13 is only available for $\times 4$ and $\times 8$ configuration.

| Field | Bits | Type ¹⁾ | Description |
|------------------|-------|--------------------|---|
| DLL | 0 | w | DLL Enable 0 Enable 1 Disable |
| DIC | 1 | w | Off-chip Driver Impedance Control 0 Normal (Driver Size = 100%) 1 Weak (Driver Size = 60%) |
| R _{TT} | 2,6 | w | Nominal Termination Resistance of ODT <i>Note: All other bit combinations are illegal.</i> 00 ∞ (ODT disabled) 01 75 Ohm 10 150 Ohm |
| AL | [5:3] | w | Additive Latency <i>Note: All other bit combinations are illegal.</i> 000 0 001 1 010 2 011 3 100 4 |
| OCD Program | [9:7] | w | Off-Chip Driver Calibration Program 000 OCD calibration mode exit, maintain setting 001 Drive (1) 010 Drive (0) 100 Adjust mode 111 OCD calibration default |
| \overline{DQS} | 10 | w | Complement Data Strobe (\overline{DQS} Output) 0 Enable 1 Disable |
| RDQS | 11 | w | Read Data Strobe Output (RDQS, \overline{RDQS}) 0 Disable 1 Enable |

| Field | Bits | Type ¹⁾ | Description (cont'd) |
|-------------|------|--------------------|--|
| Qoff | 12 | w | Output Disable 0 Output buffers enabled 1 Output buffers disabled |

1) w = write only register bits

A0 is used for DLL enable or disable. A1 is used for enabling half-strength data-output driver. A2 and A6 enables On-Die termination (ODT) and sets the Rtt value. A[5:3] are used for additive latency settings and A[9:7] enables the OCD impedance adjustment mode. A10 enables or disables the differential DQS and RDQS signals, A11 disables or enables RDQS.

Address bit A12 have to be set to 0 for normal operation. With A12 set to 1 the SDRAM outputs are disabled and in Hi-Z. 1 on BA0 and 0 for BA[2:1] have to be set to access the EMRS(1). A13 and all "higher" address bits (including BA2) have to be set to 0 for compatibility with other DDR2 memory products with higher memory densities. Refer to **EMR(1)**.

Single-ended and Differential Data Strobe Signals

Table 8 lists all possible combinations for DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$ which can be programmed by A[11:10] address bits in EMRS(1). RDQS and $\overline{\text{RDQS}}$ are available in $\times 8$ components only.

If RDQS is enabled in $\times 8$ components, the DM function is disabled. RDQS is active for reads and don't care for writes.

Table 8 Single-ended and Differential Data Strobe Signals

| EMRS(1) | | Strobe Function Matrix | | | | Signaling |
|----------------------|--|------------------------|--------------------------|-----|-------------------------|--------------------------|
| A11 (RDQS Enable) | A10 ($\overline{\text{DQS}}$ Enable) | RDQS/DM | $\overline{\text{RDQS}}$ | DQS | $\overline{\text{DQS}}$ | |
| 0 (Disable) | 0 (Enable) | DM | Hi-Z | DQS | $\overline{\text{DQS}}$ | differential DQS signals |
| 0 (Disable) | 1 (Disable) | DM | Hi-Z | DQS | Hi-Z | single-ended DQS signals |
| 1 (Enable) | 0 (Enable) | RDQS | $\overline{\text{RDQS}}$ | DQS | $\overline{\text{DQS}}$ | differential DQS signals |
| 1 (Enable) | 1 (Disable) | RDQS | Hi-Z | DQS | Hi-Z | single-ended DQS signals |

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation.

Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSK} parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMR(1) is set to 0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the

DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current and external load currents.

2.2.3.1 EMR(2)

The Extended Mode Registers EMR(2) and EMR(3) are reserved for future use and must be programmed when setting the mode register during initialization.

The extended mode register EMR(2) is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, BA2, BA0 and high on BA1, while controlling the states of the address pins. The DDR2 SDRAM should be in all bank

precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMR(2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

EMR(2) Programming

Extended Mode Register Definition (BA[2:0] = 010_B)

| BA2 | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----|-----|-----|-----|-----|-----|-----|----|----|----|-------------------|----|----|----|----|----|----|
| 0 | 1 | 0 | | | | | | | | 0 ¹⁾²⁾ | | | | | | |

reg. addr

- 1) A13 is only available for ×4 and ×8 configuration.
- 2) Must be programmed to “0”

2.2.3.2 EMR(3)

The Extended Mode Register EMR(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMR(3) Programming

Extended Mode Register Definition (BA[2:0] = 011_B)

| BA2 | BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----|-----|-----|-----|-----|-----|-----|----|----|----|-------------------|----|----|----|----|----|----|
| 0 | 1 | 1 | | | | | | | | 0 ¹⁾²⁾ | | | | | | |

reg. addr

- 1) A13 is only available for ×4 and ×8 configuration.
- 2) Must be programmed to “0”

2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other

command being issued. MRS should be set before entering OCD impedance adjustment and On Die Termination (ODT) should be carefully controlled depending on system environment.

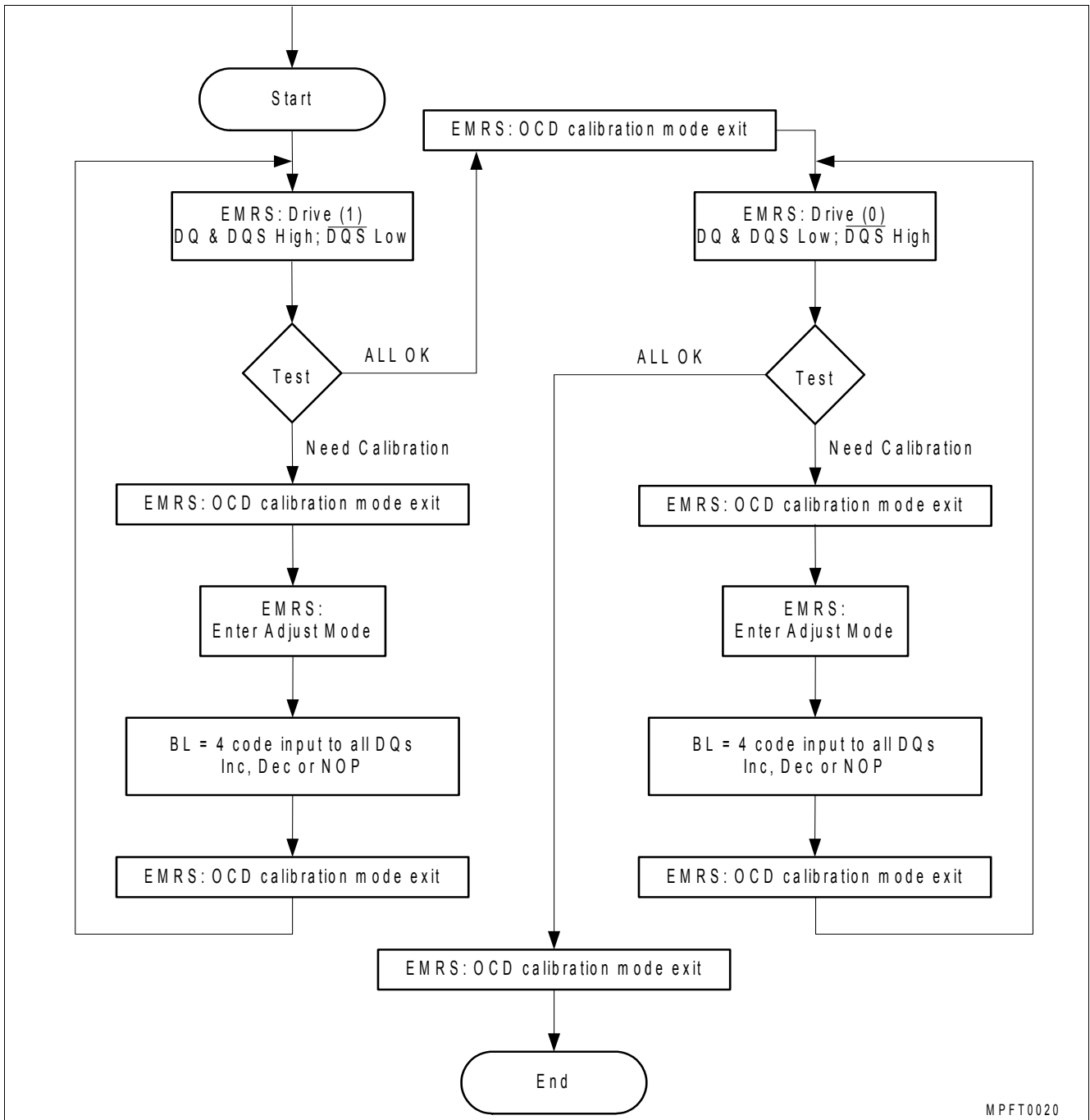


Figure 9 OCD Impedance Adjustment Flow Chart

Note: MR should be set before entering OCD impedance adjustment and ODT should be carefully controlled depending on system environment

Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS(1) mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMR(1) bit enabling RDQS operation. In Drive(1) mode, all \overline{DQ} , \overline{DQS} (and \overline{RDQS}) signals are driven high and all \overline{DQS} (and \overline{RDQS}) signals are driven low. In Drive(0) mode, all \overline{DQ} , \overline{DQS} (and \overline{RDQS}) signals are driven low and all \overline{DQS} (and \overline{RDQS}) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and

voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMR(1) and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A[9:7] as '000' in order to maintain the default or calibrated value.

Table 9 Off Chip Driver Program

| A9 | A8 | A7 | Operation |
|----|----|----|---|
| 0 | 0 | 0 | OCD calibration mode exit |
| 0 | 0 | 1 | Drive(1) \overline{DQ} , \overline{DQS} , (\overline{RDQS}) high and \overline{DQS} (\overline{RDQS}) low |
| 0 | 1 | 0 | Drive(0) \overline{DQ} , \overline{DQS} , (\overline{RDQS}) low and \overline{DQS} (\overline{RDQS}) high |
| 1 | 0 | 0 | Adjust mode |
| 1 | 1 | 1 | OCD calibration default |

OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS(1) command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 in the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs

simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the maximum step count range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 10 Off-Chip-Driver Adjust Program

| 4 bit burst code inputs to all DQs | | | | Operation | |
|------------------------------------|-----------------|-----------------|-----------------|-------------------------|---------------------------|
| D _{T0} | D _{T1} | D _{T2} | D _{T3} | Pull-up driver strength | Pull-down driver strength |
| 0 | 0 | 0 | 0 | NOP (no operation) | NOP (no operation) |
| 0 | 0 | 0 | 1 | Increase by 1 step | NOP |
| 0 | 0 | 1 | 0 | Decrease by 1 step | NOP |
| 0 | 1 | 0 | 0 | NOP | Increase by 1 step |
| 1 | 0 | 0 | 0 | NOP | Decrease by 1 step |
| 0 | 1 | 0 | 1 | Increase by 1 step | Increase by 1 step |
| 0 | 1 | 1 | 0 | Decrease by 1 step | Increase by 1 step |
| 1 | 0 | 0 | 1 | Increase by 1 step | Decrease by 1 step |
| 1 | 0 | 1 | 0 | Decrease by 1 step | Decrease by 1 step |
| Other Combinations | | | | Illegal | |

Functional Description

For proper operation of adjust mode, $WL = RL - 1 = AL + CL - 1$ clocks and t_{DS} / t_{DH} should be met as shown in **Figure 10**. Input data pattern for adjustment, $DT[0:3]$ is fixed and not affected by MRS addressing mode (i.e. sequential or interleave).

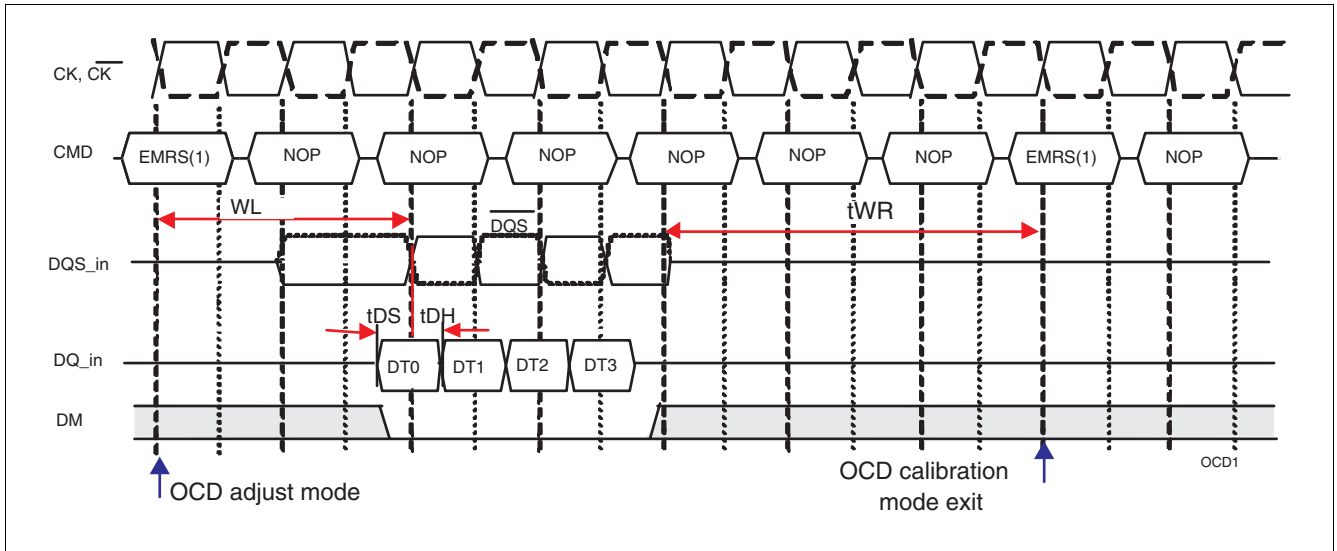


Figure 10 Timing Diagram Adjust Mode

Drive Mode

Both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out t_{OIT} after “enter drive mode” command and all output drivers are turned-off t_{OIT} after “OCD calibration mode exit” command. See **Figure 11**.

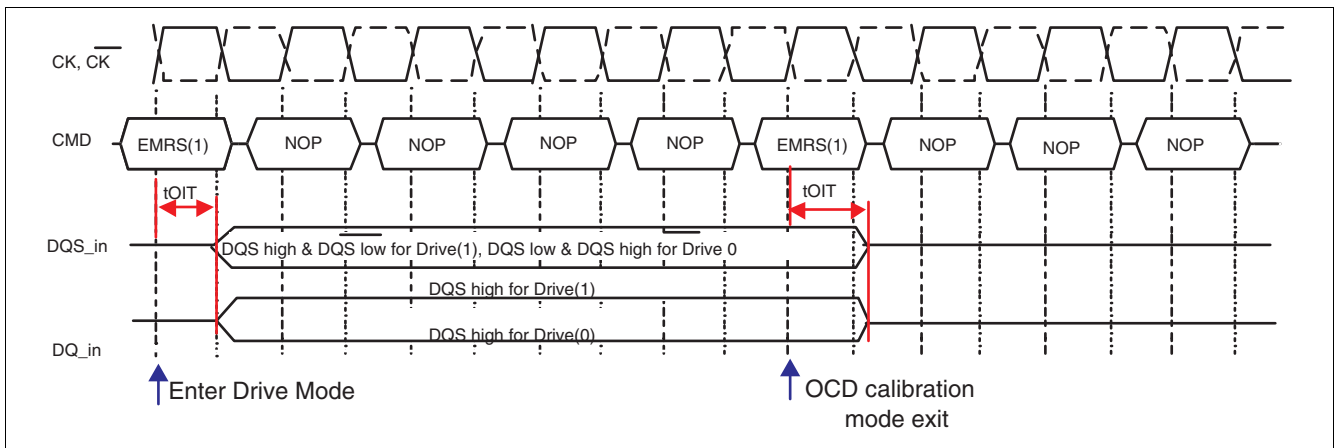


Figure 11 Timing Diagram Drive Mode

2.4 On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS, \overline{DQS} , DM for $\times 4$ and DQ, DQS, \overline{DQS} , DM, RDQS (DM/RDQS share the same pin) and \overline{RDQS} for $\times 8$ configuration via the ODT control pin. \overline{DQS} and \overline{RDQS} are only terminated when enabled by EMR(1).

For $\times 16$ configuration ODT is applied to each DQ, UDQS, \overline{UDQS} , LDQS, \overline{LDQS} , UDM and LDM signal via the ODT control pin. UDQS and LDQS are terminated

only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

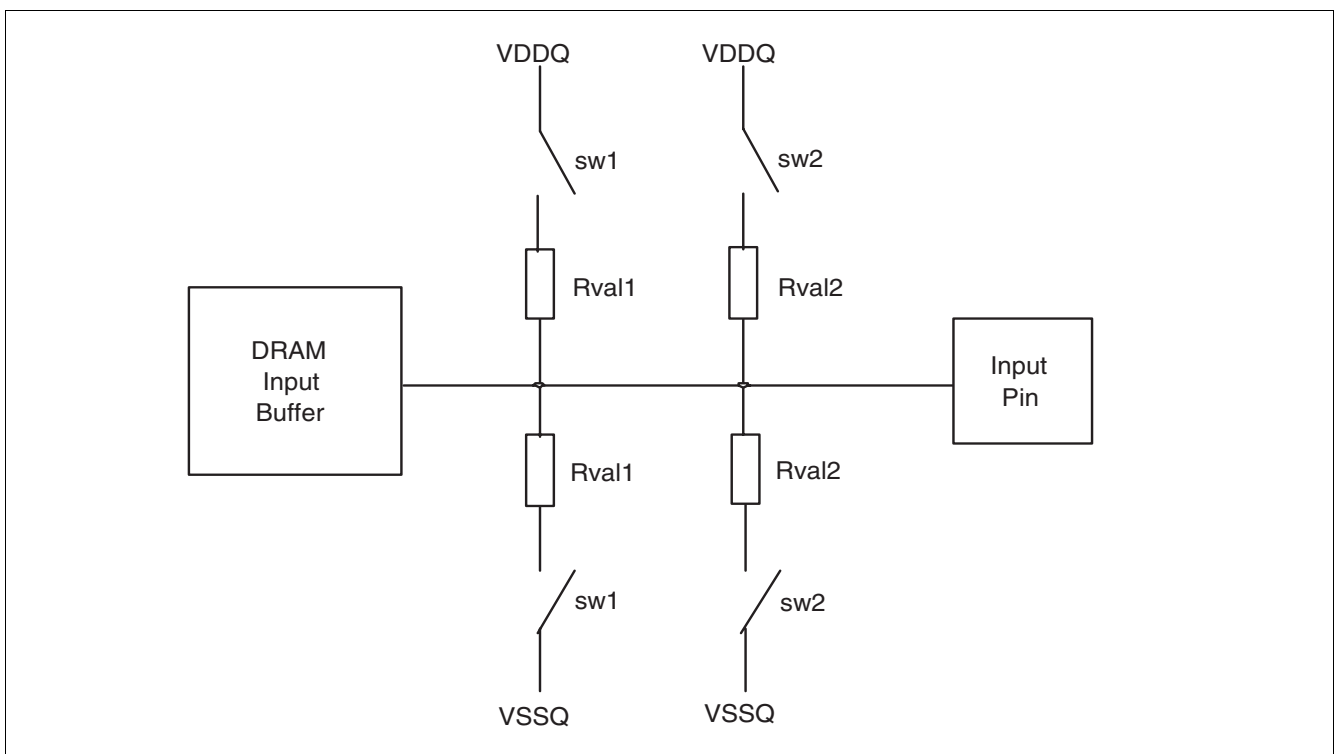


Figure 12 Functional Representation of ODT

Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS(1) address bits A6 & A2.

Target: $Rval1 = Rval2 = 2 \times Rtt$

The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.

ODT timing modes

Depending on the operating mode asynchronous or synchronous ODT timings apply.

Asynchronous ODT timings (t_{AOFPD} , t_{AONPD}) apply when the on-die DLL is disabled.

These modes are:

- Slow Exit Active Power Down Mode (with MRS bit A12 is set to "1")
- Precharge Power Down Mode

Synchronous ODT timings (t_{AOND} , t_{AOFD} , t_{AON} , t_{AOF}) apply for all other modes.

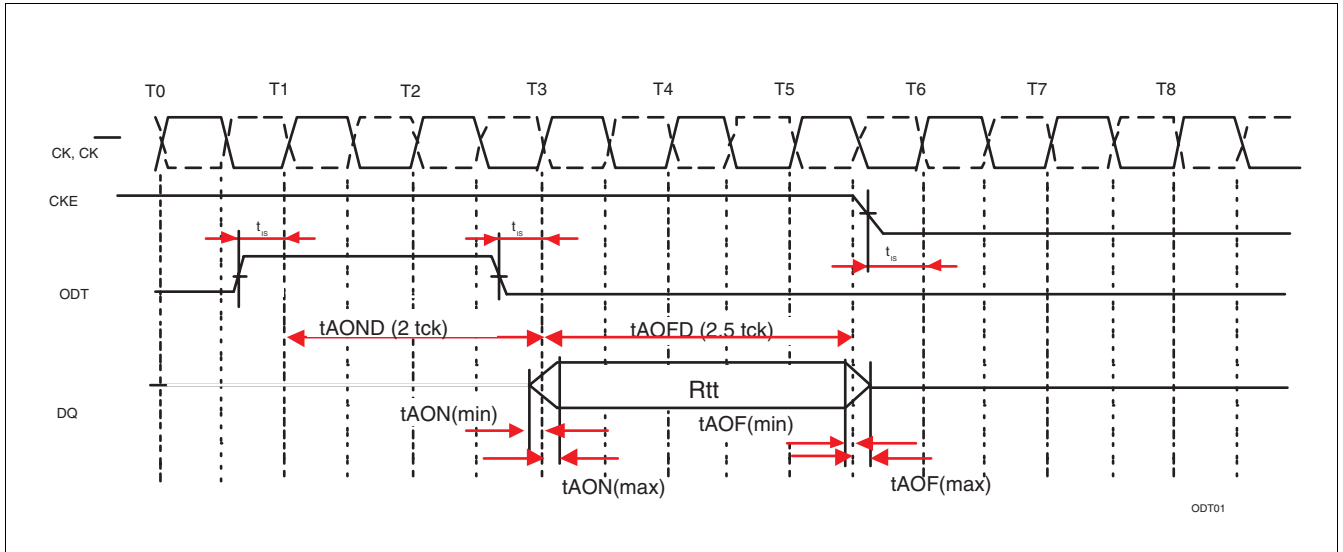


Figure 13 ODT Timing for Active and Standby (Idle) Modes (Synchronous ODT timings)

Note

1. Synchronous ODT timings apply for Active Mode and Standby Mode with CKE HIGH and for the "Fast Exit" Active Power Down Mode (MRS bit A12 set to "0"). In all these modes the on-die DLL is enabled.
2. ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON,max}$) is when the ODT resistance is fully on. Both are measured from t_{AOND} .
3. ODT turn off time min. ($t_{AOF,min}$) is when the device starts to turn off the ODT resistance. ODT turn off time max. ($t_{AOF,max}$) is when the bus is in high impedance. Both are measured from t_{AOFD} .

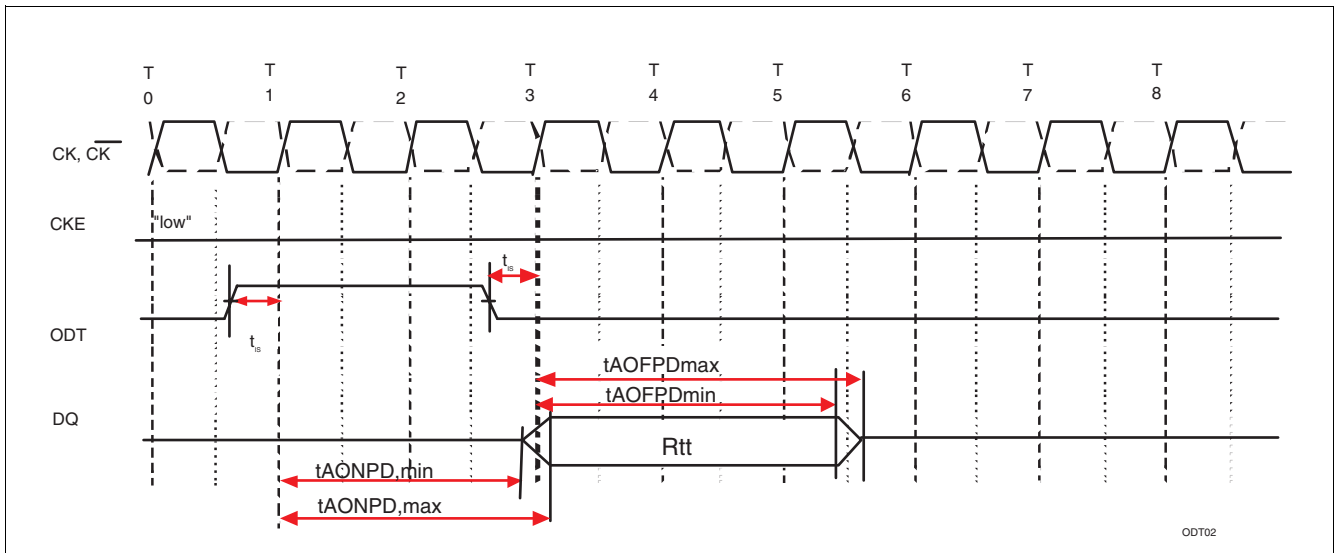


Figure 14 ODT Timing for Precharge Power-Down and Active Power-Down Mode (with slow exit) (Asynchronous ODT timings)

Note: Asynchronous ODT timings apply for Precharge Power-Down Mode and "Slow Exit" Active Power Down Mode (MRS bit A12 set to "1"), where the on-die DLL is disabled in this mode of operation.

ODT timing mode switch

When entering the Power Down Modes “Slow Exit” Active Power Down and Precharge Power Down two additional timing parameters (t_{ANPD} and t_{AXPD}) define if synchronous or asynchronous ODT timings have to be applied.

Mode entry

As long as the timing parameter $t_{ANPD,min}$ is satisfied when ODT is turned on or off before entering these power-down modes, synchronous timing parameters can be applied. If $t_{ANPD,min}$ is not satisfied, asynchronous timing parameters apply.

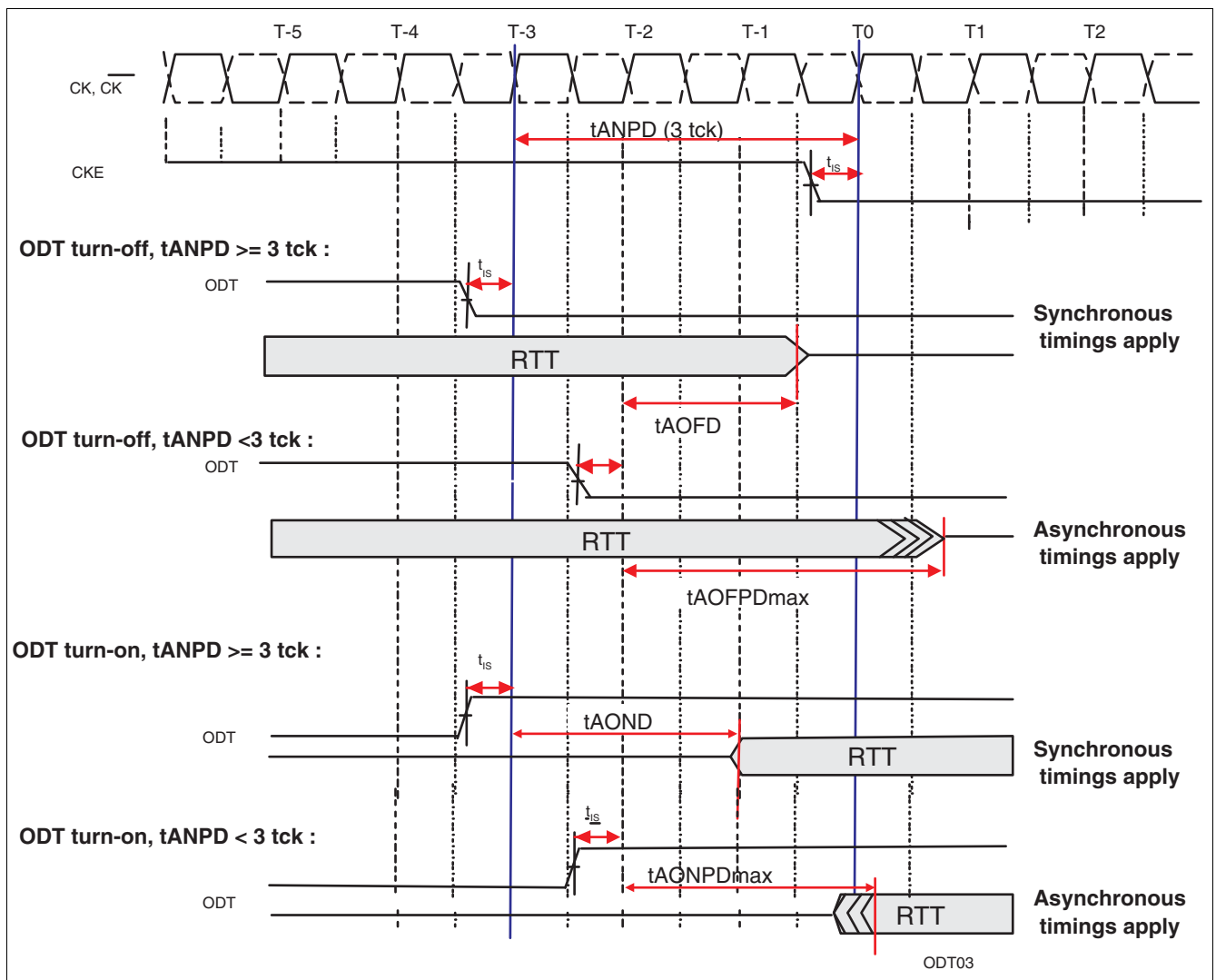


Figure 15 ODT Mode Entry Timing Diagram

Mode exit

As long as the timing parameter $t_{AXPD,min}$ is satisfied when ODT is turned on or off after exiting these power-down modes, synchronous timing parameters can be

applied. If $t_{AXPD,min}$ is not satisfied, asynchronous timing parameters apply.

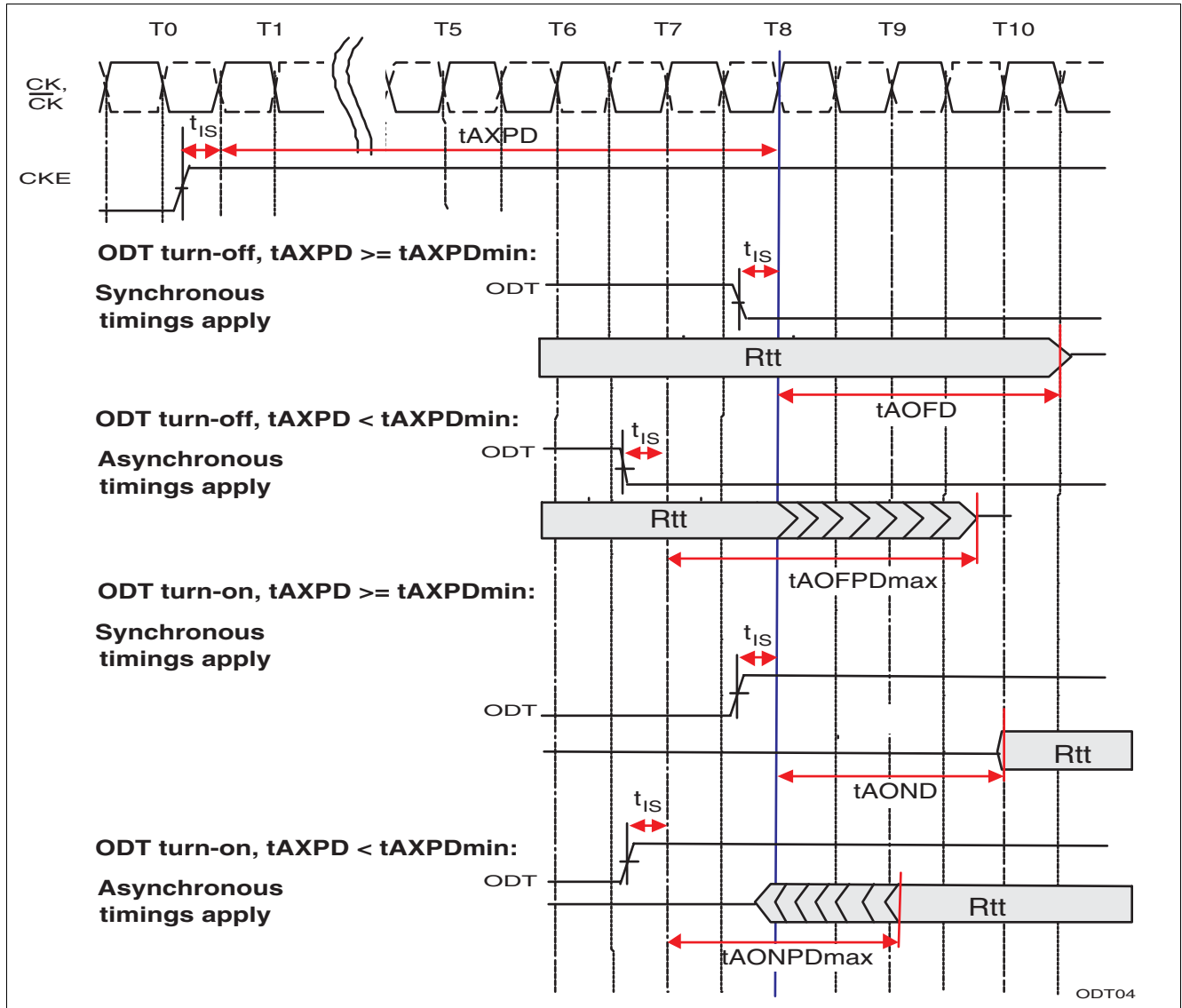


Figure 16 ODT Mode Exit Timing Diagram

2.5 Bank Activate Command

The Bank Activate command is issued by holding \overline{CAS} and \overline{WE} HIGH with \overline{CS} and \overline{RAS} LOW at the rising edge of the clock. The bank addresses BA[2:0] are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for $\times 4$ and $\times 8$ organized components. For $\times 16$ components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command

(with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the $t_{RCD,min}$ specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure $t_{RCD,min}$ is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} ,

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respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by t_{RC} . The minimum time interval between Bank Active commands to different banks is t_{RRD} .

In order to ensure that components with 8 internal memory banks do not exceed the instantaneous current supplying capability, certain restrictions on operation of the 8 banks must be observed. There are two rules.

One for restricting the number of sequential Active commands that can be issued and another for allowing

more time for \overline{RAS} precharge for a Precharge-All command. The rules are as follows:

1. Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing $t_{FAW(ns)}$ by $t_{CK(ns)}$ and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clocks N + 1 through N + 9.
2. Precharge All Allowance: t_{RP} for a Precharge-All command must be increased by 1 t_{CK} .

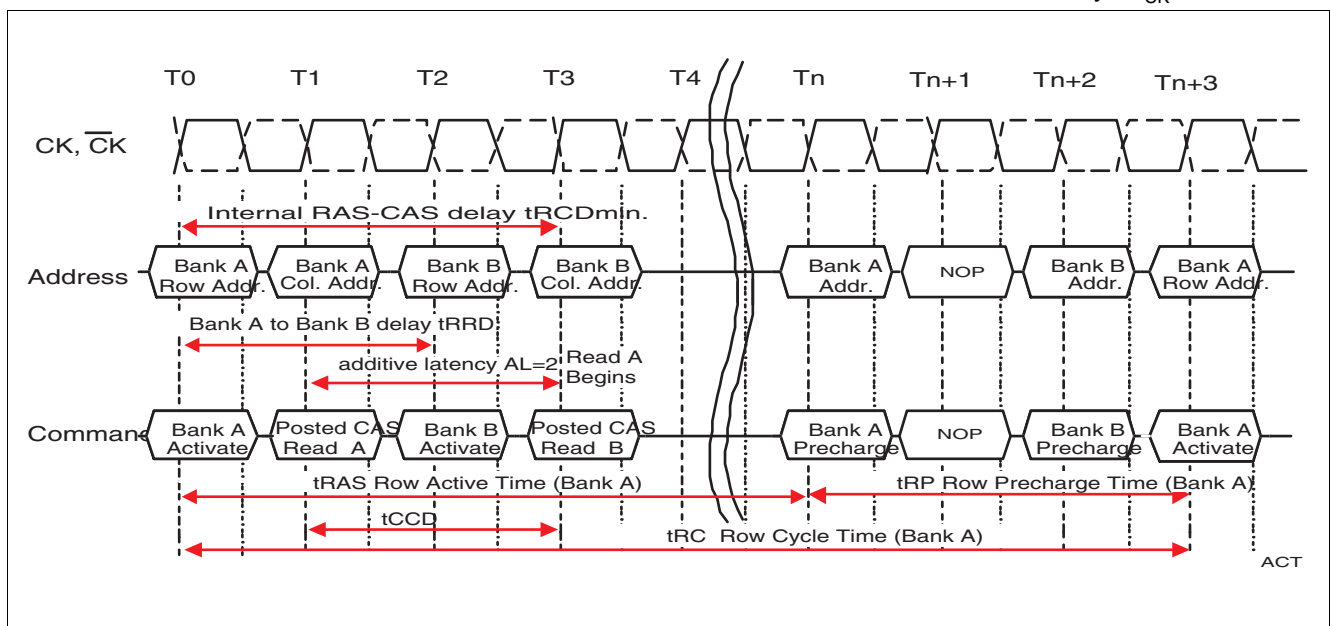


Figure 17 Bank Activate Command Cycle: $t_{RCD} = 3$, $AL = 2$, $t_{RP} = 3$, $t_{RRD} = 2$

2.6 Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting \overline{RAS} HIGH, \overline{CS} and \overline{CAS} LOW at the clock's rising edge. \overline{WE} must also be defined at this time to determine whether the access cycle is a read operation (\overline{WE} HIGH) or a write operation (\overline{WE} LOW). The DDR2 SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 533 Mb/sec/pin for main memory. The boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 64Mbit \times 16 chip has a page size of 2048 kByte which corresponds to a page length of 1024 bits (defined by CA[9:0]).

In case of a 4-bit burst operation (burst length = 4) the page length of 1024 is divided into 256 uniquely addressable segments (4-bits \times 16 I/O each). The 4-bit

burst operation will occur entirely within one of the 256 segments (defined by CA[7:0]) starting with the column address supplied to the device during the Read or Write Command (CA[9:0]). The second, third and fourth access will also occur within this segment, however, the burst order is a function of the starting address, and the burst sequence.

In case of a 8-bit burst operation (burst length = 8) the page length of 1024 is divided into 128 uniquely addressable segments (8-bits \times 16 I/O each). The 8-bit burst operation will occur entirely within one of the 128 segments (defined by CA[6:0]) beginning with the column address supplied to the device during the Read or Write Command (CA[9:0]).

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum \overline{CAS} to \overline{CAS} delay (t_{CCD}) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8) the minimum $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay (t_{CCD}) is 4 clocks for read or write cycles.

Burst interruption is allowed with 8 bit burst operation. For details see [Chapter 2.6.6](#).

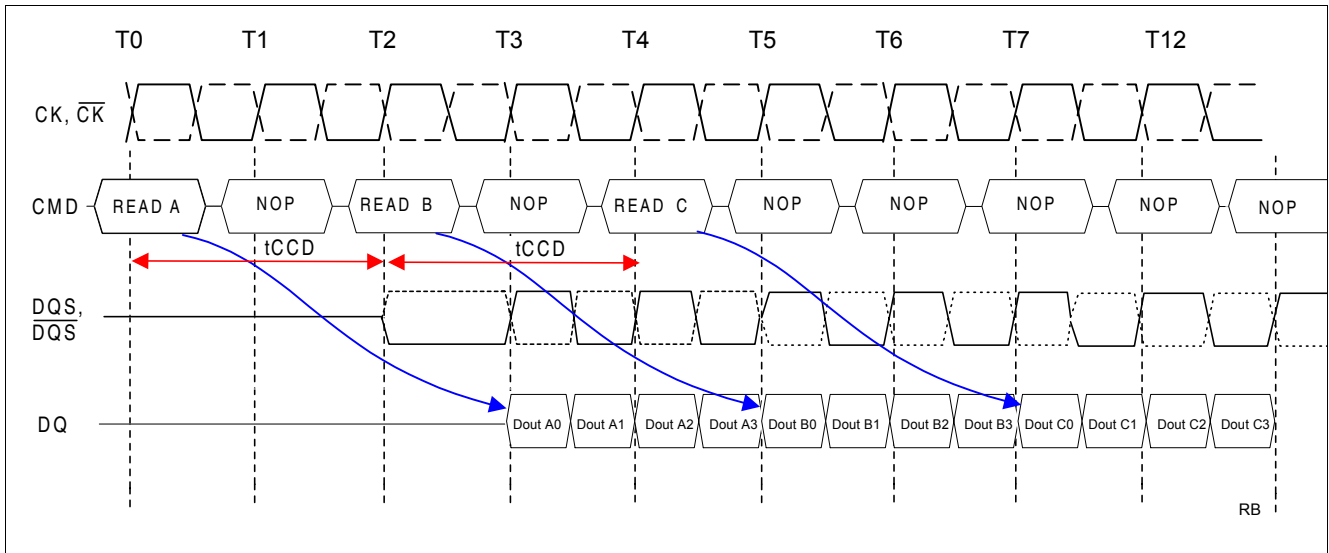


Figure 18 Read Burst Timing Example: (CL = 3, AL = 0, RL = 3, BL = 4)

2.6.1 Posted CAS

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the bank activate command (or any time during the $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time, t_{RCD} period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{\text{CAS}}$

latency (CL). Therefore if a user chooses to issue a Read/Write command before the $t_{\text{RCD},\text{min}}$, then AL greater than 0 must be written into the EMR(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency - 1) where Read Latency is defined as the sum of Additive Latency plus CAS latency (RL=AL+CL). If a user chooses to issue a Read command after the $t_{\text{RCD},\text{min}}$ period, the Read Latency is also defined as RL = AL + CL.

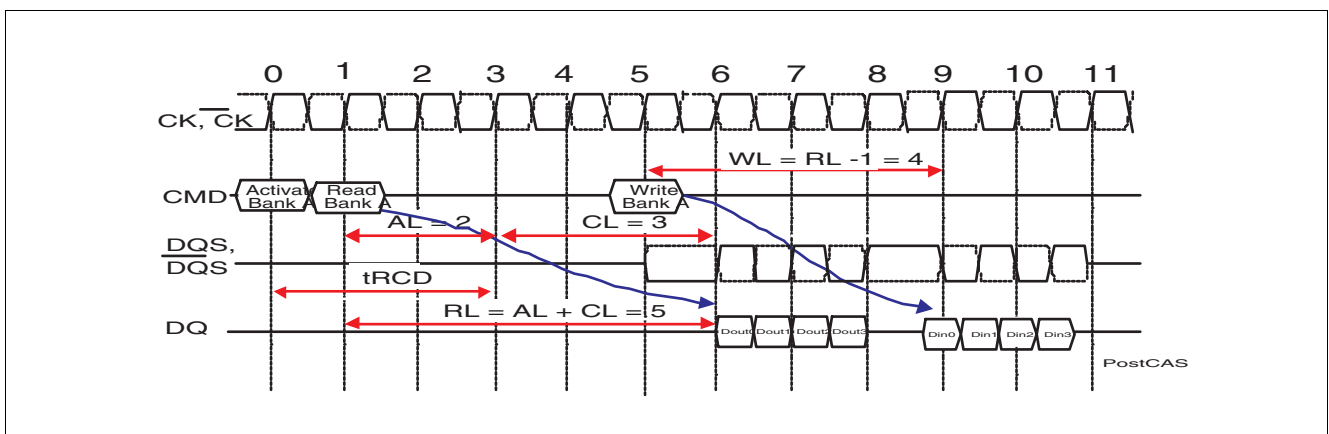


Figure 19 Activate to Read Timing Example: Read followed by a write to the same bank, Activate to Read delay $< t_{\text{RCD},\text{min}}$: AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4

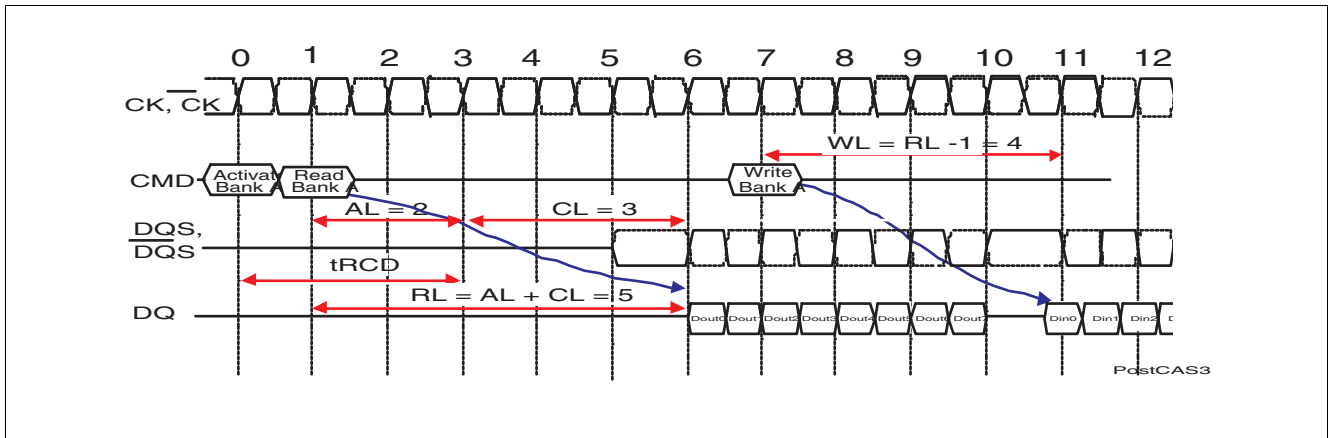


Figure 20 Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay $< t_{RCDmin}$: $AL = 2$ and $CL = 3$, $RL = (AL + CL) = 5$, $WL = (RL - 1) = 4$, $BL = 8$

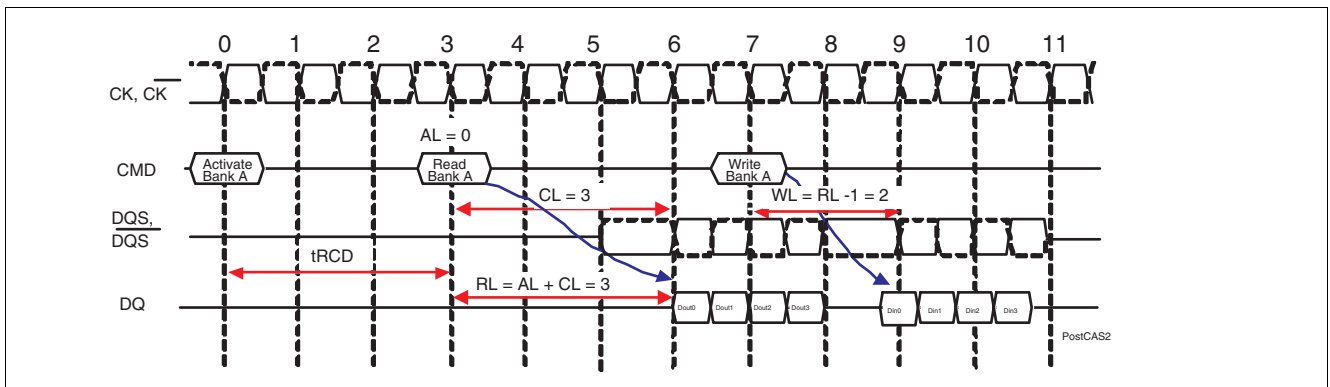


Figure 21 Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay $= t_{RCDmin}$: $AL = 0$, $CL = 3$, $RL = (AL + CL) = 3$, $WL = (RL - 1) = 2$, $BL = 4$

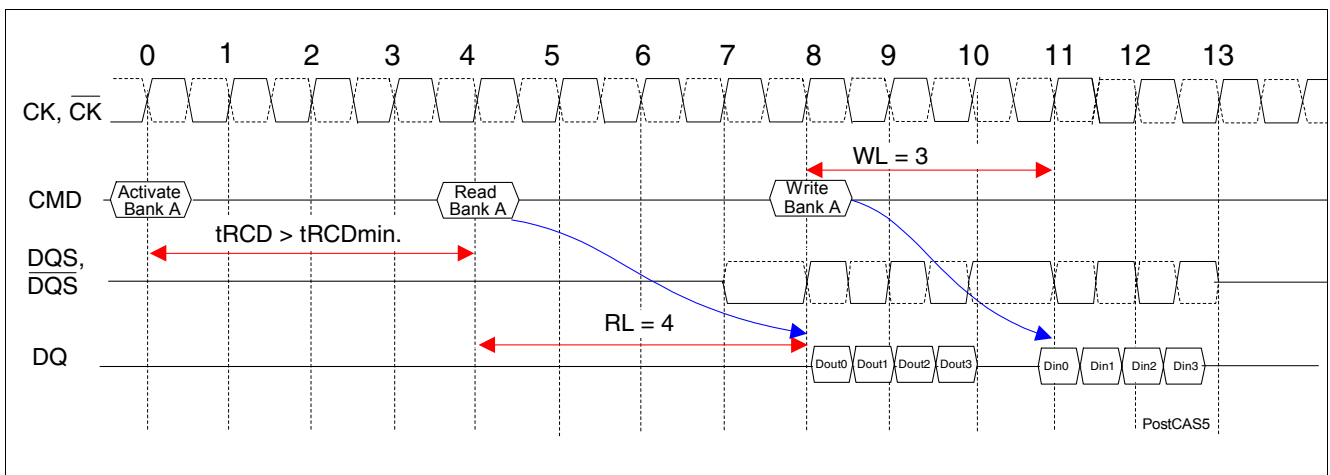


Figure 22 Read to Write Timing Example: Read followed by a write to the same bank, Activate to Read delay $> t_{RCDmin}$: $AL = 1$, $CL = 3$, $RL = 4$, $WL = 3$, $BL = 4$

2.6.2 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A[2:0] of

the MR. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MR. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the [Chapter 2.6.6](#). A Burst Stop command is not supported on DDR2 SDRAM devices.

Table 11 Burst Length and Sequence

| Burst Length | Starting Address (A2 A1 A0) | Sequential Addressing (decimal) | Interleave Addressing (decimal) |
|--------------|-----------------------------|---------------------------------|---------------------------------|
| 4 | 0 0 0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | 0 0 1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | 0 1 0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | 0 1 1 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 0 0 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 0 0 1 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 0 1 0 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 0 1 1 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 1 0 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 1 0 1 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 1 1 0 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 1 1 1 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 |

Note

1. *Page Size and Length is a function of I/O organization:*
 - 256 Mb × 4 organization (CA[9:0], CA11); Page Size = 1 kByte; Page Length = 2048
 - 128 Mb × 8 organization (CA[9:0]); Page Size = 1 kByte; Page Length = 1024
 - 64 Mb × 16 organization (CA[9:0]); Page Size = 2 kByte; Page Length = 1024
2. *Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components*

2.6.3 Read Command

The Read command is initiated by having \overline{CS} and \overline{CAS} LOW while holding \overline{RAS} and \overline{WE} HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven

onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus \overline{CAS} latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS(1)).

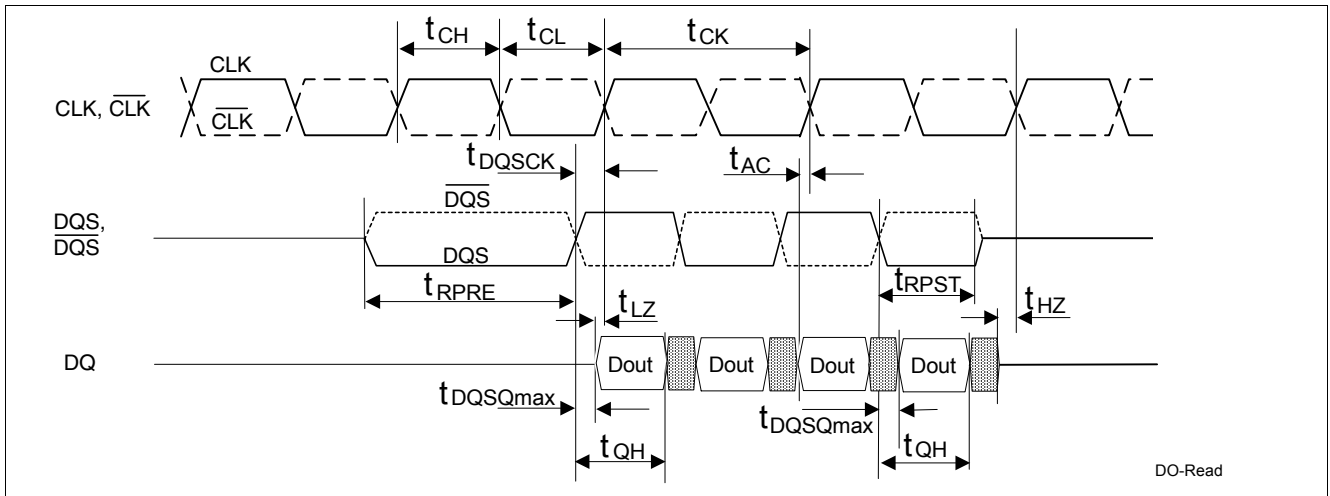


Figure 23 Basic Read Timing Diagram

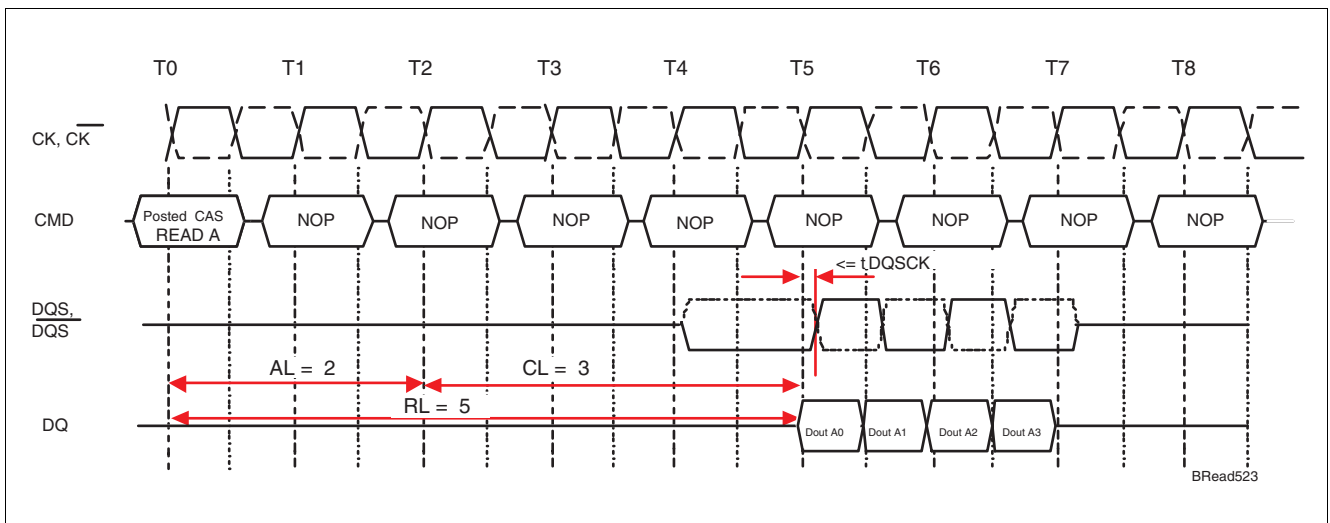


Figure 24 Burst Operation Example 1: RL = 5 (AL = 2, CL = 3, BL = 4)

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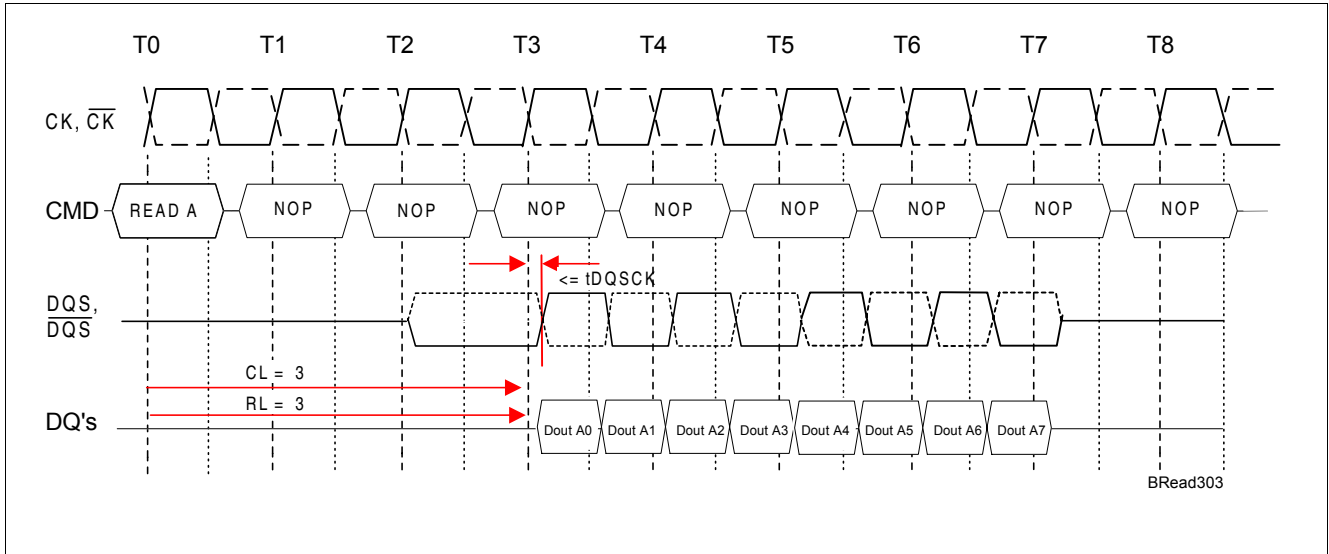


Figure 25 Read Operation Example 2: $RL = 3$ ($AL = 0$, $CL = 3$, $BL = 8$)

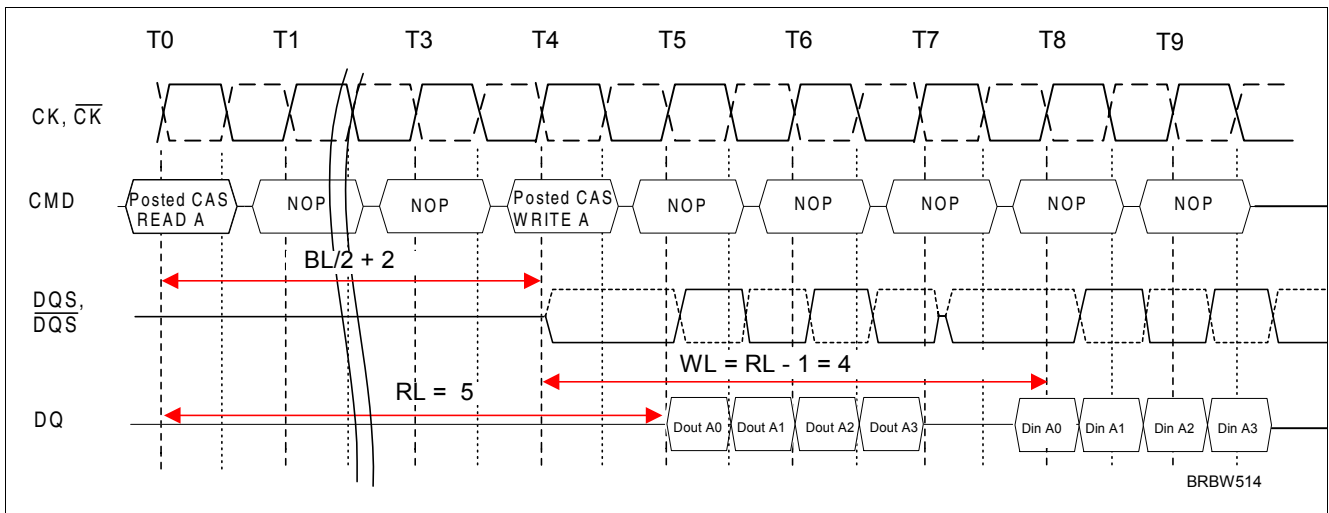


Figure 26 Read followed by Write Example: $RL = 5$, $WL = (RL - 1) = 4$, $BL = 4$

The minimum time from the read command to the write command is defined by a read-to-write turn-around time, which is $BL/2 + 2$ clocks.

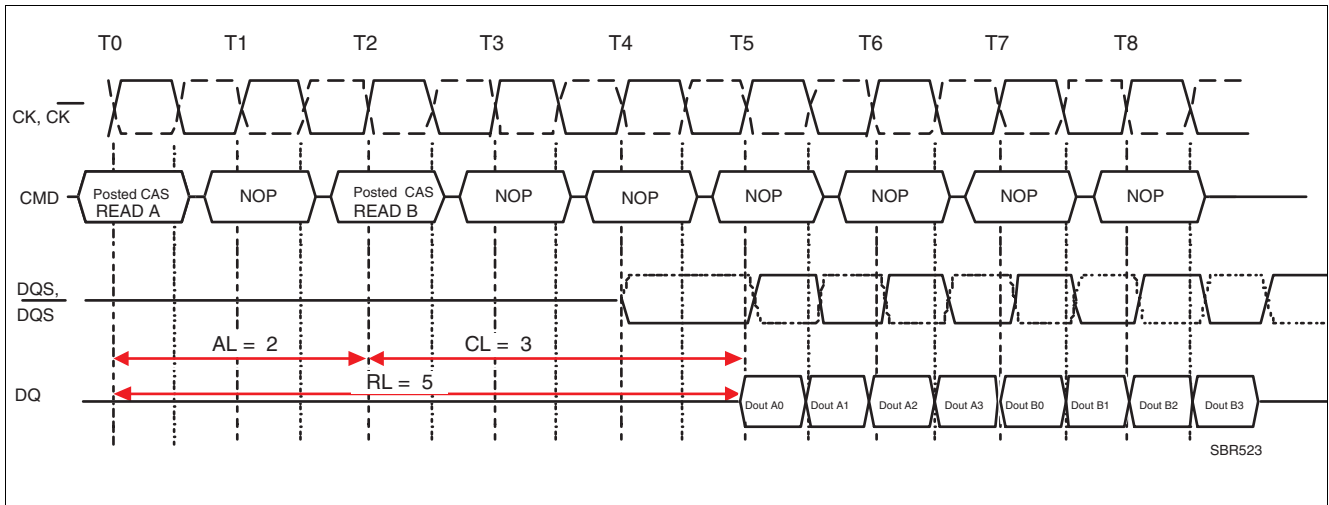


Figure 27 Seamless Read Operation Example 1: RL = 5, AL = 2, CL = 3, BL = 4

The seamless read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

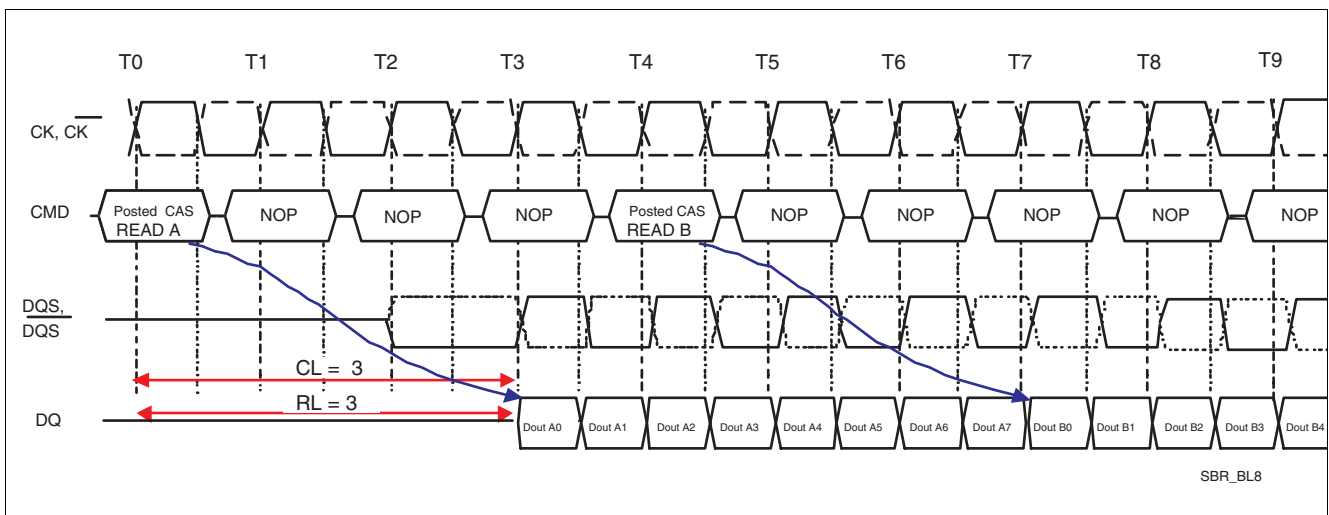


Figure 28 Seamless Read Operation Example 2: RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)

The seamless, non interrupting 8-bit read operation is supported by enabling a read command at every BL/2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.6.4 Write Command

The Write command is initiated by having \overline{CS} , \overline{CAS} and \overline{WE} LOW while holding \overline{RAS} HIGH at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to $(AL + CL - 1)$. A data strobe signal (DQS) has to be driven LOW (preamble) a time t_{WPRE} prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for write cycles. The subsequent burst bit data are issued on

successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named "write recovery time" (t_{WR}) and is the time needed to store the write data into the memory array. t_{WR} is an analog timing parameter (see Chapter 5) and is not the programmed value for WR in the MRS.

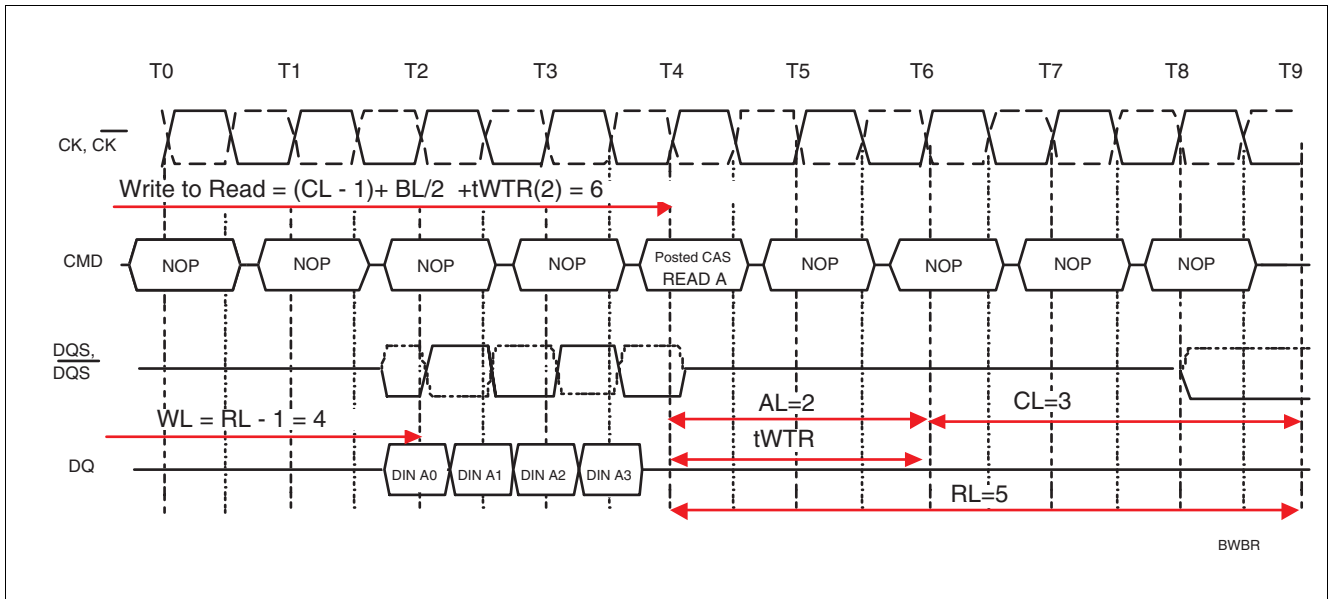


Figure 32 Write followed by Read Example: $RL = 5$ ($AL = 2$, $CL = 3$), $WL = 4$, $t_{WTR} = 2$, $BL = 4$

The minimum number of clocks from the write command to the read command is $(CL - 1) + BL/2 + t_{WTR}$, where t_{WTR} is the write-to-read turn-around time t_{WTR} expressed in clock cycles. The t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

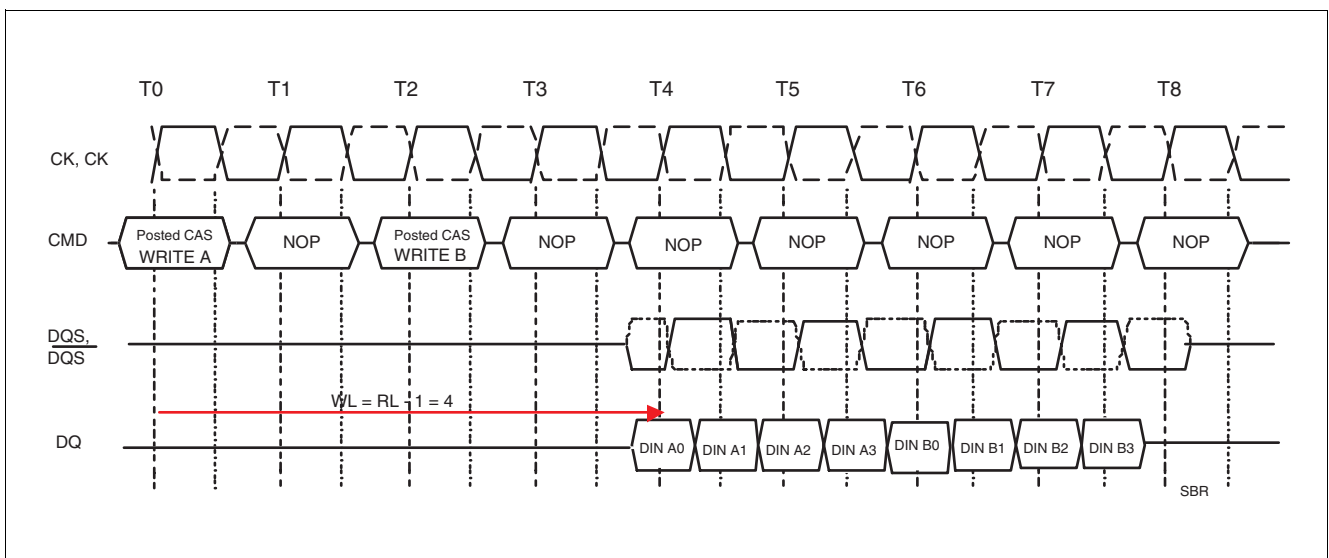


Figure 33 Seamless Write Operation Example 1: $RL = 5$, $WL = 4$, $BL = 4$

The seamless write operation is supported by enabling a write command every $BL/2$ number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

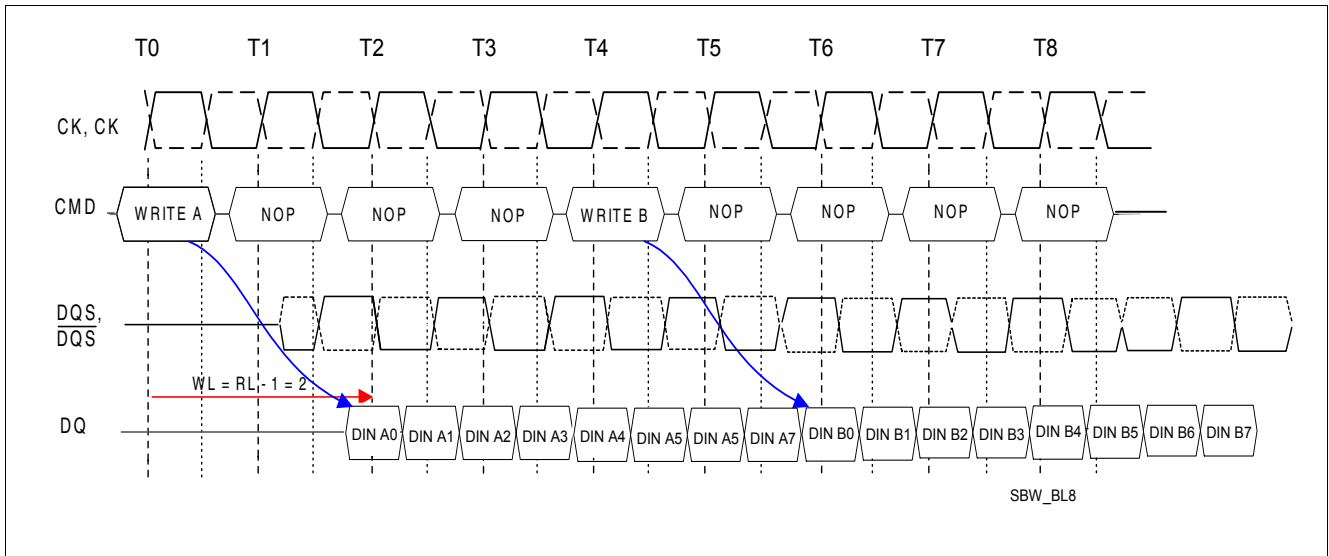


Figure 34 Seamless Write Operation Example 2: $RL = 3$, $WL = 2$, $BL = 8$, non interrupting

The seamless, non interrupting 8-bit burst write operation is supported by enabling a write command at every $BL/2$ number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

2.6.5 Write Data Mask

One write data mask input (DM) for $\times 4$ and $\times 8$ components and two write data mask inputs (LDM, UDM) for $\times 16$ components are supported on DDR2 SDRAM's, consistent with the implementation on DDR SDRAM's. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to

insure matched system timing. Data mask is not used during read cycles. If DM is HIGH during a write burst coincident with the write data, the write data bit is not written to the memory. For $\times 8$ components the DM function is disabled, when $RDQS / \overline{RDQS}$ are enabled by EMRS(1).

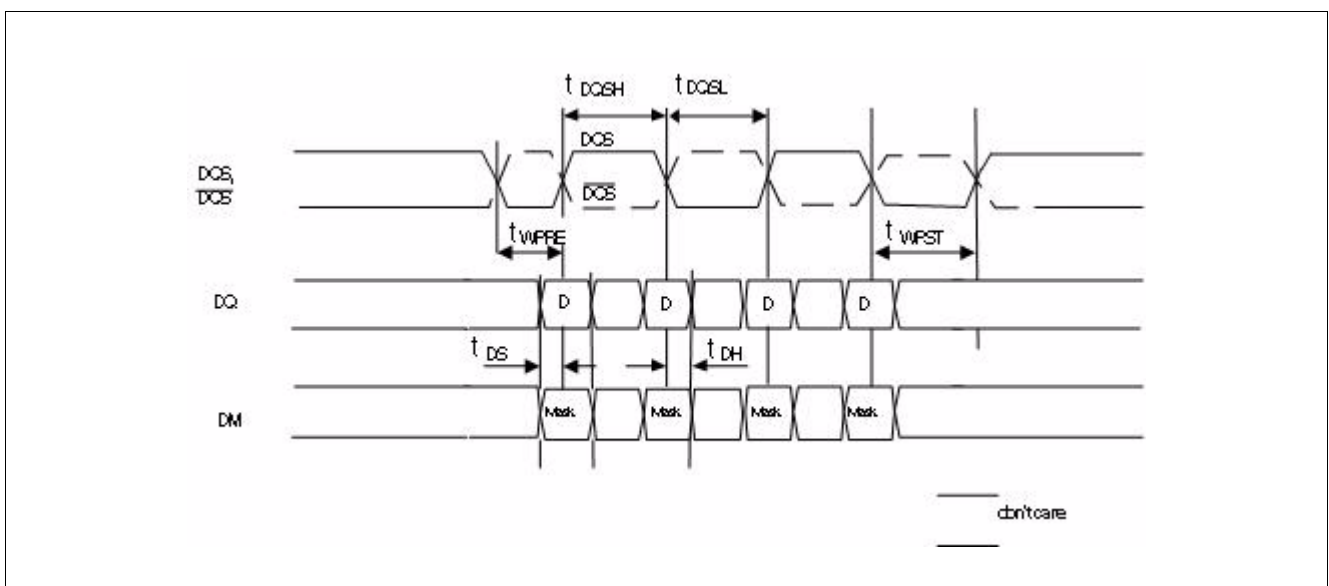


Figure 35 Write Data Mask Timing

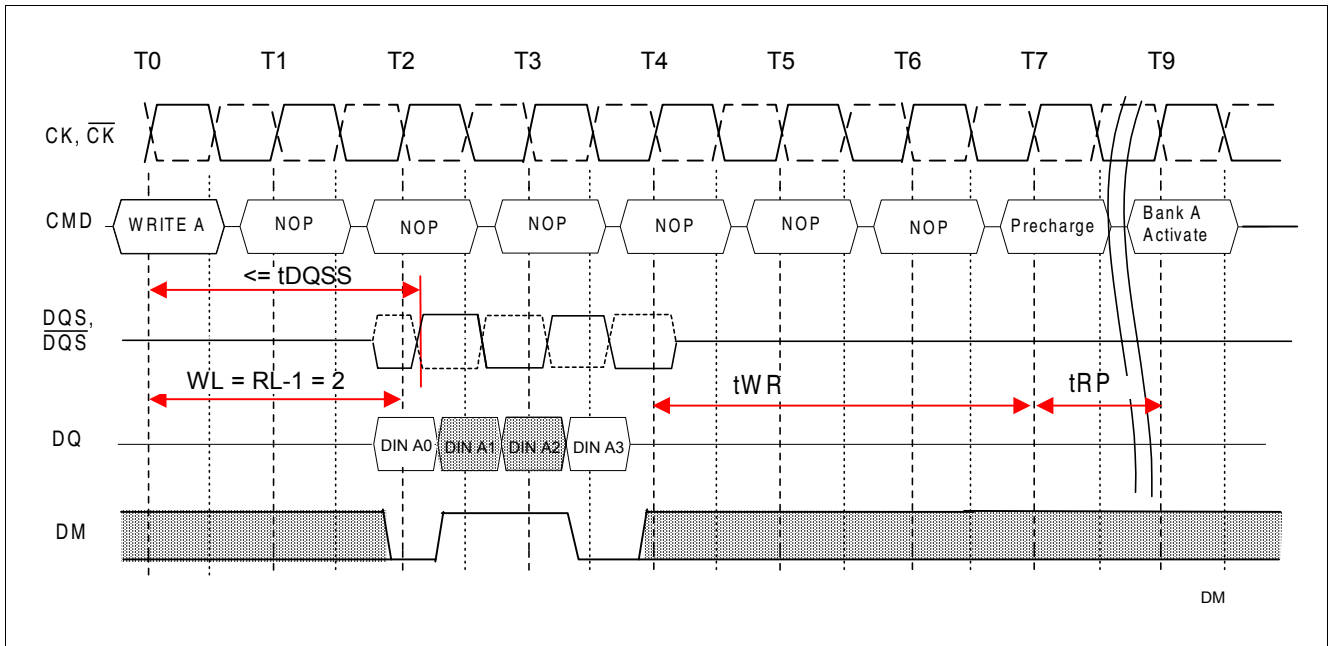


Figure 36 Write Operation with Data Mask Example: $RL = 3$ ($AL = 0$, $CL = 3$), $WL = 2$, $t_{WR} = 3$, $BL = 4$

2.6.6 Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.
2. A Write Burst can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.
7. Read burst interruption is allowed by a Read with Auto-Precharge command.
8. Write burst interruption is allowed by a Write with Auto-Precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is $AL + BL/2$ where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is $WL + BL/2 + t_{WR}$, where t_{WR} starts with the rising clock after the un-interrupted burst end and not from the end of the actual burst end.

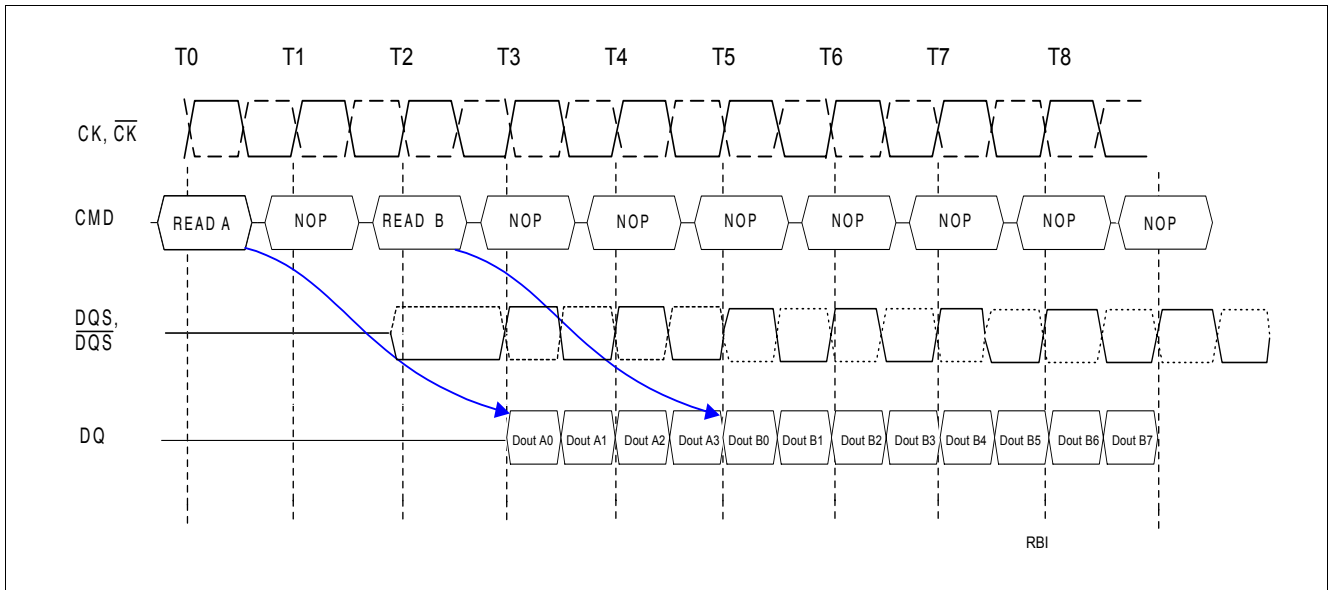


Figure 37 Read Interrupt Timing Example 1: (CL = 3, AL = 0, RL = 3, BL = 8)

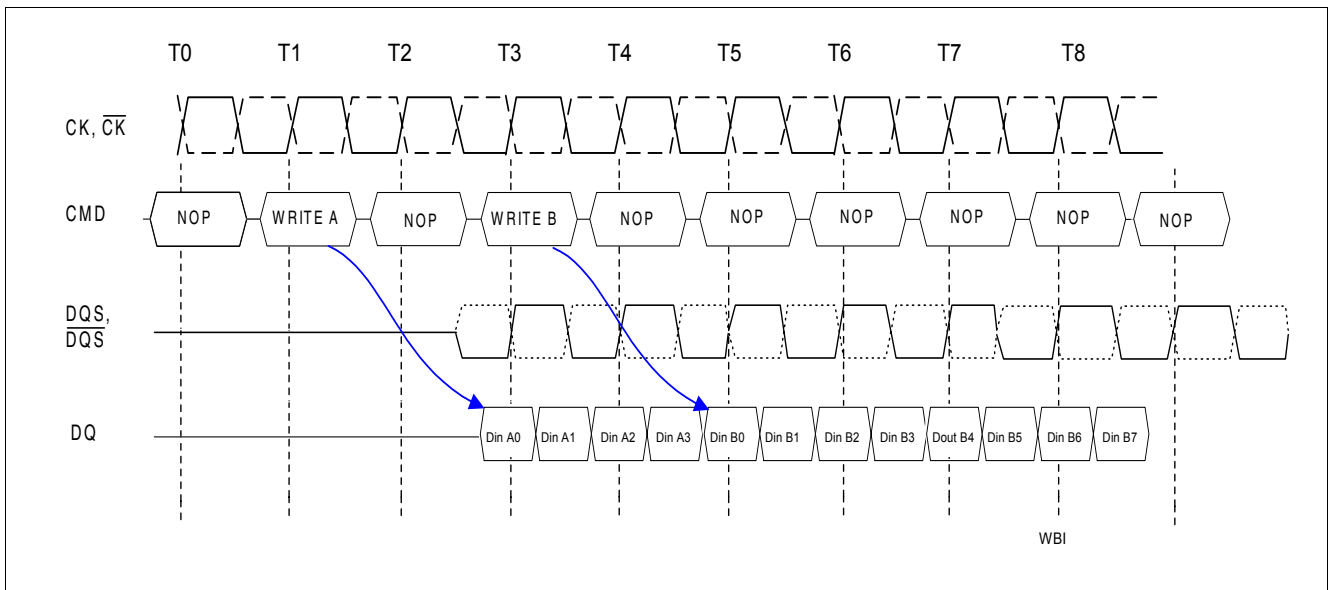


Figure 38 Write Interrupt Timing Example 2: (CL = 3, AL = 0, WL = 2, BL = 8)

2.7 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when \overline{CS} , \overline{RAS} and \overline{WE} are LOW and \overline{CAS} is HIGH at the rising edge of the clock.

The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. 4 address bits A10, BA[2:0] are used to define which bank to precharge when the command is issued.

Table 12 Bank Selection for Precharge by Address Bits

| A10 | BA2 | BA1 | BA0 | Precharge Bank(s) |
|-----|------------|------------|------------|-------------------|
| 0 | 0 | 0 | 0 | Bank 0 only |
| 0 | 0 | 0 | 1 | Bank 1 only |
| 0 | 0 | 1 | 0 | Bank 2 only |
| 0 | 0 | 1 | 1 | Bank 3 only |
| 0 | 1 | 0 | 0 | Bank 4 only |
| 0 | 1 | 0 | 1 | Bank 5 only |
| 0 | 1 | 1 | 0 | Bank 6 only |
| 0 | 1 | 1 | 1 | Bank 7 only |
| 1 | Don't Care | Don't Care | Don't Care | all banks |

Note: The bank address assignment is the same for activating and precharging a specific bank.

2.7.1 Read Operation Followed by a Precharge

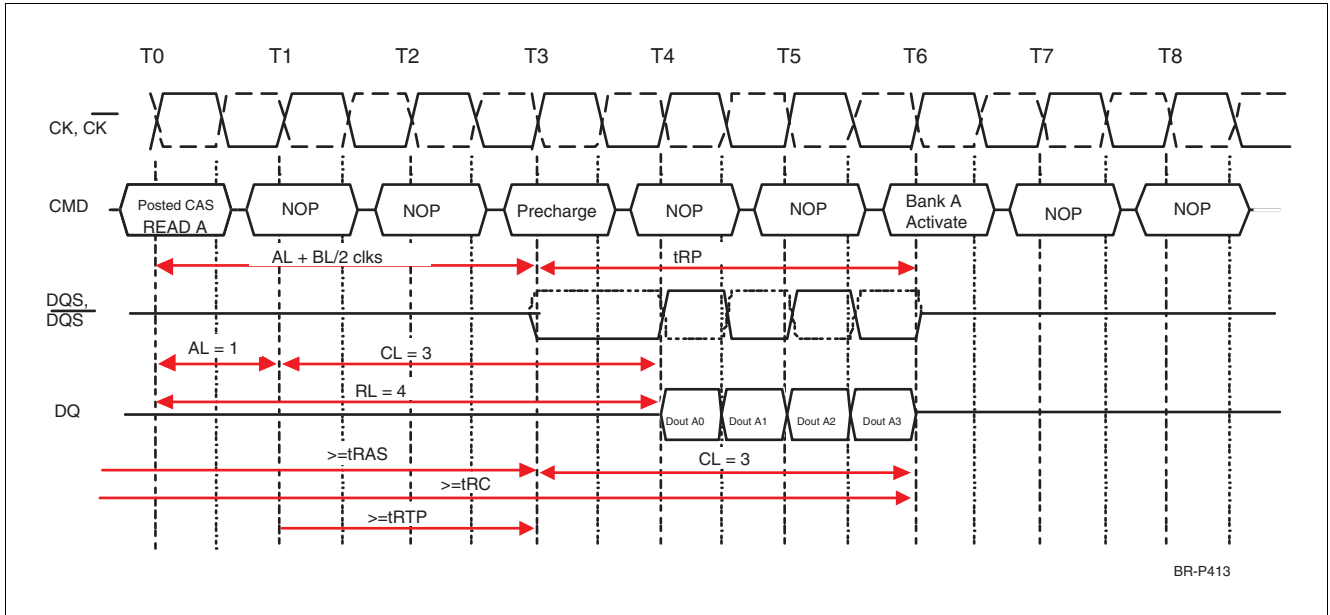
The following rules apply as long as the t_{RTP} timing parameter - Internal Read to Precharge Command delay time - is less or equal two clocks, which is the case for operating frequencies less or equal 266 Mhz (DDR2 400 and 533 speed sorts).

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 clocks. For the earliest possible precharge, the Precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2

clocks" after a Read Command, as long as the minimum t_{RAS} timing is satisfied.

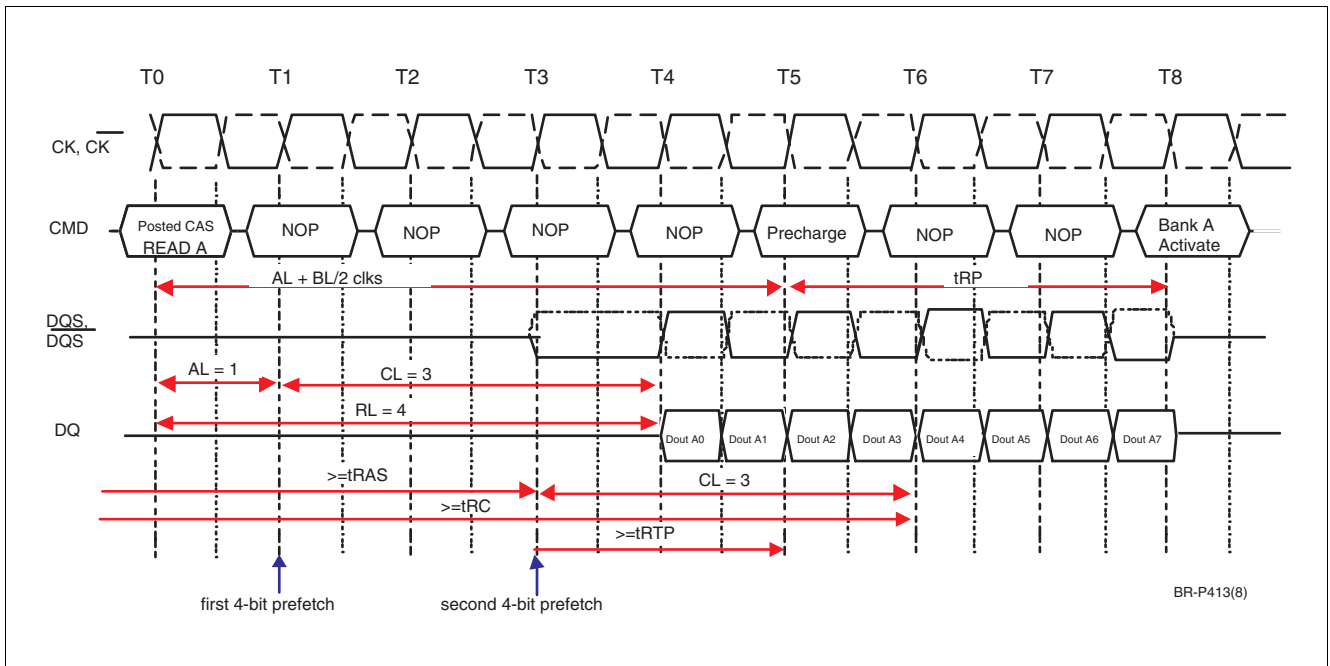
A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The RAS precharge time (t_{RP}) has been satisfied from the clock at which the precharge begins.
2. The RAS cycle time ($t_{RC,min}$) from the previous bank activation has been satisfied.



BR-P413

Figure 39 Read Operation Followed by Precharge Example 1:
RL = 4 (AL = 1, CL = 3), BL = 4, $t_{RTP} \leq 2$ clocks



BR-P413(8)

Figure 40 Read Operation Followed by Precharge Example 2:
RL = 4 (AL = 1, CL = 3), BL = 8, $t_{RTP} \leq 2$ clocks

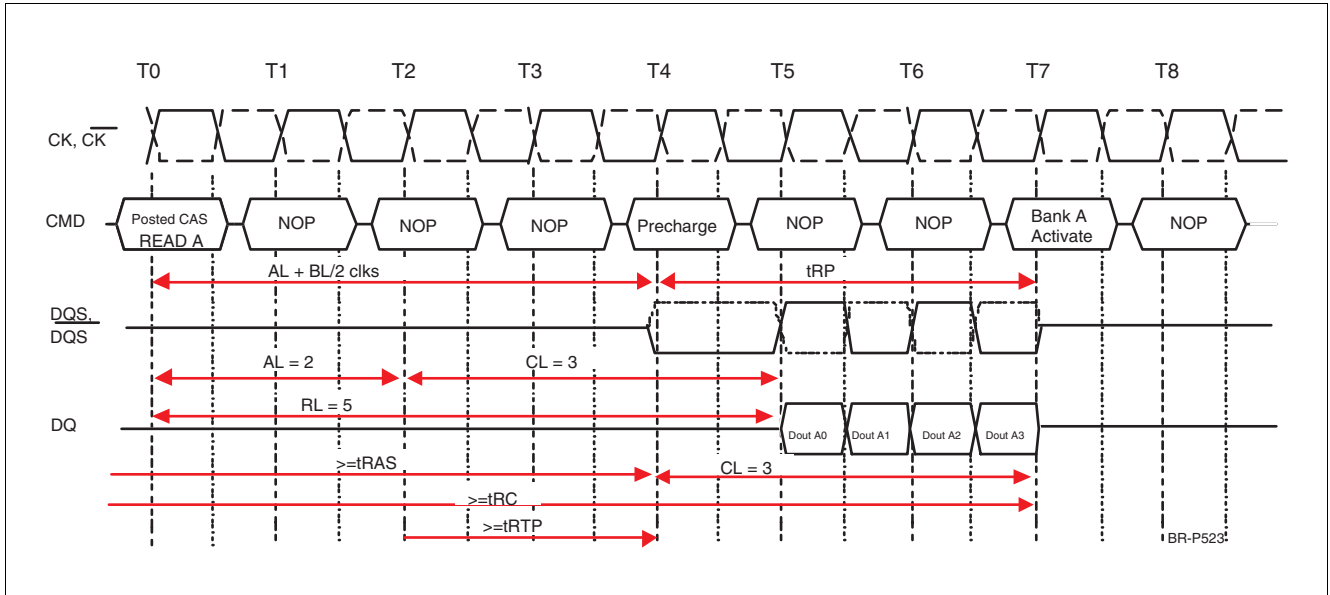


Figure 41 Read Operation Followed by Precharge Example 3:
RL = 5 (AL = 2, CL = 3), BL = 4, $t_{RTP} \leq 2$ clocks

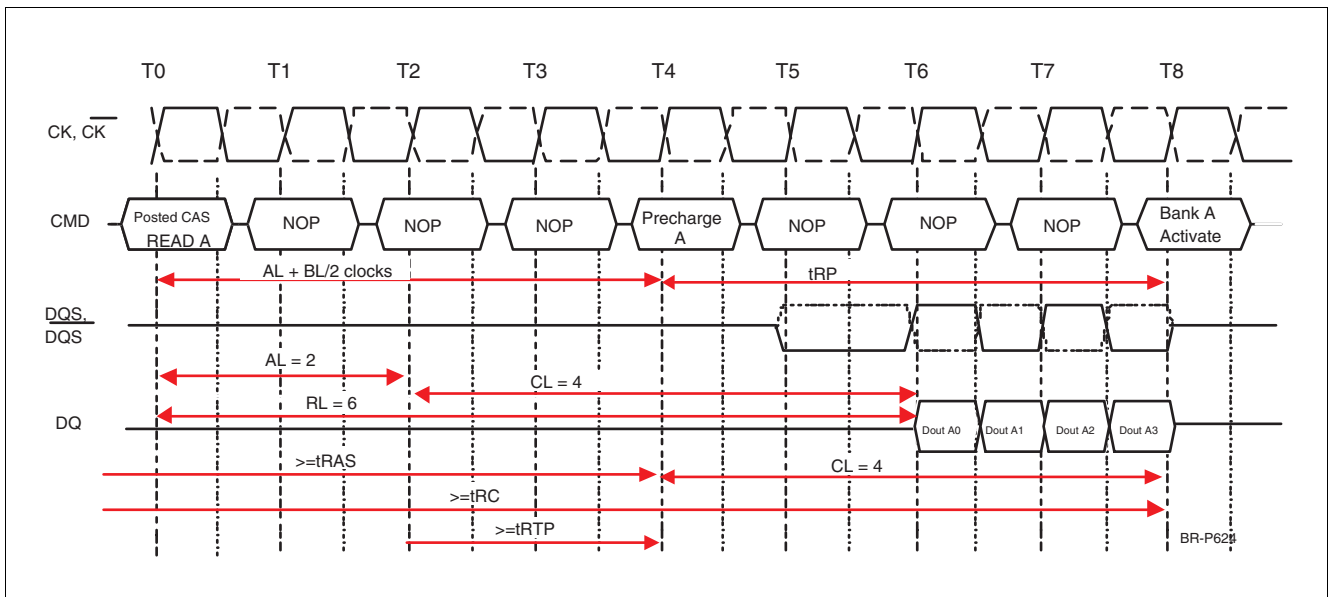


Figure 42 Read Operation Followed by Precharge Example 4:
RL = 6, (AL = 2, CL = 4), BL = 4, $t_{RTP} \leq 2$ clocks

2.7.2 Write followed by Precharge

Minimum Write to Precharge command spacing to the same bank = $WL + BL/2 + t_{WR}$. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write

to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter (see [Chapter 7](#)) and is not the programmed value WR in the MR.

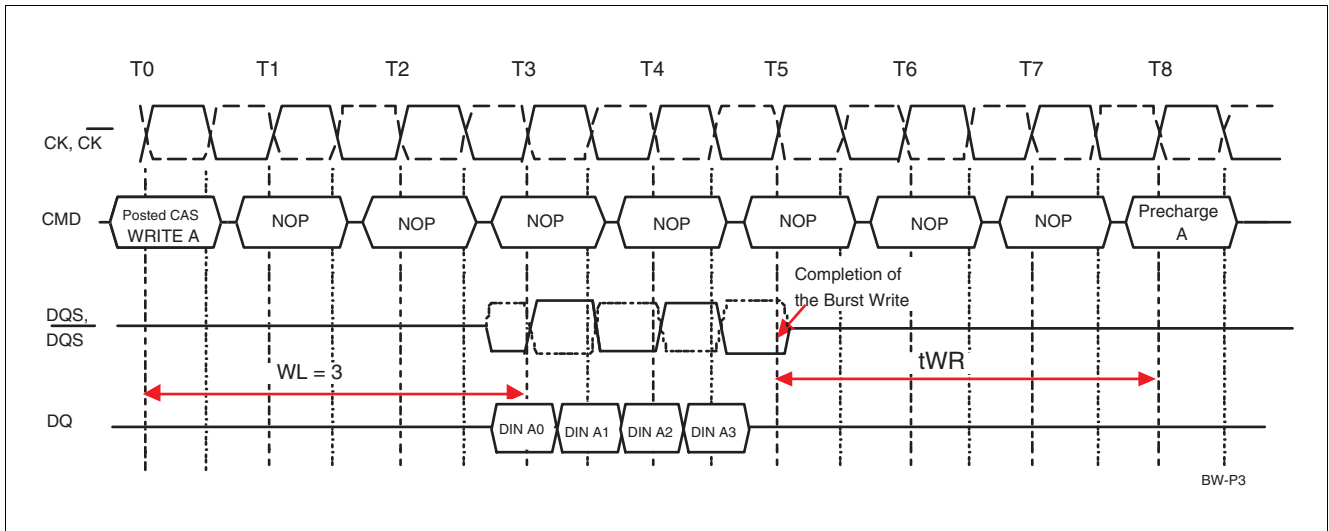


Figure 43 Write followed by Precharge Example 1: $WL = (RL - 1) = 3$, $BL = 4$, $t_{WR} = 3$

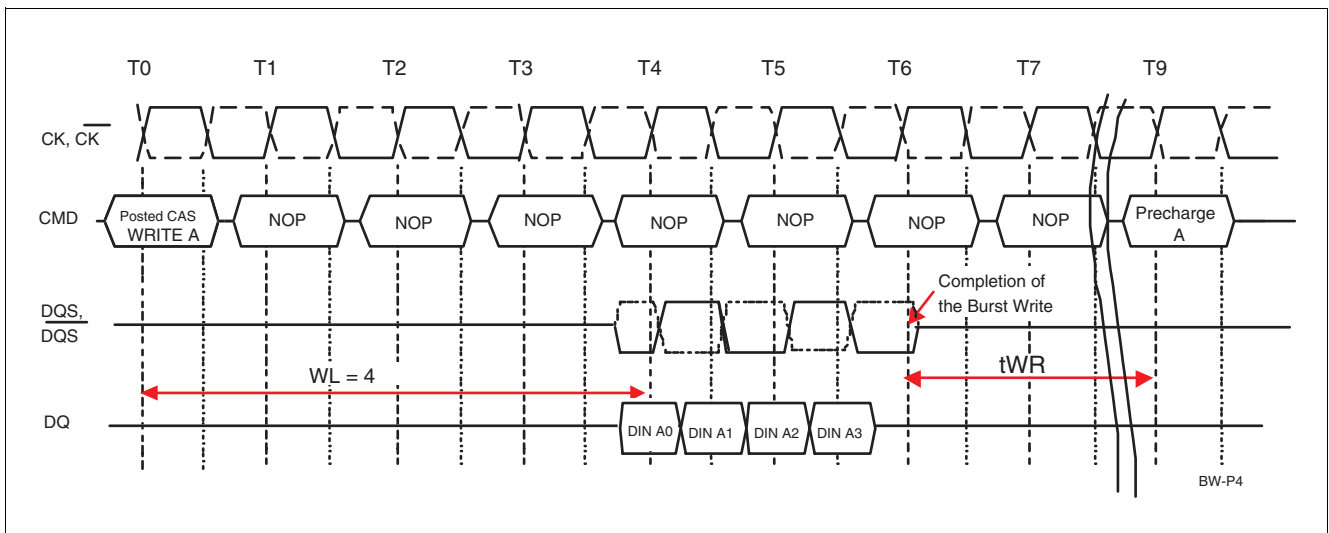


Figure 44 Write followed by Precharge Example 2: $WL = (RL - 1) = 4$, $BL = 4$, $t_{WR} = 3$

2.8 Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{\text{CAS}}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge

internally on the rising edge which is $\overline{\text{CAS}}$ Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands. The Precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{\text{CAS}}$ Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

2.8.1 Read with Auto-Precharge

If A10 is 1 when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is $(\text{AL} + \text{BL}/2)$ cycles later from the Read with AP command if $t_{\text{RAS},\text{min}}$ and t_{RTP} are satisfied. If $t_{\text{RAS},\text{min}}$ is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until $t_{\text{RAS},\text{min}}$ is satisfied. If $t_{\text{RTP},\text{min}}$ is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until $t_{\text{RTP},\text{min}}$ is satisfied.

In case the internal precharge is pushed out by t_{RTP} , t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for $\text{BL} = 4$ the minimum time from Read with Auto-Precharge to the next Activate command

becomes $\text{AL} + t_{\text{RTP}} + t_{\text{RP}}$. For $\text{BL} = 8$ the time from Read with Auto-Precharge to the next Activate command is $\text{AL} + 2 + t_{\text{RTP}} + t_{\text{RP}}$. Note that $(t_{\text{RTP}} + t_{\text{RP}})$ has to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The $\overline{\text{RAS}}$ precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.
2. The $\overline{\text{RAS}}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

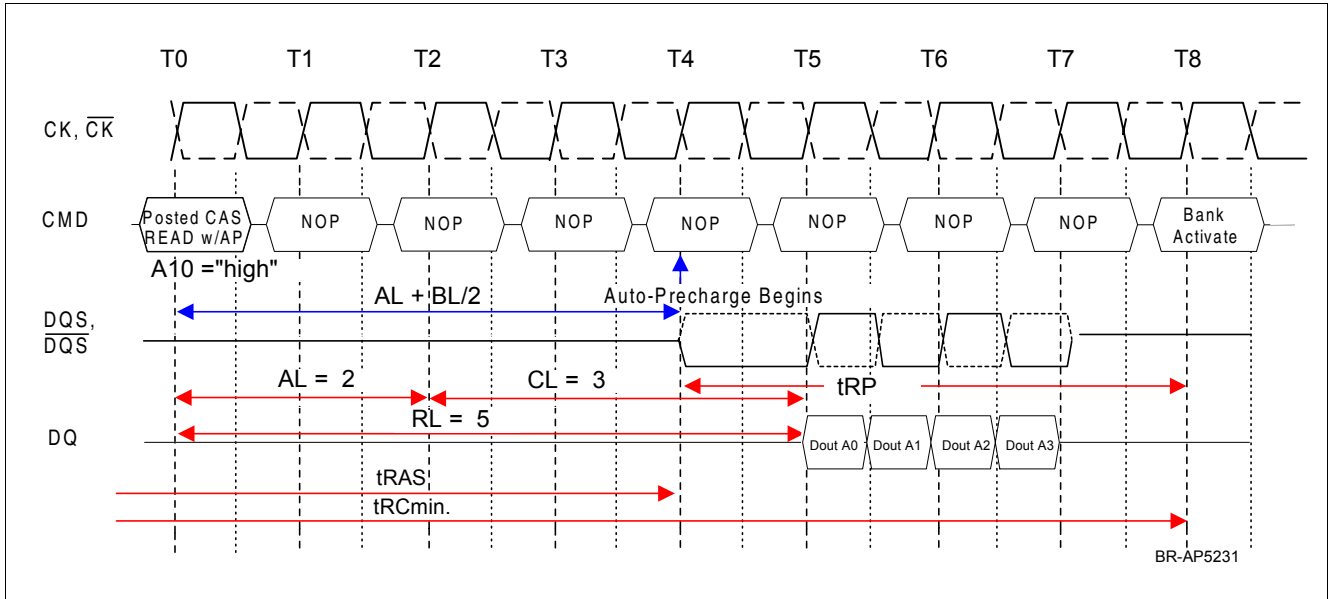


Figure 45 Read with Auto-Precharge Example 1, followed by an Activation to the Same Bank (t_{RC} Limit):
RL = 5 (AL = 2, CL = 3), BL = 4, $t_{RTP} \leq 2$ clocks

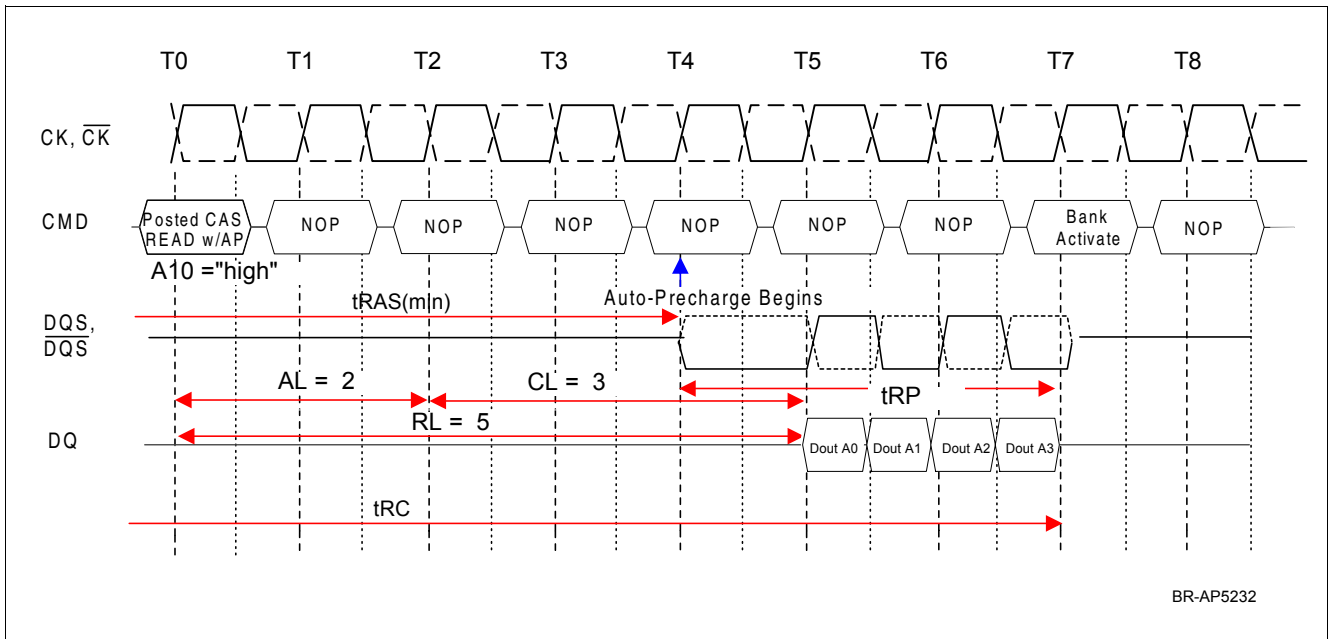


Figure 46 Read with Auto-Precharge Example 2, followed by an Activation to the Same Bank (t_{RAS} Limit):
RL = 5 (AL = 2, CL = 3), BL = 4, $t_{RTP} \leq 2$ clocks

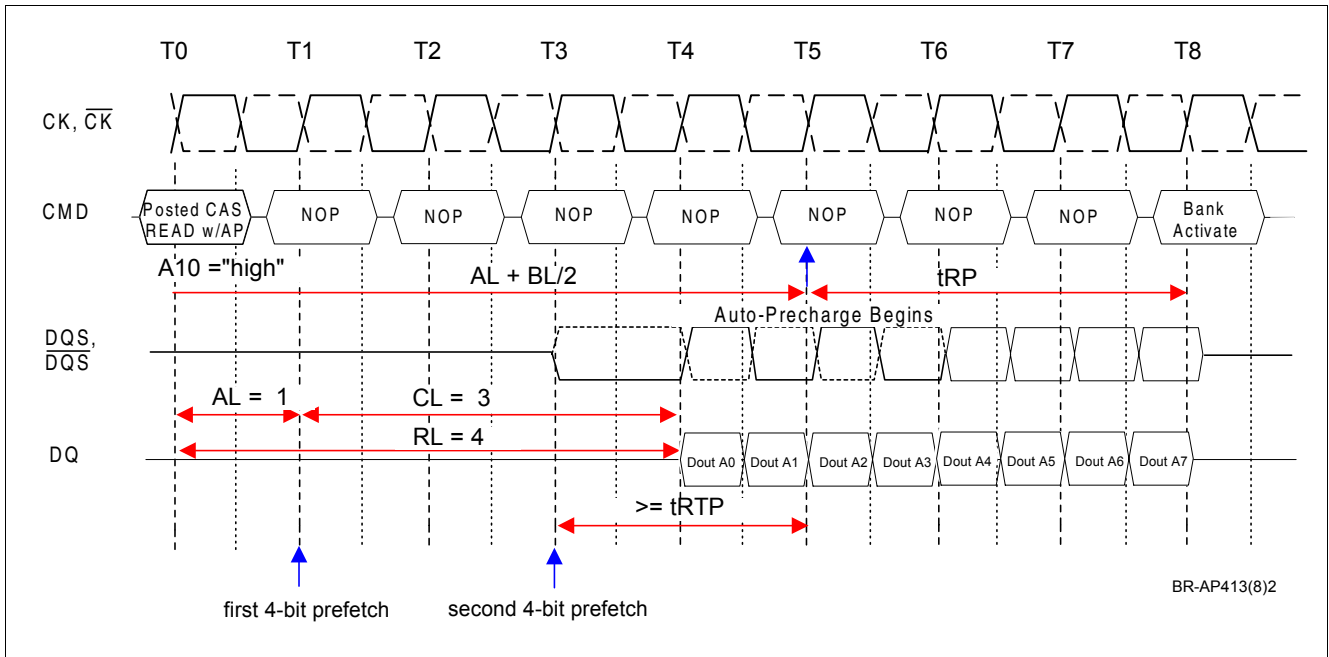


Figure 47 Read with Auto-Precharge Example 3, followed by an Activation to the Same Bank:
RL = 4 (AL = 1, CL = 3), BL = 8, $t_{RTP} \leq 2$ clocks

2.8.2 Write with Auto-Precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as t_{RAS} is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

1. The last data-in to bank activate delay time ($t_{DAL} = WR + t_{RP}$) has been satisfied.
2. The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

In DDR2 SDRAM's the write recovery time delay (WR) has to be programmed into the MRS mode register. As long as the analog t_{WR} timing parameter is not violated, WR can be programmed between 2 and 6 clock cycles. Minimum Write to Activate command spacing to the same bank = $WL + BL/2 + t_{DAL}$.

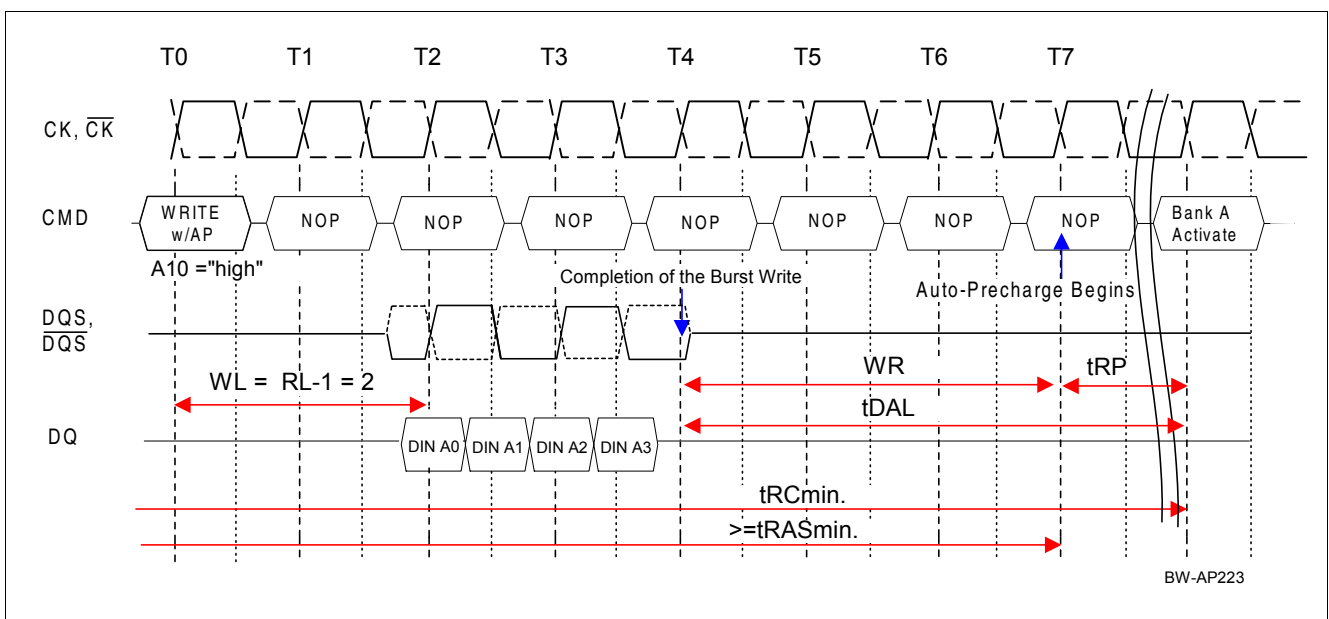


Figure 48 Write with Auto-Precharge Example 1 (t_{RC} Limit): $WL = 2$, $t_{DAL} = 6$ ($WR = 3$, $t_{RP} = 3$), $BL = 4$

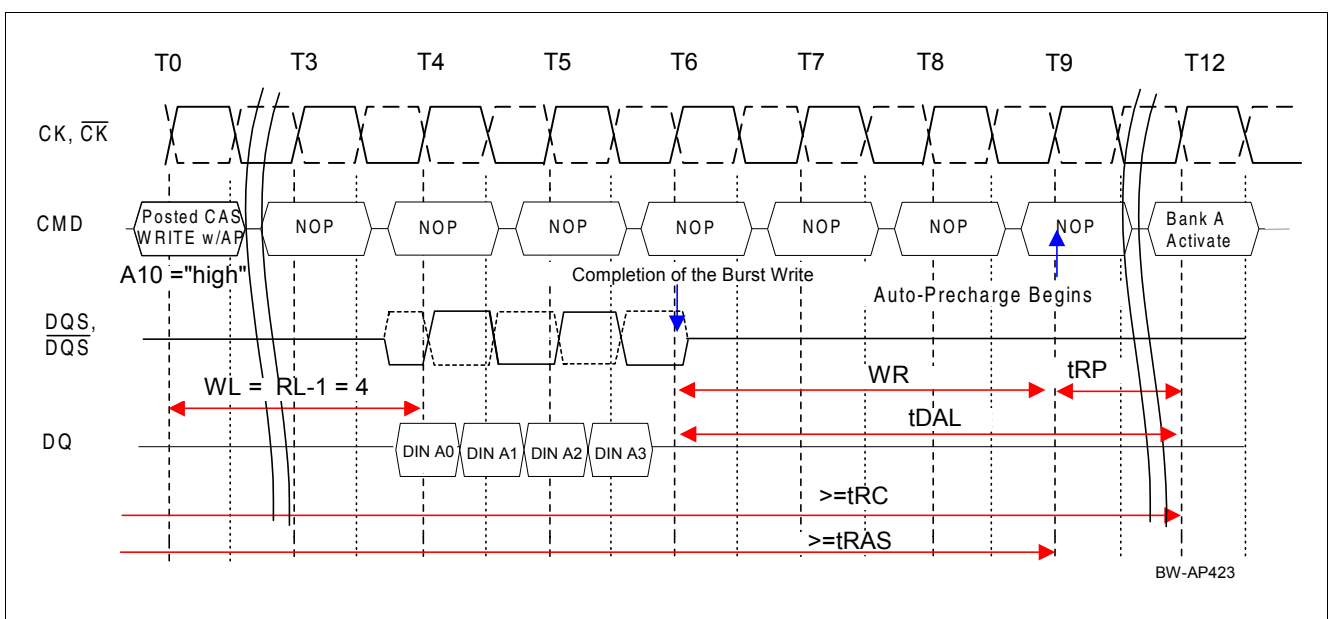


Figure 49 Write with Auto-Precharge Example 2 ($WR + t_{RP}$ Limit): $WL = 4$, $t_{DAL} = 6$ ($WR = 3$, $t_{RP} = 3$), $BL = 4$

2.8.3 Read or Write to Precharge Command Spacing Summary

The following table summarizes the minimum command delays between Read, Read w/AP, Write, Write w/AP to the Precharge commands to the same banks and Precharge-All commands.

Table 13 Minimum Command Delays

| From Command | To Command | Minimum Delay between “From Command” to “To Command” | Unit | Note |
|---------------|---|--|----------|------|
| READ | PRECHARGE (to same banks as READ) | $AL + BL/2 + \max(t_{RTP}, 2) - 2 \times t_{CK}$ | t_{CK} | 1)2) |
| | PRECHARGE-ALL | $AL + BL/2 + \max(t_{RTP}, 2) - 2 \times t_{CK}$ | t_{CK} | 1)2) |
| READ w/AP | PRECHARGE (to same banks as READ w/AP) | $AL + BL/2 + \max(t_{RTP}, 2) - 2 \times t_{CK}$ | t_{CK} | 1)2) |
| | PRECHARGE-ALL | $AL + BL/2 + \max(t_{RTP}, 2) - 2 \times t_{CK}$ | t_{CK} | 1)2) |
| WRITE | PRECHARGE (to same banks as WRITE) | $WL + BL/2 + t_{WR}$ | t_{CK} | 2)3) |
| | PRECHARGE-ALL | $WL + BL/2 + t_{WR}$ | t_{CK} | 2)3) |
| WRITE w/AP | PRECHARGE (to same banks as WRITE w/AP) | $WL + BL/2 + WR$ | t_{CK} | 2) |
| | PRECHARGE-ALL | $WL + BL/2 + WR$ | t_{CK} | 2) |
| PRECHARGE | PRECHARGE (to same banks as PRECHARGE) | 1 | t_{CK} | 2) |
| | PRECHARGE-ALL | 1 | t_{CK} | 2) |
| PRECHARGE-ALL | PRECHARGE | 1 | t_{CK} | 2) |
| | PRECHARGE-ALL | 1 | t_{CK} | 2) |

- 1) $RU\{t_{RTP}(ns) / t_{CK}(ns)\}$ must be used, where RU stands for “Round Up”
- 2) For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge-all, issued to that bank. The precharge period is satisfied after t_{RP} or t_{RPA} depending on the latest precharge command issued to that bank
- 3) $RU\{t_{WR}(ns) / t_{CK}(ns)\}$ must be used, where RU stands for “Round Up”

2.8.4 Concurrent Auto-Precharge

DDR2 devices support the “Concurrent Auto-Precharge” feature. A Read with Auto-Precharge enabled, or a Write with Auto-Precharge enabled, may be followed by any command to the other bank, as long as that command does not interrupt the read or write data transfer, and all other related limitations (e.g. contention between Read data and Write data must be avoided externally and on the internal data bus).

The minimum delay from a Read or Write command with Auto-Precharge enabled, to a command to a different bank, is summarized in **Table 14**. As defined, the $WL = RL - 1$ for DDR2 devices which allows the command gap and corresponding data gaps to be minimized.

Table 14 Command Delay Table

| From Command | To Command (different bank, non-interrupting command) | Minimum Delay with Concurrent Auto-Precharge Support | Unit | Note |
|--------------|---|--|----------|------|
| WRITE w/AP | Read or Read w/AP | $(CL - 1) + (BL/2) + t_{WTR}$ | t_{CK} | 1) |
| | Write or Write w/AP | $BL/2$ | t_{CK} | |
| | Precharge or Activate | 1 | t_{CK} | 2) |
| Read w/AP | Read or Read w/AP | $BL/2$ | t_{CK} | |
| | Write or Write w/AP | $BL/2 + 2$ | t_{CK} | |
| | Precharge or Activate | 1 | t_{CK} | 2) |

1) $RU\{t_{WTR}(ns)/t_{CK}(ns)\}$ must be used where RU stands for “Round Up”

2) This rule only applies to a selective Precharge command to another bank, a Precharge-All command is illegal

2.9 Refresh

DDR2 SDRAM requires a refresh of all rows in any rolling 64 ms interval. The necessary refresh can be generated in one of two ways: by explicit Auto-Refresh commands or by an internally timed Self-Refresh mode.

2.9.1 Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAM's. This command is non persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits “don't care” during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of $t_{REFI(maximum)}$.

When \overline{CS} , \overline{RAS} and \overline{CAS} are held LOW and \overline{WE} HIGH at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the

external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is $9 \times t_{REFI}$.

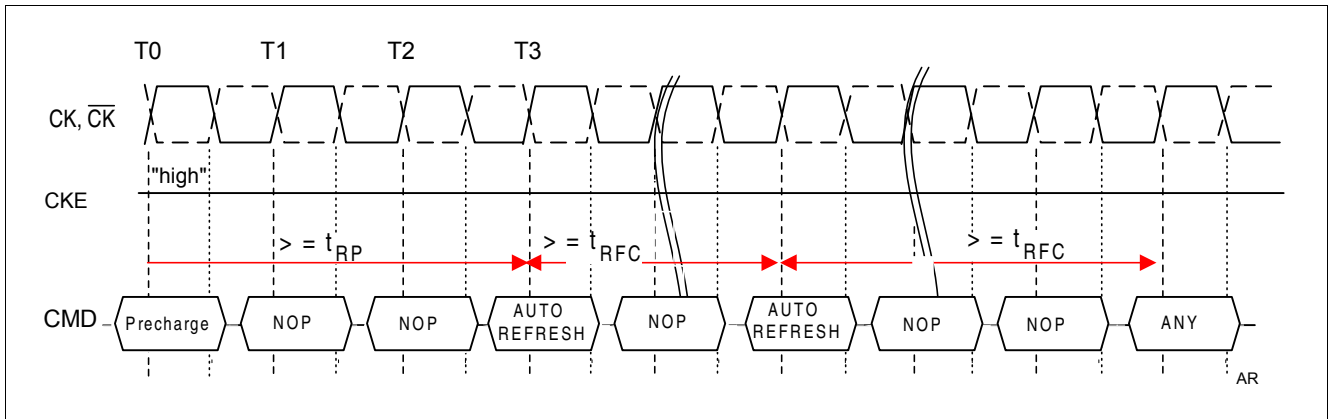


Figure 50 Auto Refresh Timing

2.9.2 Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having \overline{CS} , \overline{RAS} , \overline{CAS} and CKE held LOW with \overline{WE} HIGH at the rising edge of the clock. The device must be in idle state and ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using EMRS(1) command. Once the command is registered, CKE must be held LOW to keep the device in Self-Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are “don’t care”. The DRAM initiates a minimum of one Auto Refresh command internally within t_{CKE} period once it enters Self Refresh mode. The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR2 SDRAM must remain in Self Refresh mode is t_{CKE} . The user may change the external clock frequency or halt the external clock one

clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self-Refresh Exit command is registered, a delay of at least t_{XSNR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self-Refresh exit period t_{XSRD} for proper operation. Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after t_{XSNR} expires. NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval t_{XSNR} . ODT should be turned off during t_{XSNR} .

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh Mode.

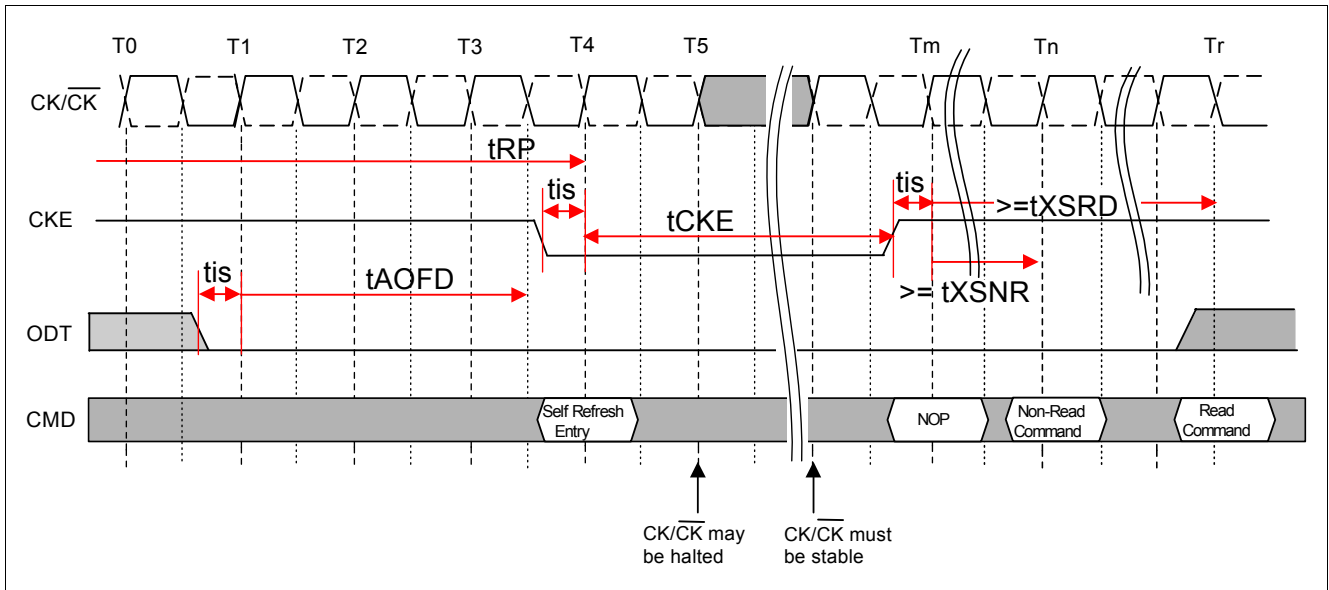


Figure 51 Self Refresh Timing

Note

1. Device must be in the “All banks idle” state before entering Self Refresh mode.
2. $t_{XSRD} (\geq 200 t_{CK})$ has to be satisfied for a Read or a Read with Auto-Precharge command.
3. t_{XSNR} has to be satisfied for any command except a Read or a Read with Auto-Precharge command
4. Since CKE is an SSTL input, V_{REF} must be maintained during Self Refresh.

2.10 Power-Down

Power-down is synchronously entered when CKE is registered LOW, along with NOP or Deselect command. CKE is not allowed to go LOW while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go LOW while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down I_{DD} specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation. DRAM design guarantees it's DLL in a locked state with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

If power-down occurs when all banks are precharged, this mode is referred to as Precharge Power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as Active Power-down. For Active Power-down two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to LOW this mode is

referred as “standard active power-down mode” and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to HIGH this mode is referred as a power saving “low power active power-down mode”. This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied.

Entering power-down deactivates the input and output buffers, excluding CK, \overline{CK} , ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are “Don't Care”. Power-down duration is limited by 9 times t_{REF1} of the device.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP} , t_{XARD} or t_{XARDS} , after CKE goes HIGH. Power-down exit latencies are defined in [Table 42](#).

Power-Down Entry

Active Power-down mode can be entered after an Activate command. Precharge Power-down mode can be entered after a Precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when t_{MRD} is satisfied.

Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept HIGH until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after $RL + BL/2$ is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed when $WL + BL/2 + t_{WTR}$ is satisfied.

In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which is $WL + BL/2 + WR$ starting from the write with Auto-Precharge command. In this case the DDR2 SDRAM enters the Precharge Power-down mode.

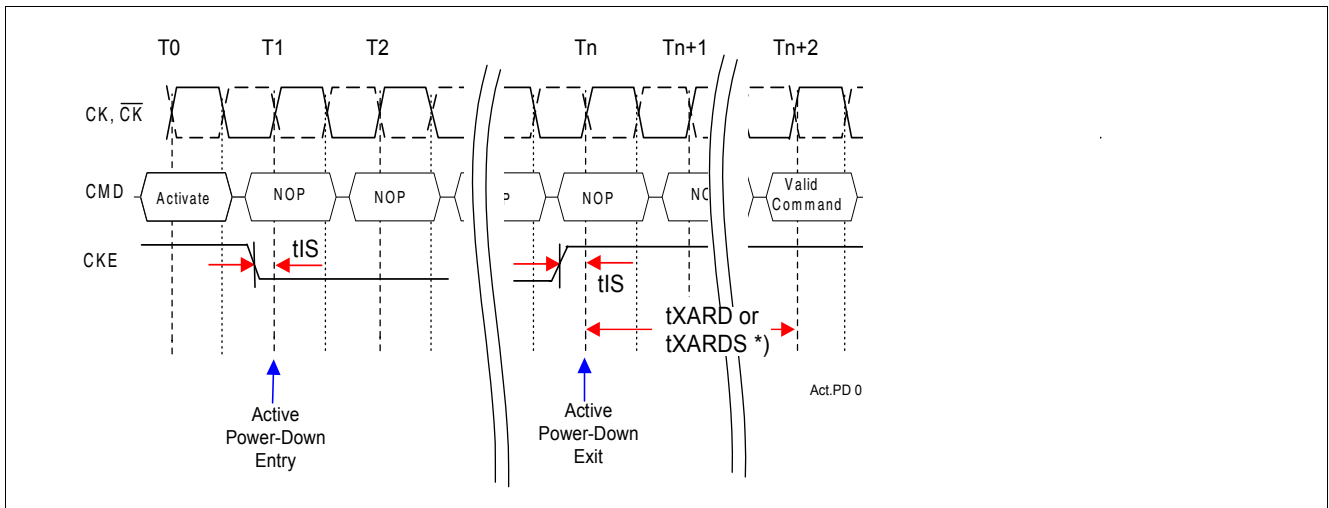


Figure 52 Active Power-Down Mode Entry and Exit after an Activate Command

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

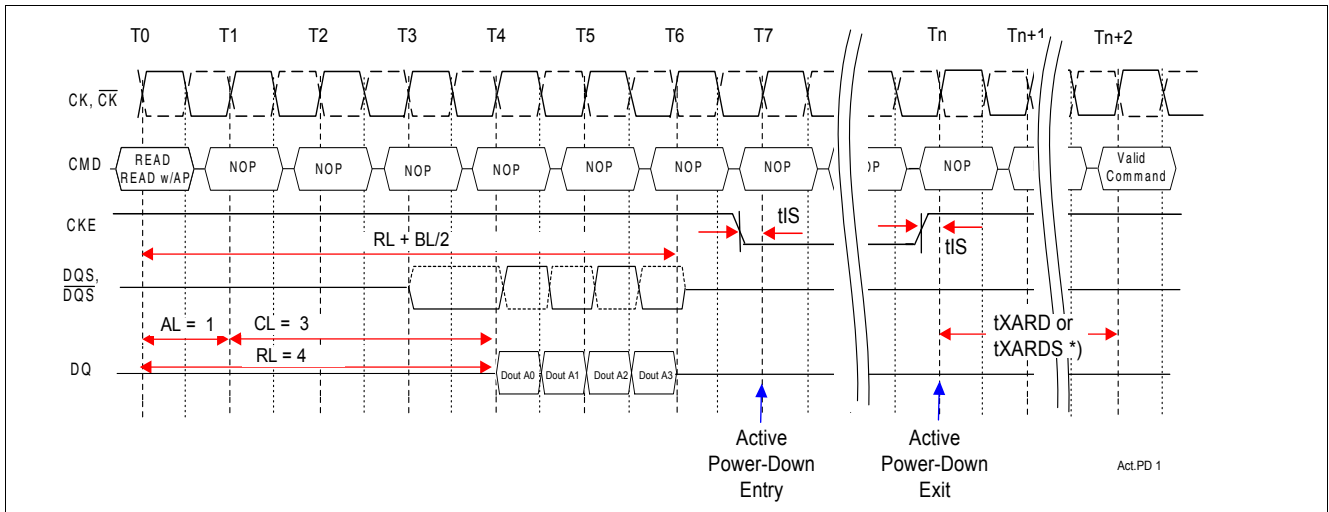


Figure 53 Active Power-Down Mode Entry and Exit Example after a Read Command:
RL = 4 (AL = 1, CL = 3), BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

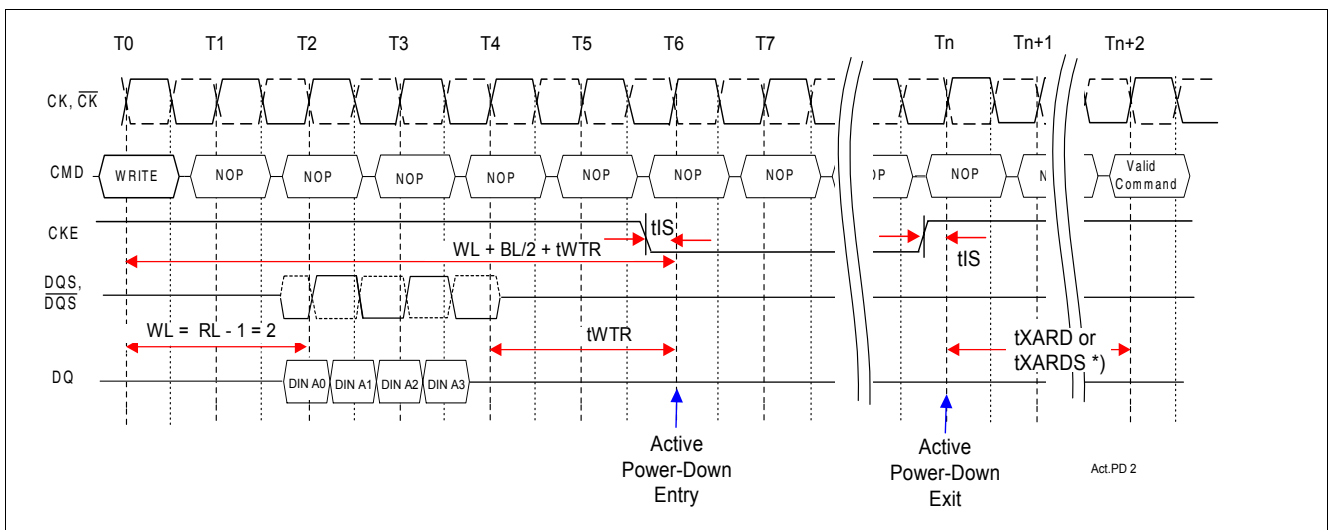


Figure 54 Active Power-Down Mode Entry and Exit Example after a Write Command:
WL = 2, $t_{WTR} = 2$, BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12.

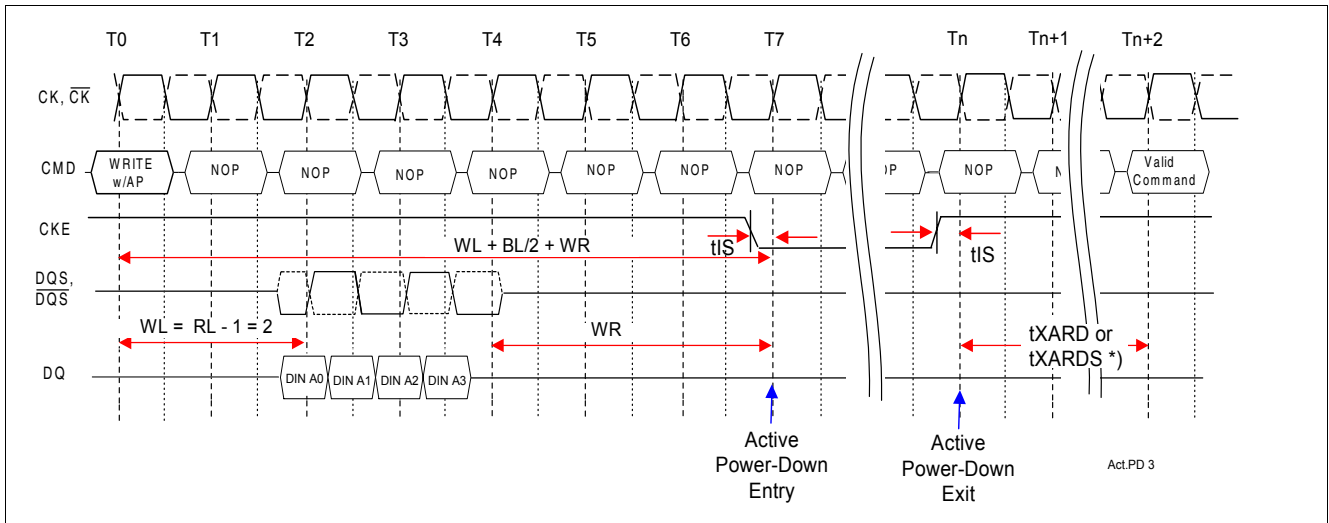


Figure 55 Active Power-Down Mode Entry and Exit Example after a Write Command with AP:
WL = 2, WR = 3, BL = 4

Note: Active Power-Down mode exit timing t_{XARD} ("fast exit") or t_{XARDS} ("slow exit") depends on the programmed state in the MR, address bit A12. WR is the programmed value in the MRS mode register.

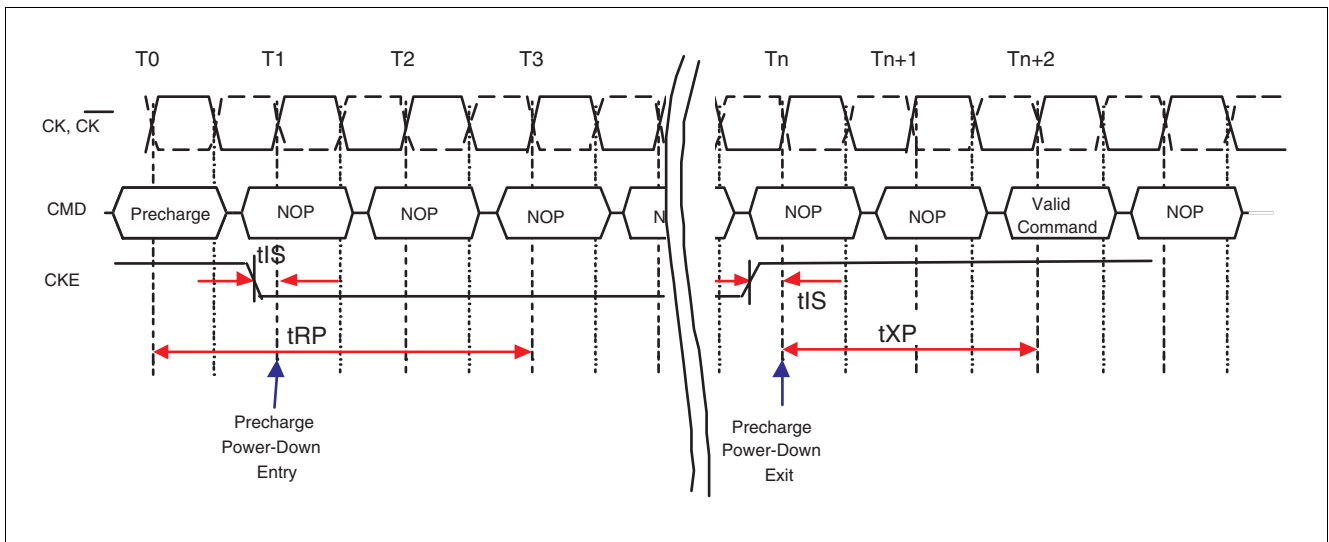


Figure 56 Precharge Power Down Mode Entry and Exit

Note: "Precharge" may be an external command or an internal precharge following Write with AP.

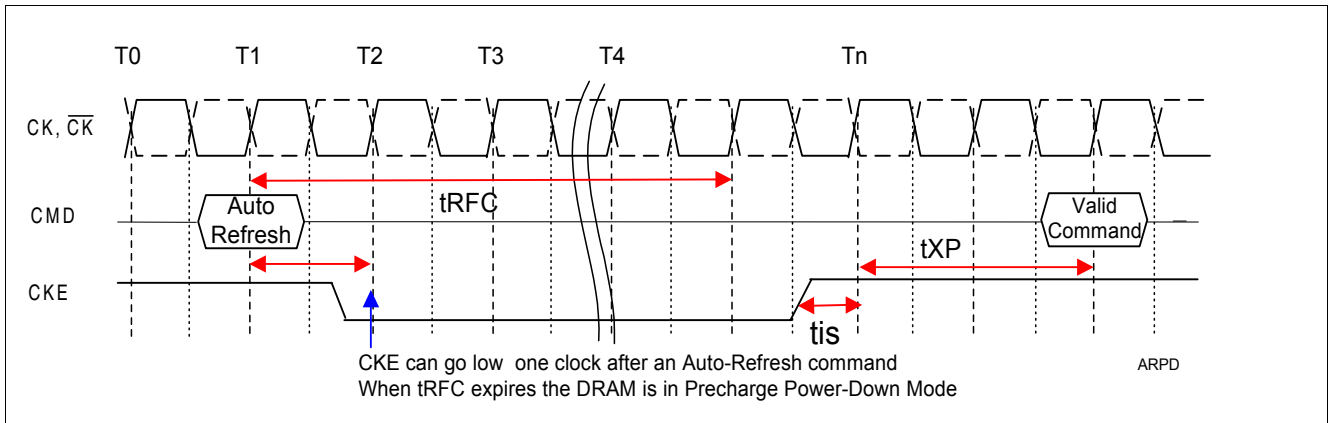


Figure 57 Auto-Refresh command to Power-Down entry

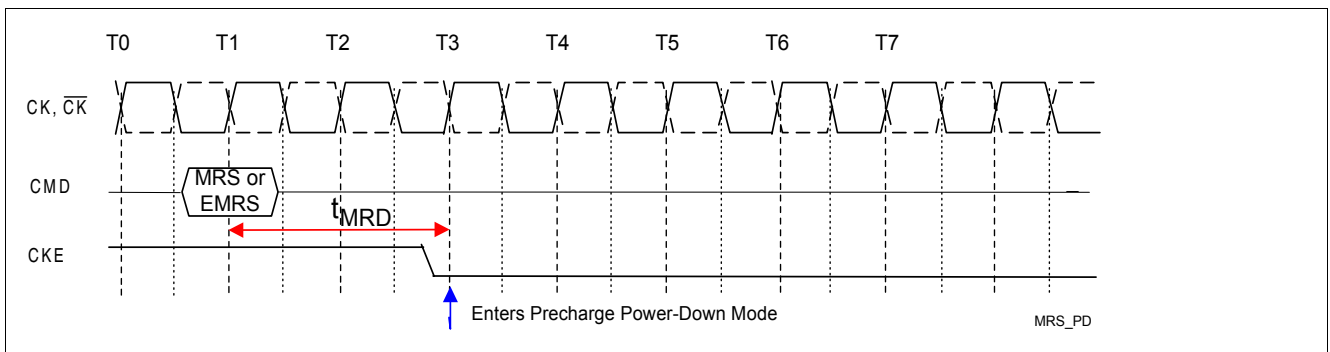


Figure 58 MRS, EMRS command to Power-Down entry

2.11 Other Commands

2.11.1 No Operation Command

The No Operation Command (NOP) should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is

registered when \overline{CS} is LOW with \overline{RAS} , \overline{CAS} , and \overline{WE} held HIGH at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

2.11.2 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs

when \overline{CS} is brought HIGH, the \overline{RAS} , \overline{CAS} , and \overline{WE} signals become don't care.

2.12 Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

- During Self-Refresh operation
- DRAM is in Precharge Power-down mode and ODT is completely turned off.

In the latter case the DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be already turned off and CKE must be at a logic LOW state. After a minimum of two clock cycles after t_{RP} and

t_{AOFD} have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a HIGH logic level again. After t_{XP} has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

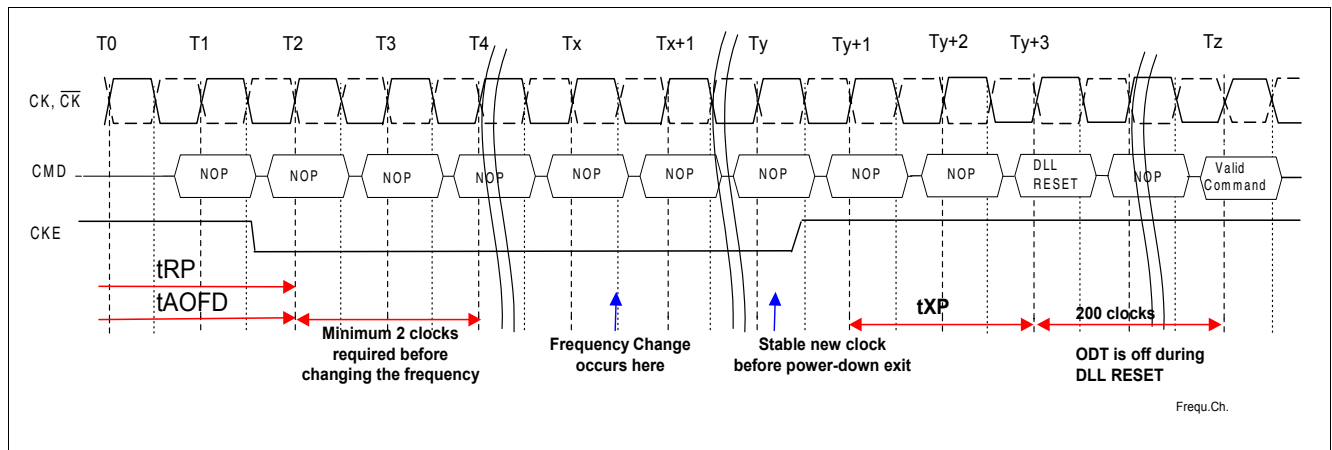


Figure 59 Input Frequency Change Example during Precharge Power-Down mode

2.13 Asynchronous CKE LOW Reset Event

In a given system, Asynchronous Reset event can occur at any time without prior knowledge. In this situation, memory controller is forced to drop CKE asynchronously LOW, immediately interrupting any valid operation. DRAM requires CKE to be maintained HIGH for all valid operations as defined in this data sheet. If CKE asynchronously drops LOW during any valid operation, the DRAM is not guaranteed to preserve the contents of the memory array. If this event

occurs, the memory controller must satisfy a time delay (t_{DELAY}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised HIGH again. The DRAM must be fully re-initialized as described the initialization sequence (Chapter 2.2.1, step 4 through 13). DRAM is ready for normal operation after the initialization sequence. See Chapter 7 for t_{DELAY} specification.

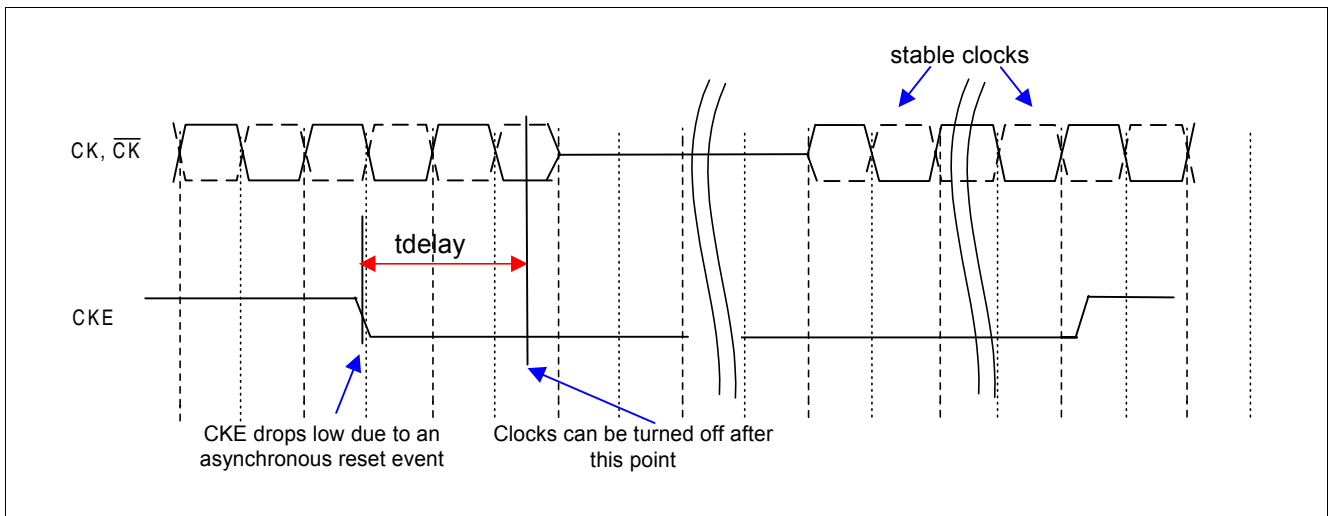


Figure 60 Asynchronous Low Reset Event

3 Truth Tables

Table 15 Command Truth Table

| Function | CKE | | \overline{CS} | RAS | \overline{CAS} | \overline{WE} | BA0 BA1 BA2 | A[13:11] | A10 | A[9:0] | Note ¹⁾²⁾³⁾ |
|------------------------------|----------------|---------------|-----------------|-----|------------------|-----------------|-------------------|-------------|-----|--------|------------------------|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| (Extended) Mode Register Set | H | H | L | L | L | L | BA | OP Code | | | 4)5) |
| Auto-Refresh | H | H | L | L | L | H | X | X | X | X | 4) |
| Self-Refresh Entry | H | L | L | L | L | H | X | X | X | X | 4)6) |
| Self-Refresh Exit | L | H | H | X | X | X | X | X | X | X | 4)6)7) |
| | | | L | H | H | H | | | | | |
| Single Bank Precharge | H | H | L | L | H | L | BA | X | L | X | 4)5) |
| Precharge all Banks | H | H | L | L | H | L | X | X | H | X | 4) |
| Bank Activate | H | H | L | L | H | H | BA | Row Address | | | 4)5) |
| Write | H | H | L | H | L | L | BA | Column | L | Column | 4)5)8) |
| Write with Auto-Precharge | H | H | L | H | L | L | BA | Column | H | Column | 4)5)8) |
| Read | H | H | L | H | L | H | BA | Column | L | Column | 4)5)8) |
| Read with Auto-Precharge | H | H | L | H | L | H | BA | Column | H | Column | 4)5)8) |
| No Operation | H | X | L | H | H | H | X | X | X | X | 4) |
| Device Deselect | H | X | H | X | X | X | X | X | X | X | 4) |
| Power Down Entry | H | L | H | X | X | X | X | X | X | X | 4)9) |
| | | | L | H | H | H | | | | | |
| Power Down Exit | L | H | H | X | X | X | X | X | X | X | 4)9) |
| | | | L | H | H | H | | | | | |

- 1) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 2) "X" means "H or L (but a defined logic level)".
- 3) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) All DDR2 SDRAM commands are defined by states of \overline{CS} , \overline{WE} , RAS, \overline{CAS} , and CKE at the rising edge of the clock.
- 5) Bank addresses (BAx) determine which bank is to be operated upon. For (E)MRS BAx selects an (Extended) Mode Register.
- 6) V_{REF} must be maintained during Self Refresh operation.
- 7) Self Refresh Exit is asynchronous.
- 8) Burst reads or writes at BL = 4 cannot be terminated. See [Chapter 2.6.6](#) for details.
- 9) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in [Chapter 2.7](#)

Table 16 Clock Enable (CKE) Truth Table for Synchronous Transitions

| Current State ¹⁾ | CKE | | Command (N) ^{2) 3)} $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}, \overline{\text{CS}}$ | Action (N) ²⁾ | Note ⁴⁾⁵⁾ |
|---|---------------------------------------|------------------------------------|--|-------------------------------|----------------------|
| | Previous Cycle ⁶⁾ (N-1) | Current Cycle ⁶⁾ (N) | | | |
| Power-Down | L | L | X | Maintain Power-Down | 7)8)11) |
| | L | H | DESELECT or NOP | Power-Down Exit | 7)9)10)11) |
| Self Refresh | L | L | X | Maintain Self Refresh | 8)11) |
| | L | H | DESELECT or NOP | Self Refresh Exit | 9)12)13) |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power-Down Entry | 7)9)10)11)14) |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power-Down Entry | 9)10)11)14) |
| | H | L | AUTOREFRESH | Self Refresh Entry | 7)11)13)15) |
| Any State other than listed above | H | H | Refer to the Command Truth Table | | 16) |

- 1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
- 2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
- 3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See [Chapter 2.4](#).
- 4) CKE must be maintained HIGH while the device is in OCD calibration mode.
- 5) V_{REF} must be maintained during Self Refresh operation.
- 6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- 7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
- 8) "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).
- 9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
- 11) t_{CKEmin} of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CKE} + t_{IH}$.
- 12) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
- 13) Valid commands for Self Refresh Exit are NOP and DESELCT only.
- 14) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See [Chapter 2.10](#) and [Chapter 2.9.2](#) for a detailed list of restrictions.
- 15) Self Refresh mode can only be entered from the All Banks Idle state.
- 16) Must be a legal command as defined in the Command Truth Table.

Table 17 Data Mask (DM) Truth Table

| Name (Function) | DM | DQs | Note |
|-----------------|----|-------|------|
| Write Enable | L | Valid | 1) |
| Write Inhibit | H | X | 1) |

- 1) Used to mask write data; provided coincident with the corresponding data.

4 Absolute Maximum Ratings

Table 18 Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit | Note |
|-------------------|---|--------------|------|------|
| V_{DD} | Voltage on V_{DD} pin relative to V_{SS} | -1.0 to +2.3 | V | 1) |
| V_{DDQ} | Voltage on V_{DDQ} pin relative to V_{SS} | -0.5 to +2.3 | V | 1) |
| V_{DDL} | Voltage on VDDL pin relative to V_{SS} | -0.5 to +2.3 | V | 1) |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.5 to +2.3 | V | 1) |
| T_{STG} | Storage Temperature | -55 to +100 | °C | 1)2) |

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

5 Electrical Characteristics

Table 19 DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Unit | Note |
|------------|-----------------------|---------|------|----------|
| T_{OPER} | Operating Temperature | 0 to 95 | °C | 1)2)3)4) |

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Above 85 °C case temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$.
- 4) Self-Refresh period is hard-coded in the chip and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

5.1 DC Characteristics

Table 20 Recommended DC Operating Conditions (SSTL_18)

| Symbol | Parameter | Rating | | | Unit | Note |
|------------|---------------------------|-----------------------|----------------------|-----------------------|------|------|
| | | Min. | Typ. | Max. | | |
| V_{DD} | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1) |
| V_{DDDL} | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 1) |
| V_{DDQ} | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1) |
| V_{REF} | Input Reference Voltage | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 2)3) |
| V_{TT} | Termination Voltage | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V | 4) |

- 1) V_{DDQ} tracks with V_{DD} , V_{DDDL} tracks with V_{DD} . AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDDL} tied together.
- 2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
- 3) Peak to peak ac noise on V_{REF} may not exceed $\pm 2\% V_{REF}$ (dc)
- 4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in die dc level of V_{REF} .

Table 21 ODT DC Electrical Characteristics

| Parameter / Condition | Symbol | Min. | Nom. | Max. | Unit | Note |
|--|----------------|-------|------|--------|----------|------|
| Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm | $R_{tt1(eff)}$ | 60 | 75 | 90 | Ω | 1) |
| Termination resistor impedance value for EMRS(1)[A6,A2] = [1,0]; 150 Ohm | $R_{tt2(eff)}$ | 120 | 150 | 180 | Ω | 1) |
| Deviation of V_M with respect to $V_{DDQ} / 2$ | delta V_M | -6.00 | — | + 6.00 | % | 2) |

- 1) Measurement Definition for $R_{tt(eff)}$: Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively. $R_{tt(eff)} = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.
- 2) Measurement Definition for V_M : Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: $delta V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$

Table 22 Input and Output Leakage Currents

| Symbol | Parameter / Condition | Min. | Max. | Unit | Note |
|----------|---|------|------|---------------|------|
| I_{IL} | Input Leakage Current; any input $0\text{ V} < V_{IN} < V_{DD}$ | -2 | +2 | μA | 1) |
| I_{OL} | Output Leakage Current; $0\text{ V} < V_{OUT} < V_{DDQ}$ | -5 | +5 | μA | 2) |

1) all other pins not under test = 0 V

2) DQ's, LDQS, $\overline{\text{LDQS}}$, UDQS, $\overline{\text{UDQS}}$, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$ are disabled and ODT is turned off

5.2 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{\text{DQS}}$ " mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured

relative to the rising or falling edges of DQS crossing at V_{REF} . In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{\text{DQS}}$. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{\text{DQS}}$ (and $\overline{\text{RDQS}}$) signals are internally disabled and don't care.

Table 23 DC & AC Logic Input Levels

| Symbol | Parameter | Min. | Max. | Unit |
|--------------|---------------------|-------------------|-------------------|------|
| $V_{IH(dc)}$ | DC input logic high | $V_{REF} + 0.125$ | $V_{DDQ} + 0.3$ | V |
| $V_{IL(dc)}$ | DC input low | -0.3 | $V_{REF} - 0.125$ | V |
| $V_{IH(ac)}$ | AC input logic high | $V_{REF} + 0.250$ | — | V |
| $V_{IL(ac)}$ | AC input low | — | $V_{REF} - 0.250$ | V |

Table 24 Single-ended AC Input Test Conditions

| Symbol | Condition | Value | Unit | Note |
|------------------|---|----------------------|--------|------|
| V_{REF} | Input reference voltage | $0.5 \times V_{DDQ}$ | V | 1) |
| $V_{SWING(max)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1) |
| SLEW | Input signal minimum Slew Rate | 1.0 | V / ns | 2)3) |

1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.

2) The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac)min}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac)max}$ for falling edges as shown in [Figure 61](#)

3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

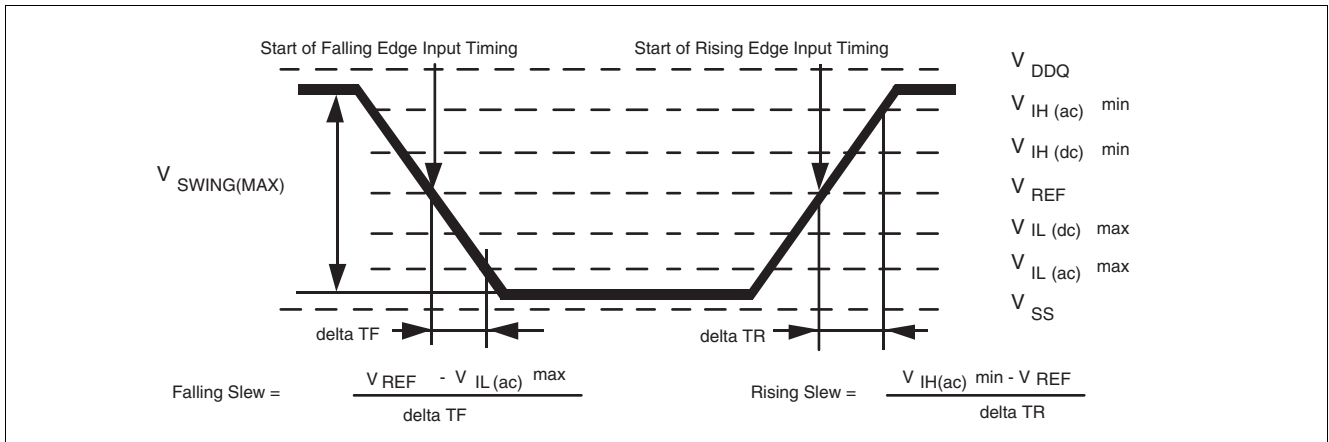


Figure 61 Single-ended AC Input Test Conditions Diagram

Table 25 Differential DC and AC Input and Output Logic Levels

| Symbol | Parameter | Min. | Max. | Unit | Note |
|--------------|--|------------------------------|------------------------------|------|------|
| $V_{IN(dc)}$ | DC input signal voltage | -0.3 | $V_{DDQ} + 0.3$ | — | 1) |
| $V_{ID(dc)}$ | DC differential input voltage | 0.25 | $V_{DDQ} + 0.6$ | — | 2) |
| $V_{ID(ac)}$ | AC differential input voltage | 0.5 | $V_{DDQ} + 0.6$ | V | 3) |
| $V_{IX(ac)}$ | AC differential cross point input voltage | $0.5 \times V_{DDQ} - 0.175$ | $0.5 \times V_{DDQ} + 0.175$ | V | 4) |
| $V_{OX(ac)}$ | AC differential cross point output voltage | $0.5 \times V_{DDQ} - 0.125$ | $0.5 \times V_{DDQ} + 0.125$ | V | 5) |

- 1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, \overline{CK} , DQS, \overline{DQS} etc.
- 2) $V_{ID(dc)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.
- 3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.
- 4) The value of $V_{IX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ} . $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
- 5) The value of $V_{OX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ} . $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

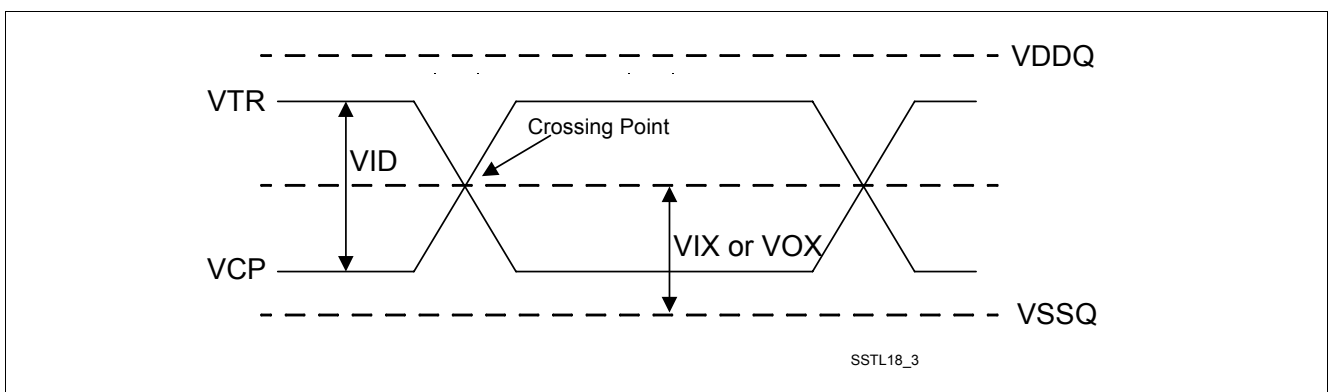


Figure 62 Differential DC and AC Input and Output Logic Levels Diagram

5.3 Output Buffer Characteristics

Table 26 SSTL_18 Output DC Current Drive

| Symbol | Parameter | SSTL_18 | Unit | Note |
|----------|----------------------------------|---------|------|------|
| I_{OH} | Output Minimum Source DC Current | -13.4 | mA | 1)2) |
| I_{OL} | Output Minimum Sink DC Current | 13.4 | mA | 2)3) |

- $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 1.42\text{ V}$. $(V_{OUT} - V_{DDQ}) / I_{OH}$ must be less than 21 Ohm for values of V_{OUT} between V_{DDQ} and $V_{DDQ} - 280\text{ mV}$.
- The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in 1) and 3). They are used to test drive current capability to ensure V_{IHmin} , plus a noise margin and V_{ILmax} minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 Ohm load line to define a convenient current for measurement.
- $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = 280\text{ mV}$. V_{OUT} / I_{OL} must be less than 21 Ohm for values of V_{OUT} between 0 V and 280 mV.

Table 27 SSTL_18 Output AC Test Conditions

| Symbol | Parameter | SSTL_18 | Unit | Note |
|-----------|---|----------------------|------|------|
| V_{OH} | Minimum Required Output Pull-up | $V_{TT} + 0.603$ | V | 1) |
| V_{OL} | Maximum Required Output Pull-down | $V_{TT} - 0.603$ | V | 1) |
| V_{OTR} | Output Timing Measurement Reference Level | $0.5 \times V_{DDQ}$ | V | |

- SSTL_18 test load for V_{OH} and V_{OL} is different from the referenced load described in [Chapter 8.1](#). The SSTL_18 test load has a 20 Ohm series resistor additionally to the 25 Ohm termination resistor into V_{TT} . The SSTL_18 definition assumes that $\pm 335\text{ mV}$ must be developed across the effectively 25 Ohm termination resistor ($13.4\text{ mA} \times 25\text{ Ohm} = 335\text{ mV}$). With an additional series resistor of 20 Ohm this translates into a minimum requirement of 603 mV swing relative to V_{TT} , at the output device ($13.4\text{ mA} \times 45\text{ Ohm} = 603\text{ mV}$).

Table 28 OCD Default Characteristics

| Symbol | Description | Min. | Nominal | Max. | Unit | Note |
|-----------|--|------|---------|------|--------|------------|
| — | Output Impedance | 12.6 | 18 | 23.4 | Ohms | 1)2) |
| — | Pull-up / Pull down mismatch | 0 | — | 4 | Ohms | 1)2)3) |
| — | Output Impedance step size for OCD calibration | 0 | — | 1.5 | Ohms | 4) |
| S_{OUT} | Output Slew Rate | 1.5 | — | 5.0 | V / ns | 1)5)6)7)8) |

- $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$; $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$
- Impedance measurement condition for output source dc current: $V_{DDQ} = 1.7\text{ V}$, $V_{OUT} = 1420\text{ mV}$; $(V_{OUT} - V_{DDQ}) / I_{OH}$ must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and $V_{DDQ} - 280\text{ mV}$. Impedance measurement condition for output sink dc current: $V_{DDQ} = 1.7\text{ V}$; $V_{OUT} = -280\text{ mV}$; V_{OUT} / I_{OL} must be less than 23.4 Ohms for values of V_{OUT} between 0 V and 280 mV.
- Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
- This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is $18 \pm 0.75\text{ Ohms}$ under nominal conditions.
- Slew Rates according to [Chapter 8.2.1](#) $V_{IL(ac)}$ to $V_{IH(ac)}$ with the load specified in [Figure 67](#).
- The absolute value of the Slew Rate as measured from DC to DC is equal to or greater than the Slew Rate as measured from AC to AC. This is verified by design and characterization but not subject to production test.
- Timing skew due to DRAM output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ's is included in t_{DQSQ} and t_{QHS} specification.

8) DRAM output Slew Rate specification applies to 400 and 533 MT/s speed bins.

5.4 Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS(1) bits A[9:7] = '111'. [Figure 63](#) and [Figure 64](#) show the driver characteristics graphically and the tables show the same data suitable for input into simulation tools.

Table 29 Full Strength Default Pull-up Driver Characteristics

| Voltage (V) | Pull-up Driver Current [mA] | | | |
|-------------|-----------------------------|-----------------------------------|------------------------------------|--------------------|
| | Min. ¹⁾ | Nominal Default low ²⁾ | Nominal Default high ²⁾ | Max. ³⁾ |
| 0.2 | -8.5 | -11.1 | -11.8 | -15.9 |
| 0.3 | -12.1 | -16.0 | -17.0 | -23.8 |
| 0.4 | -14.7 | -20.3 | -22.2 | -31.8 |
| 0.5 | -16.4 | -24.0 | -27.5 | -39.7 |
| 0.6 | -17.8 | -27.2 | -32.4 | -47.7 |
| 0.7 | -18.6 | -29.8 | -36.9 | -55.0 |
| 0.8 | -19.0 | -31.9 | -40.8 | -62.3 |
| 0.9 | -19.3 | -33.4 | -44.5 | -69.4 |
| 1.0 | -19.7 | -34.6 | -47.7 | -75.3 |
| 1.1 | -19.9 | -35.5 | -50.4 | -80.5 |
| 1.2 | -20.0 | -36.2 | -52.5 | -84.6 |
| 1.3 | -20.1 | -36.8 | -54.2 | -87.7 |
| 1.4 | -20.2 | -37.2 | -55.9 | -90.8 |
| 1.5 | -20.3 | -37.7 | -57.1 | -92.9 |
| 1.6 | -20.4 | -38.0 | -58.4 | -94.9 |
| 1.7 | -20.6 | -38.4 | -59.6 | -97.0 |
| 1.8 | — | -38.6 | -60.8 | -99.1 |
| 1.9 | — | — | — | -101.1 |

1) The driver characteristics evaluation conditions are Minimum 95 °C (T_{CASE}), $V_{DDQ} = 1.7$ V, slow–slow process

2) The driver characteristics evaluation conditions are Nominal Default 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process

3) The driver characteristics evaluation conditions are Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, fast–fast process

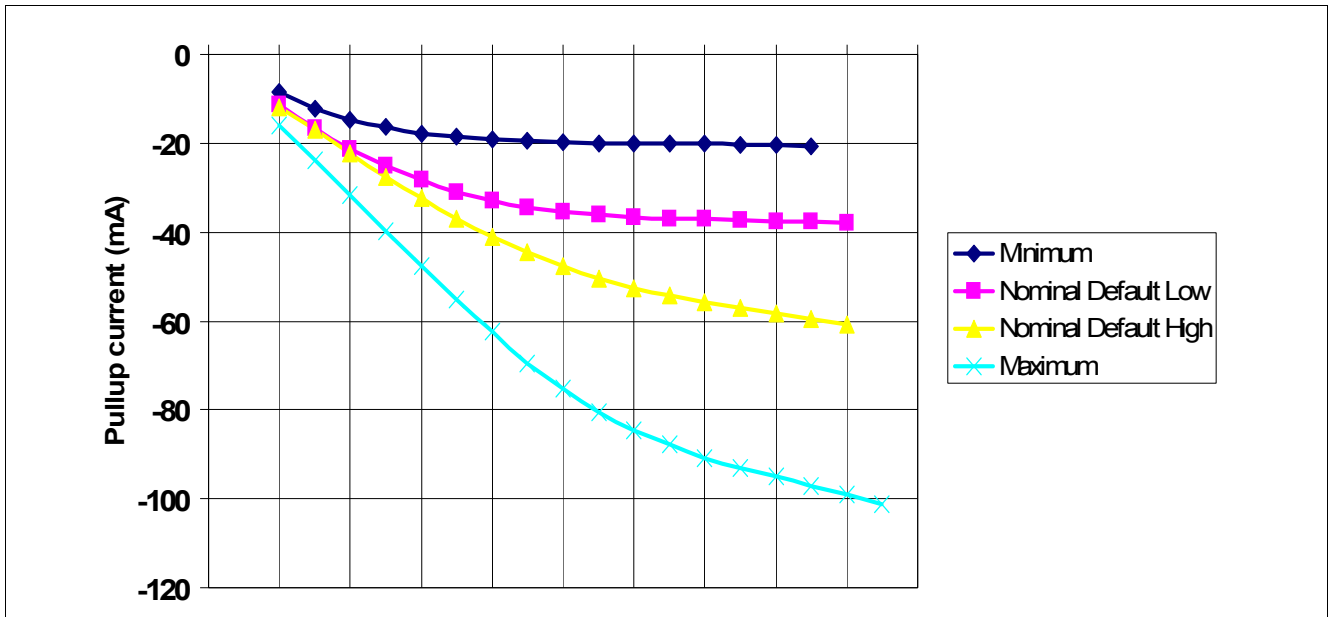


Figure 63 Full Strength Default Pull-up Driver Diagram

Table 30 Full Strength Default Pull-down Driver Characteristics

| Voltage (V) | Pull-down Driver Current [mA] | | | |
|-------------|-------------------------------|-----------------------------------|------------------------------------|--------------------|
| | Min. ¹⁾ | Nominal Default low ²⁾ | Nominal Default high ²⁾ | Max. ³⁾ |
| 0.2 | 8.5 | 11.3 | 11.8 | 15.9 |
| 0.3 | 12.1 | 16.5 | 16.8 | 23.8 |
| 0.4 | 14.7 | 21.2 | 22.1 | 31.8 |
| 0.5 | 16.4 | 25.0 | 27.6 | 39.7 |
| 0.6 | 17.8 | 28.3 | 32.4 | 47.7 |
| 0.7 | 18.6 | 30.9 | 36.9 | 55.0 |
| 0.8 | 19.0 | 33.0 | 40.9 | 62.3 |
| 0.9 | 19.3 | 34.5 | 44.6 | 69.4 |
| 1.0 | 19.7 | 35.5 | 47.7 | 75.3 |
| 1.1 | 19.9 | 36.1 | 50.4 | 80.5 |
| 1.2 | 20.0 | 36.6 | 52.6 | 84.6 |
| 1.3 | 20.1 | 36.9 | 54.2 | 87.7 |
| 1.4 | 20.2 | 37.1 | 55.9 | 90.8 |
| 1.5 | 20.3 | 37.4 | 57.1 | 92.9 |
| 1.6 | 20.4 | 37.6 | 58.4 | 94.9 |
| 1.7 | 20.6 | 37.7 | 59.6 | 97.0 |
| 1.8 | — | 37.9 | 60.9 | 99.1 |
| 1.9 | — | — | — | 101.1 |

1) The driver characteristics evaluation conditions are Minimum 95 °C (T_{CASE}), $V_{DDQ} = 1.7$ V, slow-slow process,

2) The driver characteristics evaluation conditions are Nominal Default 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process,

3) The driver characteristics evaluation conditions are Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, fast-fast process

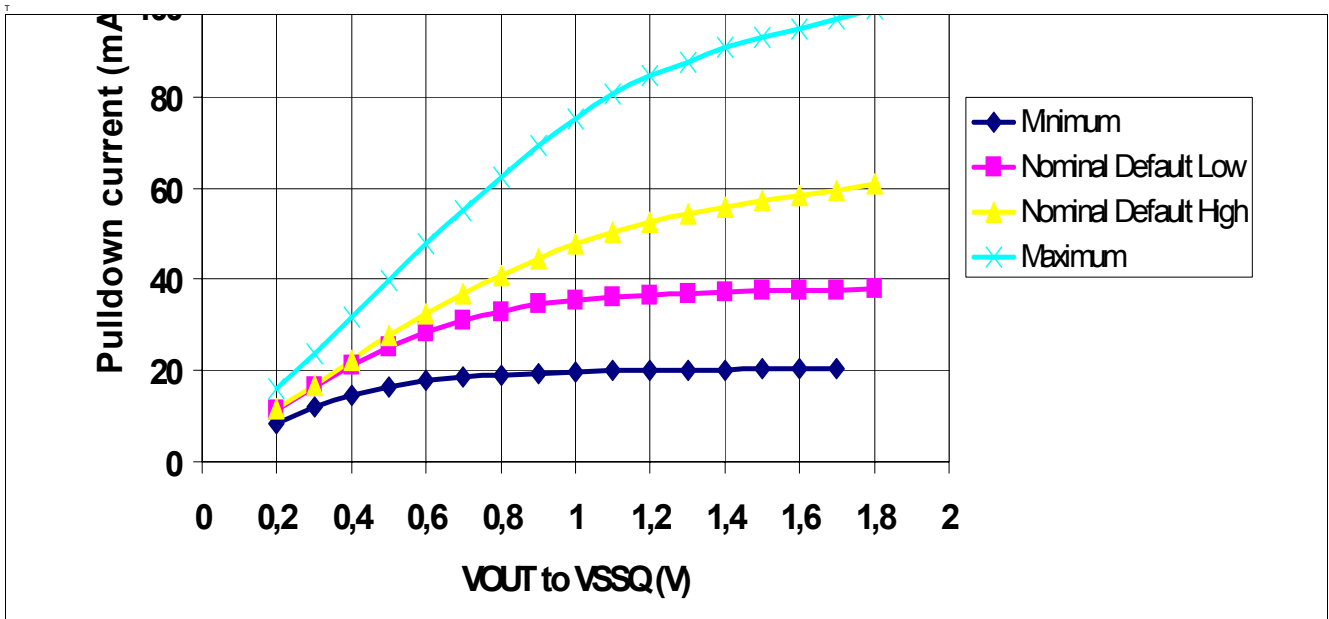


Figure 64 Full Strength Default Pull-down Driver Diagram

5.4.1 Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The [Table 31](#) and [Table 32](#) show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while

looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figure. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy and uncertainty with DQ to DQ variation, it is recommended that only the default values to be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

Table 31 Full Strength Calibrated Pull-down Driver Characteristics

| Voltage (V) | Calibrated Pull-down Driver Current [mA] | | | | |
|-------------|--|---|------------------------------------|--|--|
| | Nominal Minimum ¹⁾ (21 Ohms) | Nominal Low ²⁾ (18.75 Ohms) | Nominal ³⁾ (18 ohms) | Nominal High ²⁾ (17.25 Ohms) | Nominal Maximum ⁴⁾ (15 Ohms) |
| 0.2 | 9.5 | 10.7 | 11.5 | 11.8 | 13.3 |
| 0.3 | 14.3 | 16.0 | 16.6 | 17.4 | 20.0 |
| 0.4 | 18.7 | 21.0 | 21.6 | 23.0 | 27.0 |

- 1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}). $V_{DDQ} = 1.7$ V, any process
- 2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, any process
- 3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process
- 4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, any process

Table 32 Full Strength Calibrated Pull-up Driver Characteristics

| Voltage (V) | Calibrated Pull-up Driver Current [mA] | | | | |
|-------------|--|---|------------------------------------|--|--|
| | Nominal Minimum ¹⁾ (21 Ohms) | Nominal Low ²⁾ (18.75 Ohms) | Nominal (18 ohms) ³⁾ | Nominal High ²⁾ (17.25 Ohms) | Nominal Maximum ⁴⁾ (15 Ohms) |
| 0.2 | -9.5 | -10.7 | -11.4 | -11.8 | -13.3 |
| 0.3 | -14.3 | -16.0 | -16.5 | -17.4 | -20.0 |
| 0.4 | -18.3 | -21.0 | -21.2 | -23.0 | -27.0 |

- 1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}). $V_{DDQ} = 1.7$ V, any process
- 2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, any process
- 3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process
- 4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, any process

5.5 Input / Output Capacitance

Table 33 Input / Output Capacitance

| Symbol | Parameter | Min. | Max. | Unit |
|--------|---|------|------|------|
| CCK | Input capacitance, CK and \overline{CK} | 1.0 | 2.0 | pF |
| CDCK | Input capacitance delta, CK and \overline{CK} | — | 0.25 | pF |
| CI | Input capacitance, all other input-only pins | 1.0 | 2.0 | pF |
| CDI | Input capacitance delta, all other input-only pins | — | 0.25 | pF |
| CIO | Input/output capacitance, DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS} | 2.5 | 4.0 | pF |
| CDIO | Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS} | — | 0.5 | pF |

5.6 Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A[13:0], BA[2:0]), $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{CS}}$, $\overline{\text{WE}}$, and ODT pins. The V-I characteristics for pins with clamps is shown in [Table 34](#).

Table 34 Power & Ground Clamp V-I Characteristics

| Voltage across clamp (V) | Minimum Power Clamp Current (mA) | Minimum Ground Clamp Current (mA) |
|--------------------------|----------------------------------|-----------------------------------|
| 0.0 | 0 | 0 |
| 0.1 | 0 | 0 |
| 0.2 | 0 | 0 |
| 0.3 | 0 | 0 |
| 0.4 | 0 | 0 |
| 0.5 | 0 | 0 |
| 0.6 | 0 | 0 |
| 0.7 | 0 | 0 |
| 0.8 | 0.1 | 0.1 |
| 0.9 | 1.0 | 1.0 |
| 1.0 | 2.5 | 2.5 |
| 1.1 | 4.7 | 4.7 |
| 1.2 | 6.8 | 6.8 |
| 1.3 | 9.1 | 9.1 |
| 1.4 | 11.0 | 11.0 |
| 1.5 | 13.5 | 13.5 |
| 1.6 | 16.0 | 16.0 |
| 1.7 | 18.2 | 18.2 |
| 1.8 | 21.0 | 21.0 |

5.7 Overshoot and Undershoot Specification

Table 35 AC Overshoot / Undershoot Specification for Address and Control Pins

| Parameter | DDR2-400 | DDR2-533 | Unit |
|--|----------|----------|------|
| Maximum peak amplitude allowed for overshoot area | 0.9 | 0.9 | V |
| Maximum peak amplitude allowed for undershoot area | 0.9 | 0.9 | V |
| Maximum overshoot area above V_{DD} | 0.75 | 0.56 | V.ns |
| Maximum undershoot area below V_{SS} | 0.75 | 0.56 | V.ns |

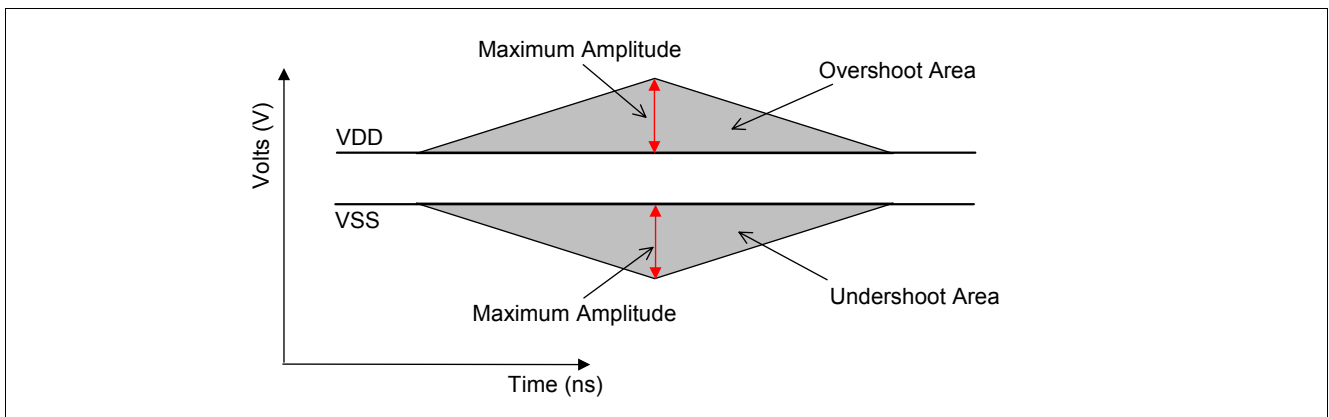


Figure 65 AC Overshoot / Undershoot Diagram for Address and Control Pins

Table 36 AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

| Parameter | DDR2-400 | DDR2-533 | Unit |
|--|----------|----------|------|
| Maximum peak amplitude allowed for overshoot area | 0.9 | 0.9 | V |
| Maximum peak amplitude allowed for undershoot area | 0.9 | 0.9 | V |
| Maximum overshoot area above V_{DDQ} | 0.38 | 0.28 | V.ns |
| Maximum undershoot area below V_{SSQ} | 0.38 | 0.28 | V.ns |

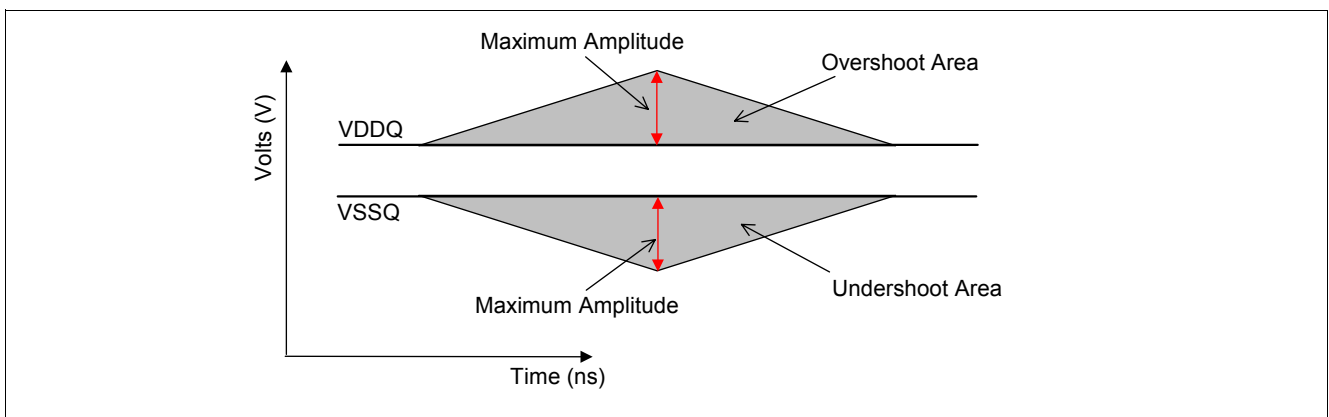


Figure 66 AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins

6 I_{DD} Specifications and Conditions

Table 37 I_{DD} Measurement Conditions

| Parameter | Symbol | Note |
|--|---------------|--------------|
| Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, \overline{CS} is high, \overline{CS} is high between valid commands. Address and control inputs are switching; Databus inputs are switching. | I_{DD0} | 1)2)3)4)5)6) |
| Operating Current - One bank Active - Read - Precharge $I_{OUT} = 0$ mA, $BL = 4$, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, $AL = 0$, $CL = C(IDD)$; \overline{CS} is high, \overline{CS} is high between valid commands. Address and control inputs are switching; Databus inputs are switching. | I_{DD1} | 1)2)3)4)5)6) |
| Precharge Power-Down Current All banks idle; \overline{CS} is low; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable; Data bus inputs are floating. | I_{DD2P} | 1)2)3)4)5)6) |
| Precharge Standby Current All banks idle; \overline{CS} is high; \overline{CS} is high; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching. | I_{DD2N} | 1)2)3)4)5)6) |
| Precharge Quiet Standby Current All banks idle; \overline{CS} is high; \overline{CS} is high; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating. | I_{DD2Q} | 1)2)3)4)5)6) |
| Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, \overline{CS} is low; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to "0" (Fast Power-down Exit). | $I_{DD3P(0)}$ | 1)2)3)4)5)6) |
| Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, \overline{CS} is low; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to "1" (Slow Power-down Exit); | $I_{DD3P(1)}$ | 1)2)3)4)5)6) |
| Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CS} is high, \overline{CS} is high between valid commands. Address inputs are switching; Data Bus inputs are switching; | I_{DD3N} | 1)2)3)4)5)6) |
| Operating Current Burst Read: All banks open; Continuous burst reads; $BL = 4$; $AL = 0$, $CL = CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CS} is high, \overline{CS} is high between valid commands. Address inputs are switching; Data Bus inputs are switching; $I_{OUT} = 0$ mA. | I_{DD4R} | 1)2)3)4)5)6) |
| Operating Current Burst Write: All banks open; Continuous burst writes; $BL = 4$; $AL = 0$, $CL = CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CS} is high, \overline{CS} is high between valid commands. Address inputs are switching; Data Bus inputs are switching; | I_{DD4W} | 1)2)3)4)5)6) |
| Burst Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, \overline{CS} is high, \overline{CS} is high between valid commands, Other control and address inputs are switching, Data bus inputs are switching. | I_{DD5B} | 1)2)3)4)5)6) |
| Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{REFI} = 7.8$ μ s interval, \overline{CS} is low and \overline{CS} is high between valid commands, Other control and address inputs are switching, Data bus inputs are switching. | I_{DD5D} | 1)2)3)4)5)6) |

Table 37 I_{DD} Measurement Conditions

| Parameter | Symbol | Note |
|---|-----------|----------------|
| Self-Refresh Current CKE \leq 0.2 V; external clock off, CK and \overline{CK} at 0 V; Other control and address inputs are floating, Data bus inputs are floating. | I_{DD6} | 1)2)3)4)5)6) |
| All Bank Interleave Read Current 1. All banks interleaving reads, $I_{OUT} = 0$ mA; BL = 4, CL=CL _(IDD) , AL = $t_{RCD(IDD)} - 1 \times t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$; $t_{FAW} = t_{FAW(IDD)}$; CKE is high, \overline{CS} is high between valid commands. Address bus inputs are stable during deselects; Data bus is switching. 2. Timing pattern for $\times 4$ and $\times 8$ components: – DDR2-400: A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7 (16 clocks) – DDR2-533: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D (20 clocks) 3. Timing pattern for $\times 16$ components: – DDR2 -400: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D (20 clocks) – DDR2 -533: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D (28 clocks) | I_{DD7} | 1)2)3)4)5)6)7) |

- 1) $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$
- 2) I_{DD} specifications are tested after the device is properly initialized.
- 3) I_{DD} parameter are specified with ODT disabled.
- 4) Data Bus consists of DQ, DM, DQS, \overline{DQS} , RDQS, \overline{RDQS} , LDQS, \overline{LDQS} , UDQS and \overline{UDQS} .
- 5) Definitions for I_{DD} :
 low is defined as $V_{IN} \leq V_{IL(ac)max}$;
 high is defined as $V_{IN} \geq V_{IH(ac)min}$;
 stable is defined as inputs are stable at a high or low level;
 floating is defined as inputs are $V_{REF} = V_{DDQ} / 2$;
 switching is defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or stobes.
- 6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in [Table 40](#).
- 7) A = Activate, RA = Read with Auto-Precharge, D=DESELECT

I_{DD} Specifications and Conditions

Table 38 I_{DD} Specification

| Product Type Speed Code | -3.7 | -5 | Unit | Note |
|-------------------------|----------|----------|------|--------|
| Speed Grade | DDR2-533 | DDR2-400 | | |
| Symbol | Max. | Max. | | |
| I_{DD0} | 75 | 70 | mA | 1) |
| | 80 | 75 | mA | 2) |
| I_{DD1} | 85 | 80 | mA | 1) |
| | 95 | 90 | mA | 2) |
| I_{DD2P} | 5 | 5 | mA | 3) |
| I_{DD2N} | 46 | 35 | mA | 3) |
| I_{DD2Q} | 32 | 28 | mA | 3) |
| I_{DD3P} | 17 | 13 | mA | 3)4) |
| | 6 | 5 | mA | 3)5) |
| I_{DD3N} | 50 | 40 | mA | 3) |
| I_{DD4R} | 110 | 90 | mA | 1) |
| | 130 | 105 | mA | 2) |
| I_{DD4W} | 115 | 95 | mA | 1) |
| | 165 | 130 | mA | 2) |
| I_{DD5B} | 185 | 180 | mA | 3) |
| I_{DD5D} | 7 | 7 | mA | 3) |
| I_{DD6} | 5 | 5 | mA | 3)6)7) |
| | 3 | 3 | mA | 3)8)9) |
| I_{DD7} | 205 | 195 | mA | 1) |
| | 270 | 255 | mA | 2) |

- 1) $\times 4/\times 8$
- 2) $\times 16$
- 3) $\times 16/\times 4/\times 8$
- 4) MRS(12)=0
- 5) MRS(12)=1
- 6) I_{DD6} : $0 \leq T_{CASE} \leq 85$ °C
- 7) standard products
- 8) low power products
- 9) available on request

6.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 39 I_{DD} Measurement Test Condition

| Parameter | Symbol | -3.7 | -5 | Unit | Note |
|--|-------------------|-------------------|----------------|----------|------|
| | | DDR2-533 4-4-4 | DDR2-400 3-3-3 | | |
| CAS Latency | $CL_{(IDD)}$ | 4 | 3 | t_{CK} | |
| Clock Cycle Time | $t_{CK(IDD)}$ | 3.75 | 5 | ns | |
| Active to Read or Write delay | $t_{RCD(IDD)}$ | 15 | 15 | ns | |
| Active to Active / Auto-Refresh command period | $t_{RC(IDD)}$ | 60 | 55 | ns | |
| Four Active Window Period | $t_{FAW(IDD)}$ | 37.5 | 37.5 | ns | 1) |
| | | 50 | 50 | ns | 2) |
| Active bank A to Active bank B command delay | $t_{RRD(IDD)}$ | 7.5 | 7.5 | ns | 1) |
| | | 10 | 10 | ns | 2) |
| Active to Precharge Command | $t_{RASmin(IDD)}$ | 45 | 40 | ns | |
| | | $t_{RASmax(IDD)}$ | 70000 | 70000 | ns |
| Precharge Command Period | $t_{RP(min)}$ | 15 | 15 | ns | |
| Auto-Refresh to Active / Auto-Refresh command period | $t_{RFC(IDD)}$ | 127.5 | 127.5 | ns | |

1) $\times 4$ & $\times 8$ (1 kB page size)

2) $\times 16$ (2 kB page size)

6.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "weak" or "strong" termination can be selected. The

current consumption for any terminated input pin depends on whether the input pin is driven or floating. See [Table 40](#).

Table 40 ODT current per terminated input pin

| ODT Current | | EMRS(1) State | Min. | Typ. | Max. | Unit |
|---|------------|----------------|------|------|------|-------|
| Enabled ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; Data Bus inputs are floating | I_{ODTO} | A6 = 0, A2 = 1 | 5 | 6 | 7.5 | mA/DQ |
| | | A6 = 1, A2 = 0 | 2.5 | 3 | 3.75 | mA/DQ |
| Active ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are stable or switching. | I_{ODTT} | A6 = 0, A2 = 1 | 10 | 12 | 15 | mA/DQ |
| | | A6 = 1, A2 = 0 | 5 | 6 | 7.5 | mA/DQ |

Note: For power consumption calculations the ODT duty cycle has to be taken into account

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Table 41 Speed Grade Definition Speed Bins

| Speed Grade | | | DDR2-533C | | DDR2-400B | | Unit | Note |
|----------------------|----------|-----------|-----------|-------|-----------|-------|----------|------------|
| IFX Sort Name | | | -3.7 | | -5 | | | |
| CAS-RCD-RP latencies | | | 4-4-4 | | 3-3-3 | | t_{CK} | |
| Parameter | | Symbol | Min. | Max. | Min. | Max. | — | |
| Clock Frequency | @ CL = 3 | t_{CK} | 5 | 8 | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 4 | t_{CK} | 3.75 | 8 | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 5 | t_{CK} | 3.75 | 8 | 5 | 8 | ns | 1)2)3)4) |
| RAS-CAS-Delay | | t_{RAS} | 45 | 70000 | 40 | 70000 | ns | 1)2)3)4)5) |
| Row Precharge Time | | t_{RC} | 60 | — | 55 | — | ns | 1)2)3)4) |
| Row Active Time | | t_{RCD} | 15 | — | 15 | — | ns | 1)2)3)4) |
| Row Cycle Time | | t_{RP} | 15 | — | 15 | — | ns | 1)2)3)4) |

- 1) Timings are guaranteed with CK/\overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see [Chapter 8](#). Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the "Reference Load for Timing Measurements" according to [Chapter 8.1](#) only.
- 2) The CK/\overline{CK} input reference level (for timing reference to CK/\overline{CK}) is the point at which CK and \overline{CK} cross. The DQS/\overline{DQS} , $RDQS/\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/\overline{CK} , DQS/\overline{DQS} , $RDQS/\overline{RDQS}$ is defined in [Chapter 8.3](#).
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} . See section 8 for the reference load for timing measurements.
- 5) $t_{RAS(max)}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.

Table 42 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533

| Parameter | Symbol | -3.7 DDR2-533 4-4-4 | | -5 DDR2-400 3-3-3 | | Unit | Note 1)2)3)4)5)6) |
|--|-----------------|----------------------------|------|----------------------------|-------|----------|----------------------|
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK/\overline{CK} | t_{AC} | -500 | +500 | -600 | + 600 | ps | |
| CAS A to \overline{CAS} B command period | t_{CCD} | 2 | — | 2 | — | t_{CK} | |
| CK , \overline{CK} high-level width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | |
| CKE minimum high and low pulse width | t_{CKE} | 3 | — | 3 | — | t_{CK} | |
| CK , \overline{CK} low-level width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | |
| Auto-Precharge write recovery + precharge time | t_{DAL} | $WR + t_{RP}$ | — | $WR + t_{RP}$ | — | t_{CK} | 7) |
| Minimum time clocks remain ON after CKE asynchronously drops LOW | t_{DELAY} | $t_{IS} + t_{CK} + t_{IH}$ | — | $t_{IS} + t_{CK} + t_{IH}$ | — | ns | 8) |
| DQ and DM input hold time | $t_{DH}(base)$ | 225 | — | 275 | — | ps | 9) |
| DQ and DM input hold time (single ended data strobe) | $t_{DH1}(base)$ | -25 | — | 25 | — | ps | 9) |

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Table 42 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533

| Parameter | Symbol | -3.7 DDR2-533 4-4-4 | | -5 DDR2-400 3-3-3 | | Unit | Note 1)2)3)4)5)6) |
|--|------------------------|---------------------------|-------------|---------------------------|-------------|----------|----------------------|
| | | Min. | Max. | Min. | Max. | | |
| DQ and DM input pulse width (each input) | t_{DIPW} | 0.35 | — | 0.35 | — | t_{CK} | |
| DQS output access time from CK / \overline{CK} | t_{DQSK} | -450 | +450 | -500 | + 500 | ps | |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | t_{CK} | |
| DQS-DQ skew (for DQS & associated DQ signals) | t_{DQSQ} | — | 300 | — | 350 | ps | 10) |
| Write command to 1st DQS latching transition | t_{DQSS} | WL - 0.25 | WL + 0.25 | WL - 0.25 | WL + 0.25 | t_{CK} | |
| DQ and DM input setup time | $t_{DS}(\text{base})$ | 100 | — | 150 | — | ps | 9) |
| DQ and DM input setup time (single ended data strobe) | $t_{DS1}(\text{base})$ | -25 | — | 25 | — | ps | 9) |
| DQS falling edge hold time from CK (write cycle) | t_{DSH} | 0.2 | — | 0.2 | — | t_{CK} | |
| DQS falling edge to CK setup time (write cycle) | t_{DSS} | 0.2 | — | 0.2 | — | t_{CK} | |
| Four Activate Window period | t_{FAW} | 37.5 | — | 37.5 | — | ns | 11)12) |
| | | 50 | — | 50 | — | ns | 13)12) |
| Clock half period | t_{HP} | min. (t_{CL}, t_{CH}) | | min. (t_{CL}, t_{CH}) | | | 14) |
| Data-out high-impedance time from CK / \overline{CK} | t_{HZ} | — | t_{ACmax} | — | t_{ACmax} | ps | 15) |
| Address and control input hold time | t_{IH} | 375 | — | 475 | — | ps | 9) |
| Address and control input pulse width (each input) | t_{IPW} | 0.6 | — | 0.6 | — | t_{CK} | |
| Address and control input setup time | t_{IS} | 250 | — | 350 | — | ps | 9) |
| DQ low-impedance time from CK / \overline{CK} | $t_{LZ(DQ)}$ | $2 \times t_{ACmin}$ | t_{ACmax} | $2 \times t_{ACmin}$ | t_{ACmax} | ps | 15) |
| DQS low-impedance from CK / \overline{CK} | $t_{LZ(DQS)}$ | t_{ACmin} | t_{ACmax} | t_{ACmin} | t_{ACmax} | ps | 15) |
| Mode register set command cycle time | t_{MRD} | 2 | — | 2 | — | t_{CK} | |
| OCD drive mode output delay | t_{OIT} | 0 | 12 | 0 | 12 | ns | |
| Data output hold time from DQS | t_{QH} | $t_{HP} - t_{QHS}$ | — | $t_{HP} - t_{QHS}$ | — | | |
| Data hold skew factor | t_{QHS} | — | 400 | — | 450 | ps | |
| Average periodic refresh Interval | t_{REFI} | — | 7.8 | — | 7.8 | μs | 16)17) |
| | | — | 3.9 | — | 3.9 | μs | 16)18) |
| Auto-Refresh to Active/Auto-Refresh command period | t_{RFC} | 127.5 | — | 127.5 | — | ns | 19) |

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Table 42 Timing Parameter by Speed Grade - DDR2-400 & DDR2-533

| Parameter | Symbol | -3.7 DDR2-533 4-4-4 | | -5 DDR2-400 3-3-3 | | Unit | Note 1)2)3)4)5)6) |
|---|-------------|------------------------|------|----------------------|------|----------|----------------------|
| | | Min. | Max. | Min. | Max. | | |
| Precharge-All (8 banks) command period | t_{RP} | $t_{RP}+1t_{CK}$ | — | $t_{RP}+1t_{CK}$ | — | ns | 20) |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | 15) |
| Read postamble | t_{RPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 15) |
| Active bank A to Active bank B command period | t_{RRD} | 7.5 | — | 7.5 | — | ns | 11)21) |
| | | 10 | — | 10 | — | ns | 13)21) |
| Internal Read to Precharge command delay | t_{RTP} | 7.5 | — | 7.5 | — | ns | |
| Write preamble | t_{WPRE} | 0.25 | — | 0.25 | — | t_{CK} | |
| Write postamble | t_{WPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 22) |
| Write recovery time | t_{WR} | 15 | — | 15 | — | ns | |
| Internal Write to Read command delay | t_{WTR} | 7.5 | — | 10 | — | ns | 23) |
| Exit power down to any valid command (other than NOP or Deselect) | t_{XARD} | 2 | — | 2 | — | t_{CK} | 24) |
| Exit active power-down mode to Read command (slow exit, lower power) | t_{XARDS} | 6 - AL | — | 6 - AL | — | t_{CK} | 24) |
| Exit precharge power-down to any valid command (other than NOP or Deselect) | t_{XP} | 2 | — | 2 | — | t_{CK} | |
| Exit Self-Refresh to non-Read command | t_{XSNR} | $t_{RFC}+10$ | — | $t_{RFC}+10$ | — | ns | |
| Exit Self-Refresh to Read command | t_{XSRD} | 200 | — | 200 | — | t_{CK} | |

- 1) $V_{DDQ} = 1.8V \pm 0.1V$; $V_{DD} = 1.8V \pm 0.1V$. See notes ³⁾⁴⁾⁵⁾⁶⁾
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/\overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see [Chapter 8](#) of this data sheet. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the [Reference Load for Timing Measurements](#) according to [Chapter 8.1](#) only.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , $RDQS / \overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/\overline{CK} , DQS / \overline{DQS} , $RDQS / \overline{RDQS}$ is defined in [Chapter 8.3](#) of this data sheet.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} . See [Chapter 8](#) for the reference load for timing measurements.
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required as describes in [Chapter 2.12](#).
- 9) For timing definition, Slew Rate and Slew Rate derating see [Chapter 8.3](#)

Electrical Characteristics

- 10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between \overline{DQS} / \overline{DQS} and associated DQ in any given cycle.
- 11) $\times 4$ & $\times 8$ (1k page size)
- 12) 8 bank device Sequential Activation Restriction. No more than 4 banks may be activated in a rolling t_{FAW} window.
- 13) $\times 16$ (2k page size)
- 14) Min (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 15) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 16) The Auto-Refresh command interval has been reduced to 3.9 μs when operating the DDR2 DRAM in a temperature range between 85°C and 95°C.
- 17) $0 \leq T_{CASE} \leq 85^\circ C$
- 18) $85^\circ C < T_{CASE} \leq 95^\circ C$
- 19) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 20) $t_{RP(A)}$ for a Precharge-All command for an 8 bank device is equal to $t_{RP} + 1 \times t_{CK}$, where t_{RP} are the values for a single bank precharge.
- 21) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See [Chapter 1.5](#)
- 22) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 23) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 24) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing t_{XARDS} has to be satisfied.

Table 43 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

| Symbol | Parameter / Condition | Min. | Max. | Unit | Note |
|-------------|--------------------------------------|----------------------|-----------------------------------|----------|------|
| t_{AOND} | ODT turn-on delay | 2 | 2 | t_{CK} | |
| t_{AON} | ODT turn-on | $t_{AC(min)}$ | $t_{AC(max)} + 1$ ns | ns | 1) |
| t_{AONPD} | ODT turn-on (Power-Down Modes) | $t_{AC(min)} + 2$ ns | $2 t_{CK} + t_{AC(max)} + 1$ ns | ns | |
| t_{AOFD} | ODT turn-off delay | 2.5 | 2.5 | t_{CK} | |
| t_{AOF} | ODT turn-off | $t_{AC(min)}$ | $t_{AC(max)} + 0.6$ ns | ns | 2) |
| t_{AOFPD} | ODT turn-off (Power-Down Modes) | $t_{AC(min)} + 2$ ns | $2.5 t_{CK} + t_{AC(max)} + 1$ ns | ns | |
| t_{ANPD} | ODT to Power Down Mode Entry Latency | 3 | — | t_{CK} | |
| t_{AXPD} | ODT Power Down Exit Latency | 8 | — | t_{CK} | |

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .

Note: For product nomenclature see [Chapter 10](#) of this data sheet

8 AC Timing Measurement Conditions

8.1 Reference Load for Timing Measurements

Figure 67 represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial

transmission line terminated at the tester electronics. This reference load is also used for output Slew Rate characterization. The output timing reference voltage level for single ended signals is the crosspoint with V_{TT} . The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. \overline{DQS}) signal.

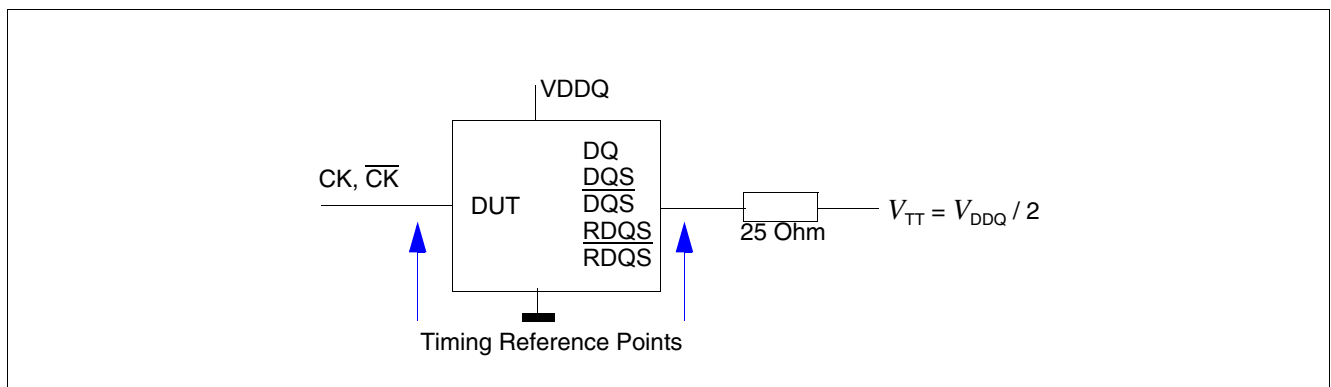


Figure 67 Reference Load for Timing Measurements

8.2 Slew Rate Measurement Conditions

8.2.1 Output Slew Rate

For DQ and single ended DQS signals output Slew Rate for falling and rising edges is measured between $V_{TT} - 250$ mV and $V_{TT} + 250$ mV.

For differential signals (DQS / \overline{DQS}) output Slew Rate is measured between $DQS - \overline{DQS} = -500$ mV and

$DQS - \overline{DQS} = +500$ mV. Output Slew Rate is defined with the reference load according to **Figure 67** and verified by design and characterization, but not subject to production test.

8.2.2 Input Slew Rate - Differential signals

Input Slew Rate for differential signals (CK / \overline{CK} , DQS / \overline{DQS} , RDQS / \overline{RDQS}) for rising edges are measured from $CK - \overline{CK} = -250$ mV to $CK - \overline{CK} = +500$ mV and

from $CK - \overline{CK} = +250$ mV to $CK - \overline{CK} = -500$ mV for falling edges.

8.3 Input and Data Setup and Hold Time

8.3.1 Definition for Input Setup (t_{IS}) and Hold Time (t_{IH})

Address and control input setup time (t_{IS}) is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test. Address and control input hold time

(t_{IH}) is referenced from the input signal crossing at the $V_{IL(dc)}$ level for a rising signal and $V_{IH(dc)}$ for a falling signal applied to the device under test.

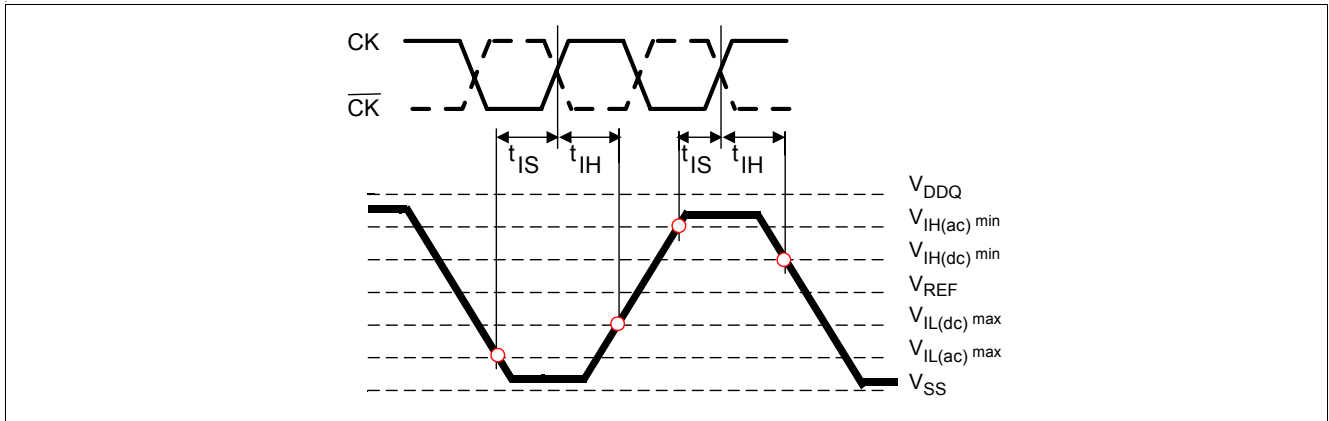


Figure 68 Input Setup and Hold Time

8.3.2 Definition for Data Setup (t_{DS}) and Hold Time (t_{DH}), differential Data Strobes

Data input setup time (t_{DS}) with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test.

DQS/ \overline{DQS} signals must be monotonic between $V_{IL(dc)max}$ and $V_{IH(dc)min}$. Data input hold time (t_{DH}) with

differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IL(dc)}$ level to the differential data strobe crosspoint for a rising signal and $V_{IH(dc)}$ to the differential data strobe crosspoint for a falling signal applied to the device under test.

DQS/ \overline{DQS} signals must be monotonic between $V_{IL(dc)max}$ and $V_{IH(dc)min}$.

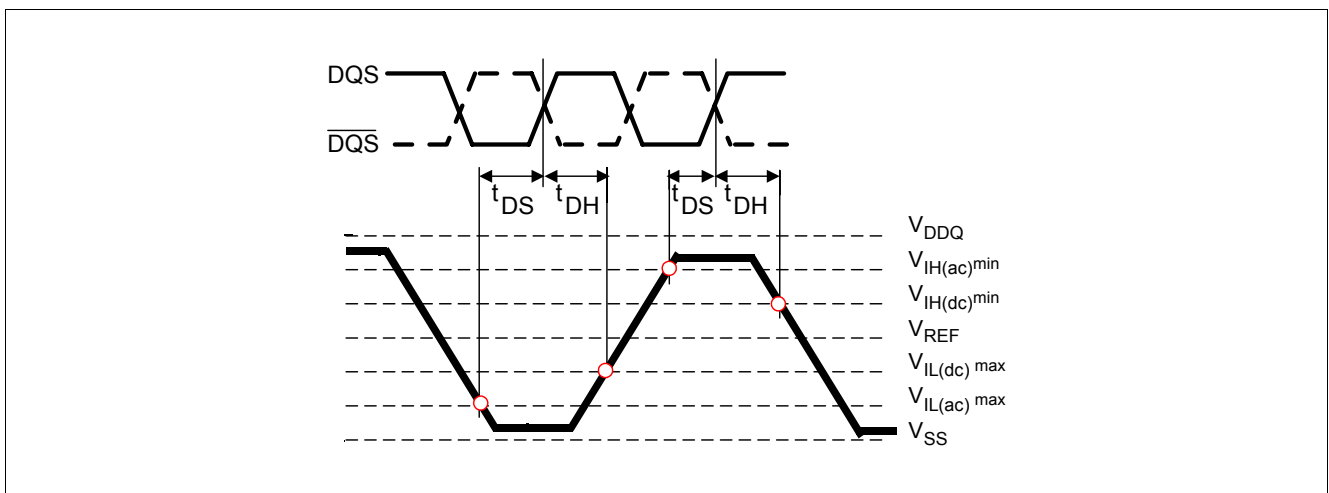


Figure 69 Data Setup and Hold Time (Differential Data Strobes)

8.3.3 Definition for Data Setup (t_{DS1}) and Hold Time (t_{DH1}), Single-Ended Data Strobes

Data input setup time (t_{DS1}) with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a falling signal applied to the device under test.

Data input hold time (t_{DH1}) with single-ended data strobe enabled MR[bit10]=1, is referenced from the input

signal crossing at the $V_{IH(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a rising signal and from the input signal crossing at the $V_{IL(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the end of its transition for a falling signal applied to the device under test.

The DQS signal must be monotonic between $V_{IL(dc)max}$ and $V_{IH(dc)min}$.

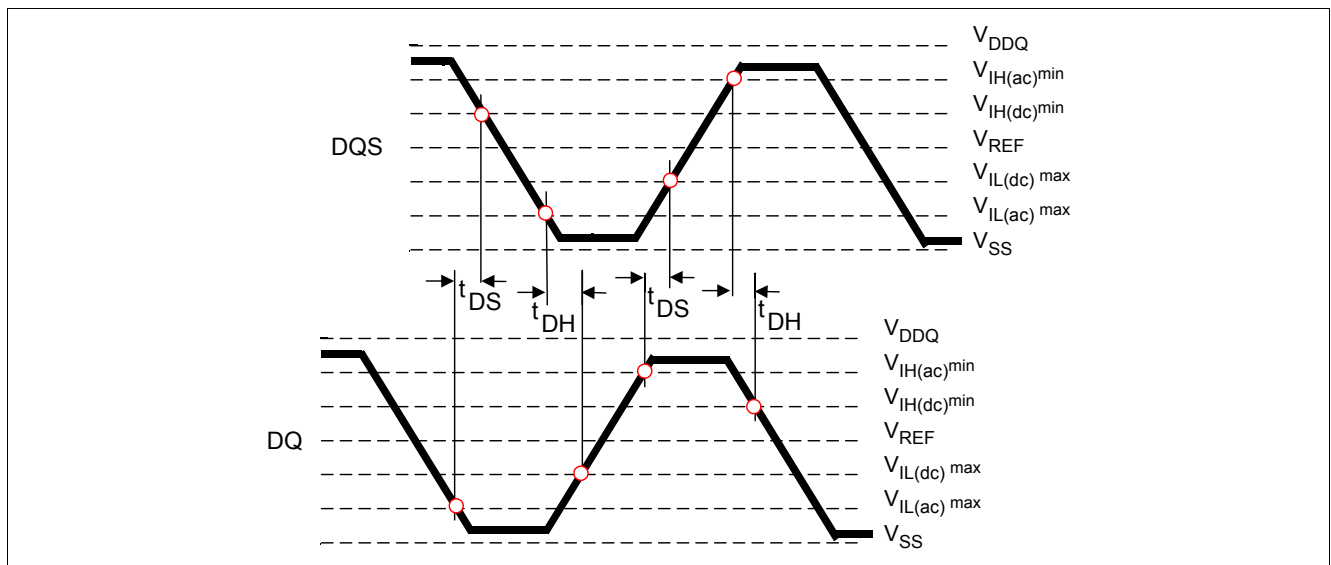


Figure 70 Data Setup and Hold Time (Single Ended Data Strobes)

8.3.4 Slew Rate Definition for Input and Data Setup and Hold Times

Setup (t_{IS} & t_{DS}) nominal Slew Rate for a rising signal is defined as the Slew Rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)min}$. Setup (t_{IS} & t_{DS}) nominal Slew Rate for a falling signal is defined as the Slew Rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)max}$. If the actual signal is always earlier than the nominal Slew Rate line between shaded 'V_{REF(dc)} to ac region', use nominal Slew Rate for derating value (see Figure 71). If the actual signal is later than the nominal Slew Rate line anywhere between shaded 'V_{REF(dc)} to ac region', the Slew Rate of a tangent line to the actual signal from the ac level to dc

level is used for derating value.(see Figure 72) Hold (t_{IH} & t_{DH}) nominal Slew Rate for a rising signal is defined as the Slew Rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH} & t_{DH}) nominal Slew Rate for a falling signal is defined as the Slew Rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal Slew Rate line between shaded 'dc to V_{REF} region', use nominal Slew Rate for derating value (see Figure 71). If the actual signal is earlier than the actual signal from the dc level to V_{REF} level is used for derating value (see Figure 72)

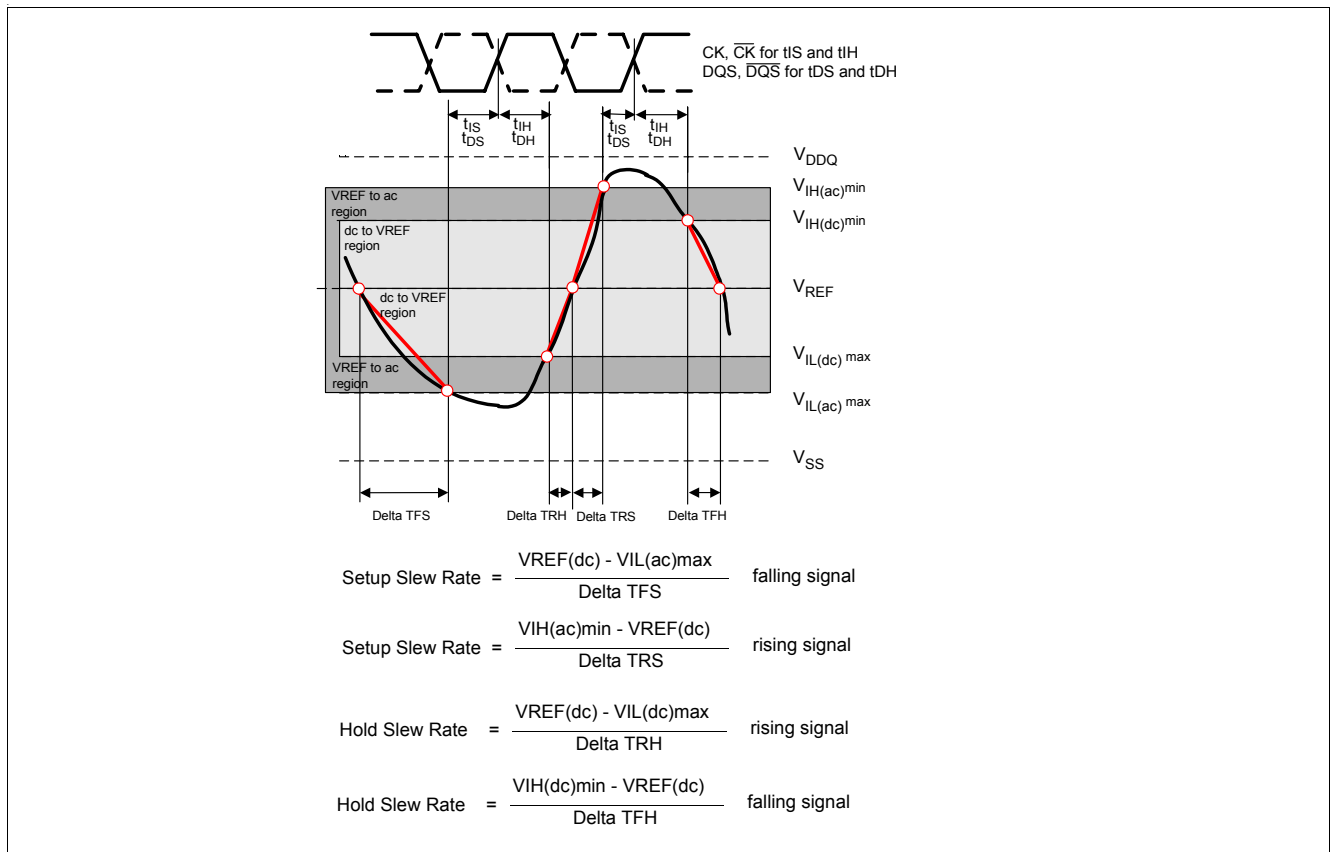


Figure 71 Slew Rate Definition Nominal

AC Timing Measurement Conditions

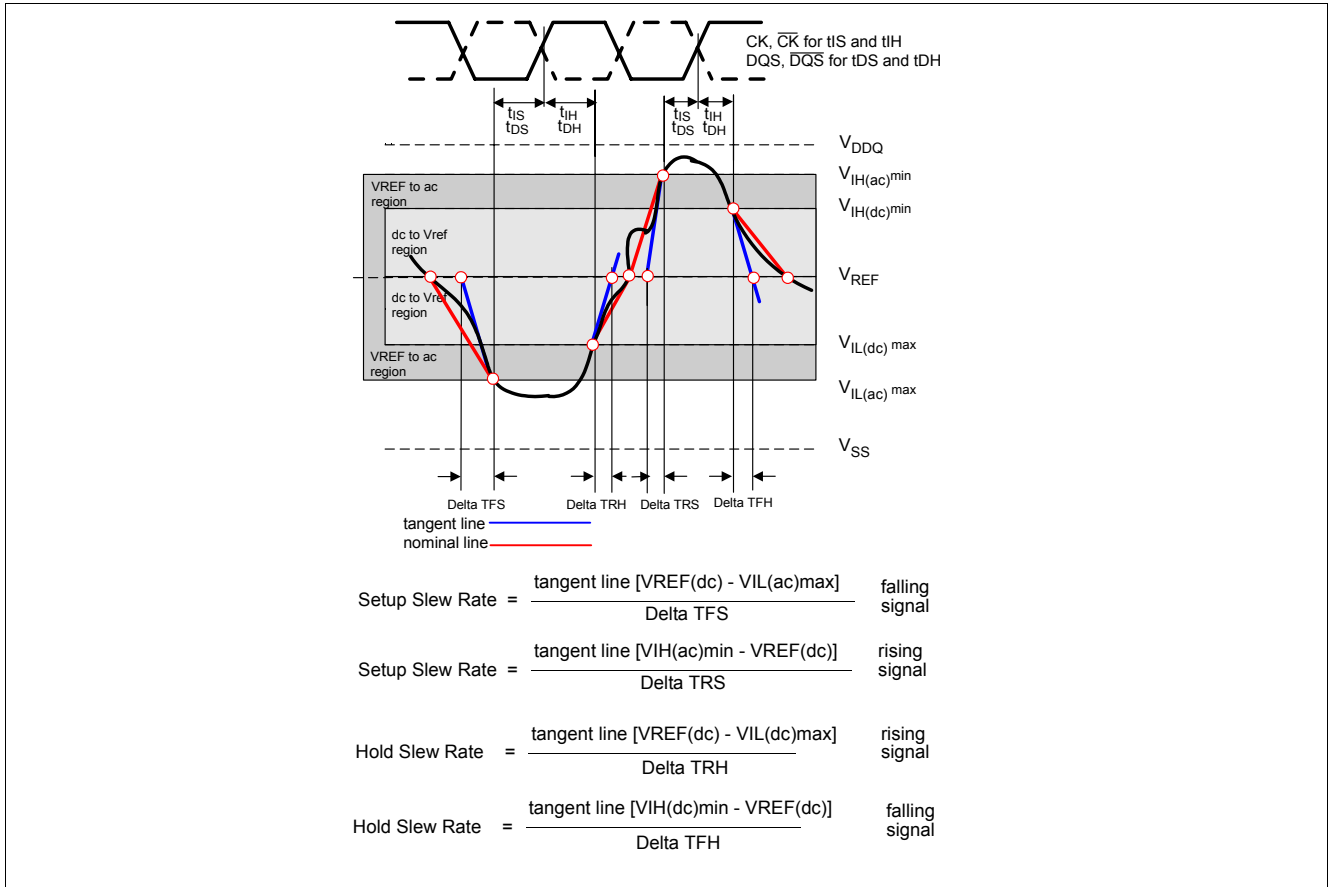


Figure 72 Slew Rate Definition Tangent

AC Timing Measurement Conditions

8.3.5 Setup (t_{IS}) and Hold (t_{IH}) Time Derating Tables

- For all input signals the total input setup time and input hold time required is calculated by adding the data sheet value to the derating value respectively.
Example: $t_{IS}(\text{total setup time}) = t_{IS}(\text{base}) + \Delta t_{IS}$
- For slow Slew Rate the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH(ac)} / V_{IL(ac)}$ at the time of the rising clock) a valid input signal is still required to complete the transition and reach $V_{IH(ac)} / V_{IL(ac)}$. For Slew Rates in between the values listed in the next tables, the derating values may be obtained by linear interpolation. These values are not subject to production test. They are verified only by design and characterization.

Table 44 Input Setup (t_{IS}) and Hold (t_{IH}) Time Derating Values

| Command / Address Slew Rate (V/ns) | CK, \overline{CK} Differential Slew Rate | | | | | | Unit | Note |
|------------------------------------|--|-----------------|-----------------|-----------------|-----------------|-----------------|------|------|
| | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | | |
| | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | Δt_{IS} | Δt_{IH} | | |
| 4.0 | +187 | +94 | +217 | +124 | +247 | +154 | ps | 1) |
| 3.5 | +179 | +89 | +209 | +119 | +239 | +149 | ps | 1) |
| 3.0 | +167 | +83 | +197 | +113 | +227 | +143 | ps | 1) |
| 2.5 | +150 | +75 | +180 | +105 | +210 | +135 | ps | 1) |
| 2.0 | +125 | +45 | +155 | +75 | +185 | +105 | ps | 1) |
| 1.5 | +83 | +21 | +113 | +51 | +143 | +81 | ps | 1) |
| 1.0 | 0 | 0 | +30 | +30 | +60 | +60 | ps | 1) |
| 0.9 | -11 | -14 | +19 | +16 | +49 | +46 | ps | 1) |
| 0.8 | -25 | -31 | +5 | -1 | +35 | +29 | ps | 1) |
| 0.7 | -43 | -54 | -13 | -24 | +17 | +6 | ps | 1) |
| 0.6 | -67 | -83 | -37 | -53 | -7 | -23 | ps | 1) |
| 0.5 | -110 | -125 | -80 | -95 | -50 | -65 | ps | 1) |
| 0.4 | -175 | -188 | -145 | -158 | -115 | -128 | ps | 1) |
| 0.3 | -285 | -292 | -255 | -262 | -225 | -232 | ps | 1) |
| 0.25 | -350 | -375 | -320 | -345 | -290 | -315 | ps | 1) |
| 0.2 | -525 | -500 | -495 | -470 | -465 | -440 | ps | 1) |
| 0.15 | -800 | -708 | -770 | -678 | -740 | -648 | ps | 1) |
| 0.1 | -1450 | -1125 | -1420 | -1095 | -1390 | -1065 | ps | 1) |

1) For all input signals $t_{IS}(\text{total}) = t_{IS}(\text{base}) + \Delta t_{IS}$ and $t_{IH}(\text{total}) = t_{IH}(\text{base}) + \Delta t_{IH}$

AC Timing Measurement Conditions

Table 45 Data Setup (t_{DS}) and Hold Time (t_{DH}) Derating Values for Differential DQS/ \overline{DQS} ¹⁾²⁾

| DQ Slew Rate (V/ns) | DQS, \overline{DQS} Differential Slew Rate | | | | | | | | | | | | | | | | | |
|---------------------|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | | 0.8 V/ns | |
| | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} | Δt_{DS} | Δt_{DH} |
| 2.0 | +125 | +45 | +125 | +45 | +125 | +45 | — | — | — | — | — | — | — | — | — | — | — | — |
| 1.5 | +83 | +21 | +83 | +21 | +83 | +21 | +95 | +33 | — | — | — | — | — | — | — | — | — | — |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | +12 | +12 | +24 | +24 | — | — | — | — | — | — | — | — |
| 0.9 | — | — | -11 | -14 | -11 | -14 | +1 | -2 | +13 | +10 | +25 | +22 | — | — | — | — | — | — |
| 0.8 | — | — | — | — | -25 | -31 | -13 | -19 | -1 | -7 | +11 | +5 | +23 | +17 | — | — | — | — |
| 0.7 | — | — | — | — | — | — | -31 | -42 | -19 | -30 | -7 | -18 | +5 | -6 | +17 | +6 | — | — |
| 0.6 | — | — | — | — | — | — | — | — | -43 | -49 | -31 | -47 | -19 | -35 | -7 | -23 | +5 | -11 |
| 0.5 | — | — | — | — | — | — | — | — | — | — | -74 | -89 | -62 | -77 | -50 | -65 | -38 | -53 |
| 0.4 | — | — | — | — | — | — | — | — | — | — | — | — | -127 | -140 | -115 | -128 | -103 | -116 |

1) All units in ps.

2) For all input signals $t_{DS}(\text{total}) = t_{DS}(\text{base}) + \Delta t_{DS}$ and $t_{DH}(\text{total}) = t_{DH}(\text{base}) + \Delta t_{DH}$

Table 46 Data Setup (t_{DS}) and Hold Time (t_{DH}) Derating Values for Single Ended DQS¹⁾²⁾³⁾

| DQ Slew Rate (V/ns) | DQS Single-ended Slew Rate | | | | | | | | | | | | | | | | | |
|---------------------|----------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | 0.9 V/ns | | 0.8 V/ns | | 0.7 V/ns | | 0.6 V/ns | | 0.5 V/ns | | 0.4 V/ns | |
| | Δt_{D1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} | Δt_{DS1} | Δt_{DH1} |
| 2.0 | +125 | +45 | +125 | +45 | +125 | +45 | - | - | - | - | - | - | - | - | - | - | - | - |
| 1.5 | +83 | +21 | +83 | +21 | +83 | +21 | +95 | +33 | - | - | - | - | - | - | - | - | - | - |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | +12 | +12 | +24 | +24 | - | - | - | - | - | - | - | - |
| 0.9 | - | - | -11 | -14 | -11 | -14 | +1 | -2 | +13 | +10 | +25 | +22 | - | - | - | - | - | - |
| 0.8 | - | - | - | - | -25 | -31 | -13 | -19 | -1 | -7 | +11 | +5 | +23 | +17 | - | - | - | - |
| 0.7 | - | - | - | - | - | - | -31 | -42 | -19 | -30 | -7 | -18 | +5 | -6 | +17 | +6 | - | - |
| 0.6 | - | - | - | - | - | - | - | - | -43 | -49 | -31 | -47 | -19 | -35 | -7 | -23 | +5 | -11 |
| 0.5 | - | - | - | - | - | - | - | - | - | - | -74 | -89 | -62 | -77 | -50 | -65 | -38 | -53 |
| 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | - | -127 | -140 | -115 | -128 | -103 |

1) All units in ps.

2) For all input signals $t_{DS1}(\text{total}) = t_{DS1}(\text{base}) + \Delta t_{DS1}$ and $t_{DH1}(\text{total}) = t_{DH1}(\text{base}) + \Delta t_{DH1}$

3) For slow Slew Rate the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH(ac)} / V_{IL(ac)}$ at the time of the rising DQS) a valid input signal is still required to complete the transition and reach $V_{IH(ac)} / V_{IL(ac)}$. For Slew Rates in between the values listed in the table, the derating values may be obtained by linear interpolation. These values are not subject to production test. They are verified only by design and characterization.

9 Package Dimensions

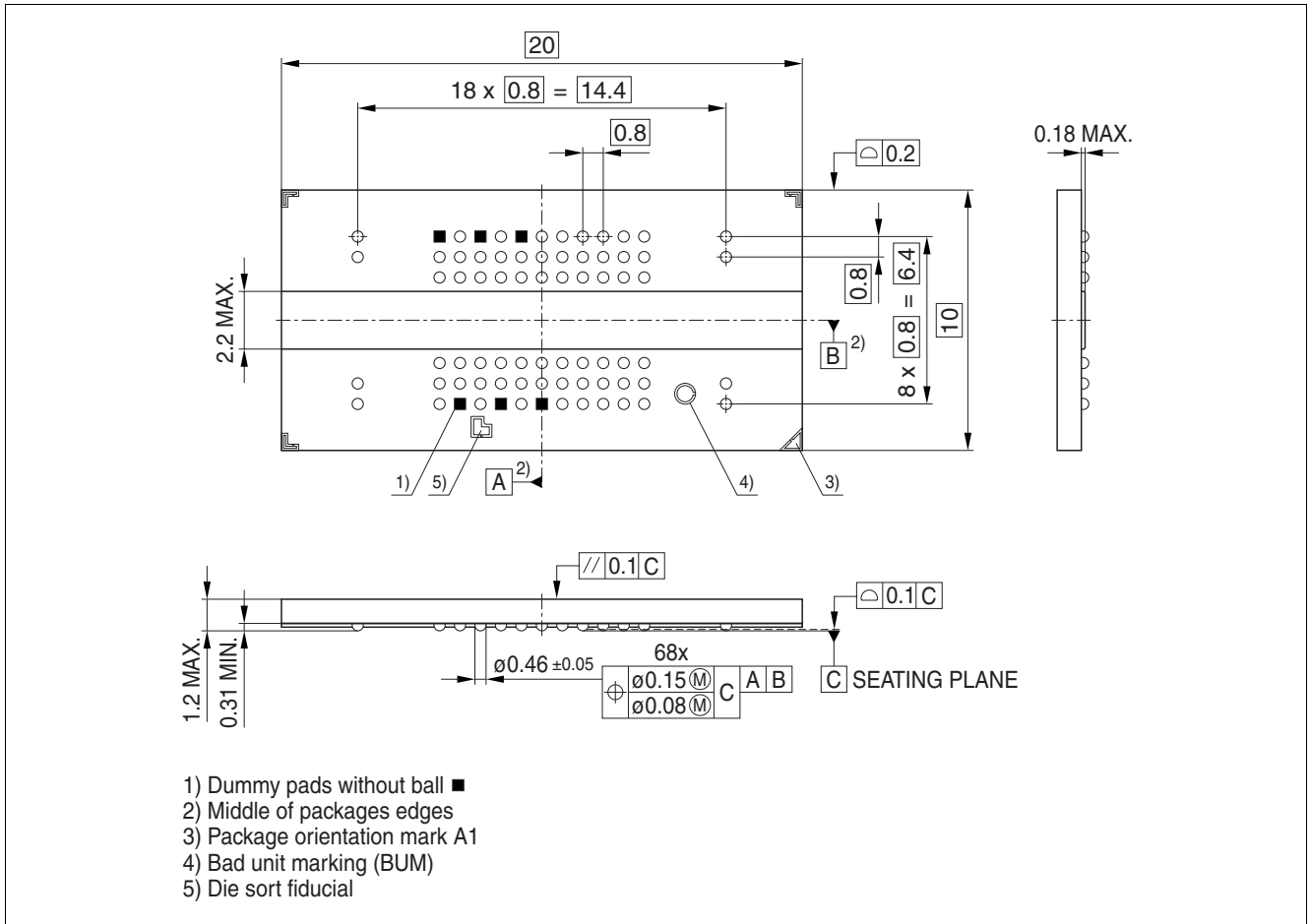


Figure 73 Package Pinout P-TFBGA-68 (top view)

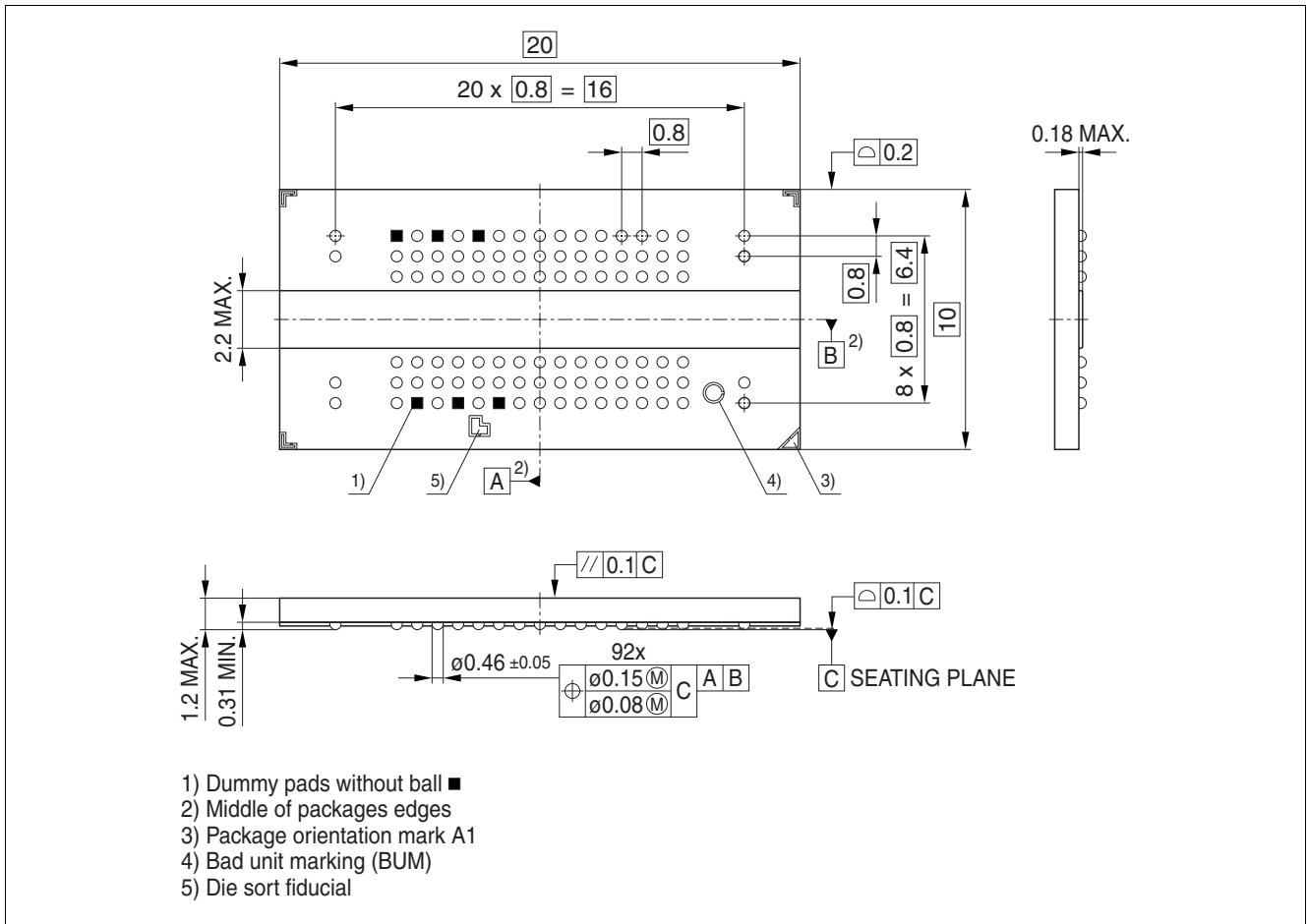


Figure 74 Package Pinout P-TFBGA-92 (top view)

10 DDR2 Component Nomenclature

Table 47 Nomenclature Fields and Examples

| Example for | Field Number | | | | | | | | | | |
|-------------|--------------|----|---|----|----|---|---|---|---|----|----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| DDR2 DRAM | HYB | 18 | T | 1G | 16 | | 0 | A | C | -5 | |

Table 48 DDR2 DRAM Nomenclature

| Field | Description | Values | Coding |
|-------|---------------------------|--------|-----------------------|
| 1 | INFINEON Component Prefix | HYB | Constant |
| 2 | Interface Voltage [V] | 18 | SSTL1.8 |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Component Density [Mbit] | 256 | 256 Mbit |
| | | 512 | 512 Mbit |
| | | 1G | 1 Gbit |
| | | 2G | 2 Gbit |
| 5+6 | Number of I/Os | 40 | ×4 |
| | | 80 | ×8 |
| | | 16 | ×16 |
| 7 | Product Variations | 0 .. 9 | look up table |
| 8 | Die Revision | A | First |
| | | B | Second |
| 9 | Package, Lead-Free Status | C | FBGA, lead-containing |
| | | F | FBGA, lead-free |
| 10 | Speed Grade | -3.7 | DDR2-533 |
| | | -5 | DDR2-400 |
| 11 | N/A for Components | | |

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