M54958FP

400MHz DUAL PLL FREQUENCY SYNTHESIZER

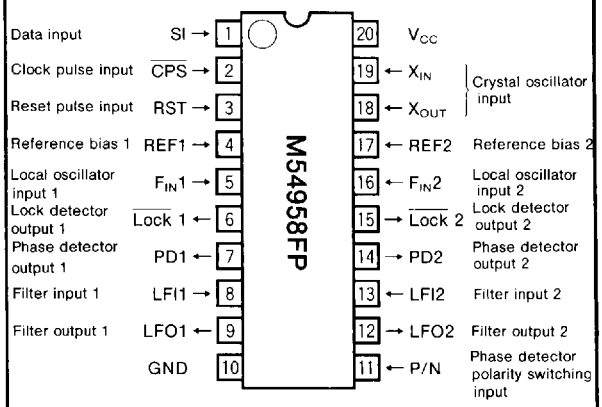
DESCRIPTION

M54958FP is a 400MHz band 2 system 1 chip PLL frequency synthesizer. Since PLL with 2 systems is incorporated, it is optimum for cordlessphone, dual band transceiver, etc. Two modulus prescalers of 1/128 and 1/129 are incorporated, and direct input of maximum 400MHz is available.

FEATURES

- PLL with 2 systems is incorporated.
- 1/128 and 1/129 prescalers are incorporated (fmax = 400MHz).
- Wide range of operating voltage (V_{CC}=3.0V~5.5V)
- Low current consumption
  When the two systems of PLL are operating :
  When one of them is not operating :
  When both of them are not operating :
- Divider for reference frequency is also programmable.
  Setting range of dividing ratio N (f_{REF}) = 128~16,376)
  (Can be set by multiples of 8.)
- Programmable divider for local oscillator
  Setting range of dividing ratio N (V. C. O) = 16,384~131,071 (Can be set by integral multiples.)
- Serial data input system (3 data transmission lines)
- PLL lock/unlock status indication function

PIN CONFIGURATION (TOP VIEW)



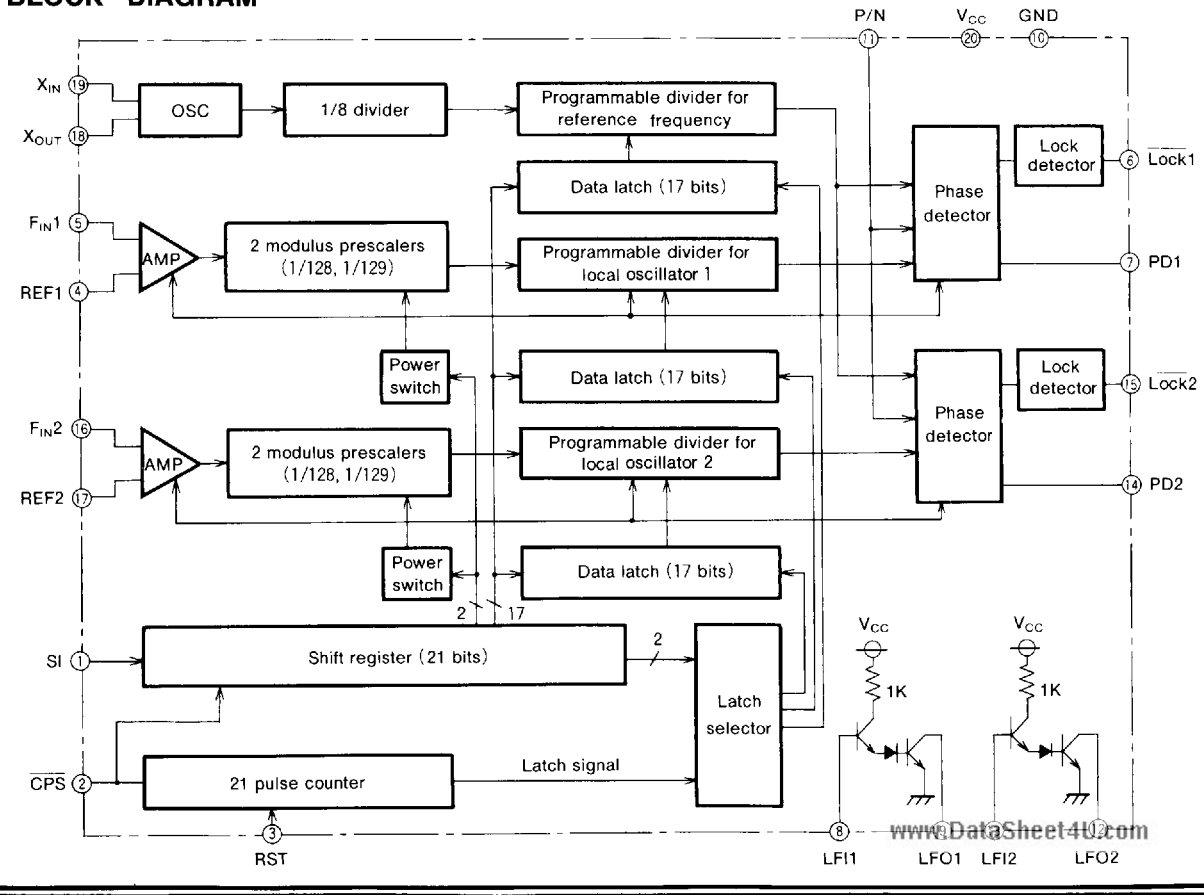
Outline 20P2N

- Power on/off of 2 system PLL can be set independently by transmitted data from controller.
- Two transistor circuits for LPF are incorporated.

APPLICATION

Cordlessphone, wirelessphone, etc.

BLOCK DIAGRAM

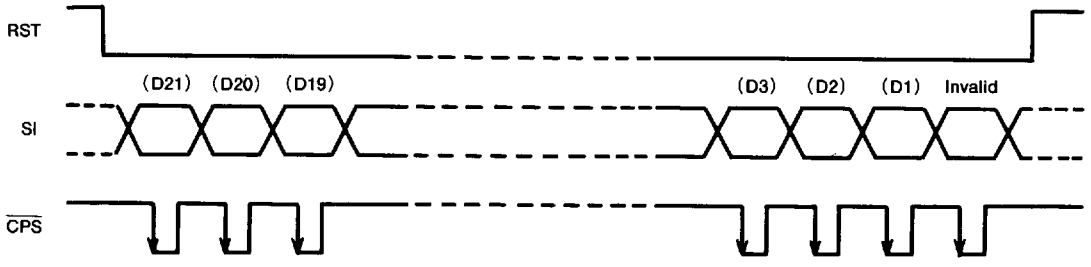


PIN DESCRIPTION

Pin no.	Symbol	Pin name	Description
1	SI	Data input	Data input terminal of shift register
2	$\overline{CPS}$	Clock pulse input	Clock pulse input terminal of shift register
3	RST	Reset pulse input	Reset pulse input terminal of 21 pulse counter
4	REF1	Reference bias 1	Grounded with 1000pF condenser.
5	$F_{IN}1$	Local oscillator input 1	Local oscillator frequency (V. C. O.) input fmax = 400MHz
6	$\overline{Lock}1$	Lock detector output 1	When PLL system is locked ··· "L" When it is unlocked ··· "H" Open Collector. Unsteady when the power of PLL1 is off.
7	PD1	Phase detector output 1	Tristate output
8	LFI1	Filter input 1	Base input of transistor for LPF
9	LFO1	Filter output 1	Collector output of transistor for LPF
10	GND	Ground	
11	P/N	Phase detector polarity switching terminal	When this terminal is at "H", PD terminal becomes "H" for phase lead and "L" for phase lag. When it is at "L", PD terminal becomes "L" for phase lead and "H" for phase lag.
12	LFO2	Filter output 2	Collector output of transistor for LPF
13	LFI2	Filter input 2	Base input of transistor for LPF
14	PD2	Phase detector output 2	Tristate output
15	$\overline{Lock}2$	Lock detector output 2	When PLL system is locked ··· "L" When it is unlocked ····· "H" Open collector. Unsteady when the power of PLL2 is off.
16	$F_{IN}2$	Local oscillator input 2	Local oscillator frequency (V. C. O.) input fmax = 400MHz
17	REF2	Reference bias 2	Grounded with 1000pF condenser.
18	X_{OUT}	Crystal oscillator input	Output from 12.8MHz reference oscillator is input to X_{IN}. Oscillator by external crystal resonator is available.
19	X_{IN}		
20	V_{CC}	Power terminal	3.0~5.5V

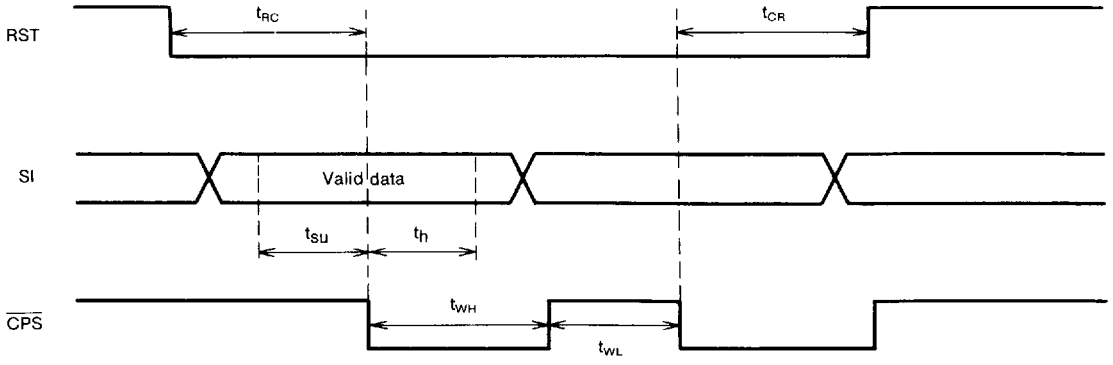
FUNCTION

1. DATA INPUT



Note 1 : SI input status is read into the shift register in sequence at the trailing edge of CPS input.
2 : All the data (power on/off, latch selector, Nvalue) is set at the trailing edge of the 21st pulse, and later CPS is invalid.
3 : Neither CPS nor SI is accepted while RST is at "H".

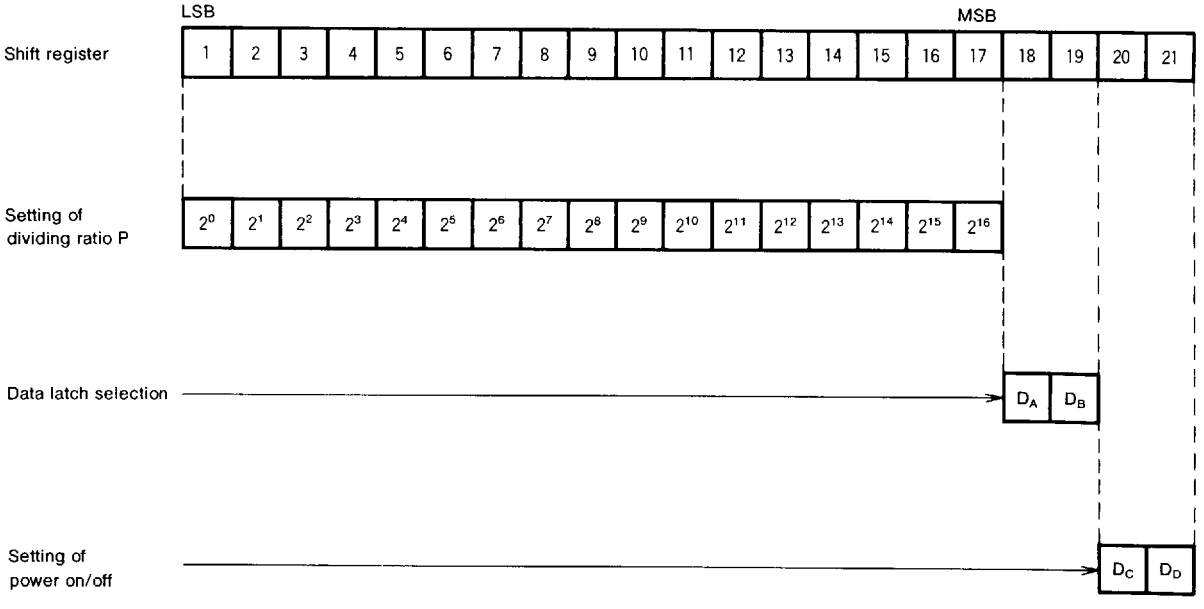
2. INPUT SIGNAL TIMING



$t_{SU}=t_h=t_{WH}=t_{WL}=10\mu S$ min.

$t_{RC}=t_{CR}=20\mu S$ min.

3. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Dividing ratio P of programmable divider is given in 17 bit binary code.
Total dividing ratio of reference freqency N (f_{REF}) is :
N (f_{REF}) $=8_XP$, where P=16~2,047
Total dividing ratio of local oscillator frequency N (V. C. O) is :
N (V. C. O) =P, where P=16,384~131,071

5 : Data latch to be updated is selected by D_A and D_B.

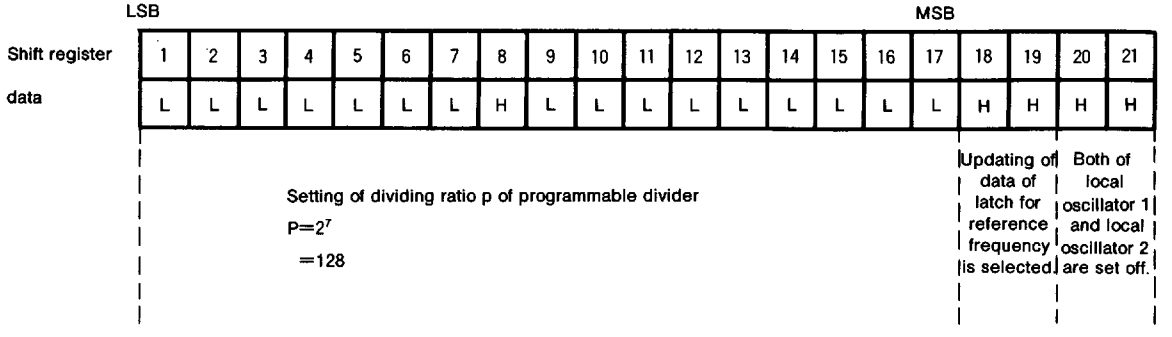
Data		Explanation
D_A	D_B	
L	L	This is for test mode.Do not use.
H	L	Data of latch for local oscillator 1 is updated.
L	H	Data of latch for local oscillator 2 is updated.
H	H	Data of latch for reference frequency is updated.

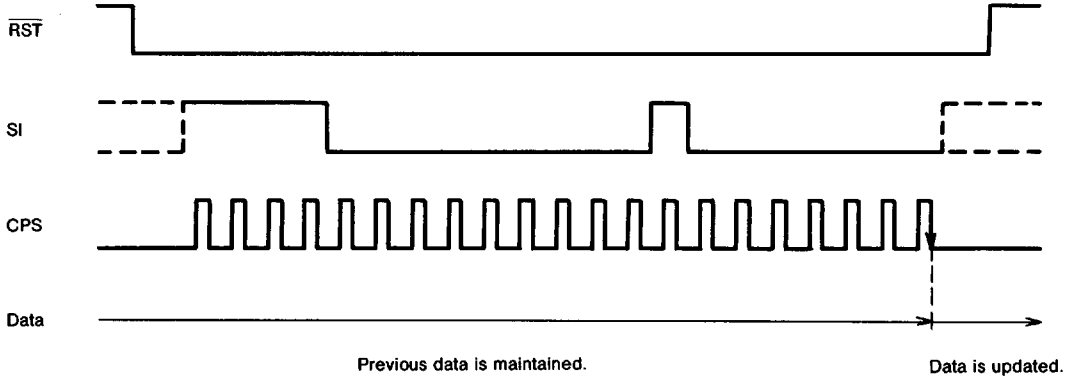
Note 6 : Power on/off of PLL system is set by D_C and D_D.

Data		Explanation
D_C	D_D	
L	L	On status of both systems of local oscillator 1 and local oscillator 2
H	L	On status of only local oscillator 1
L	H	On status of only local oscillator 2
H	H	Off status of both systems

4. DATA CODING EXAMPLE

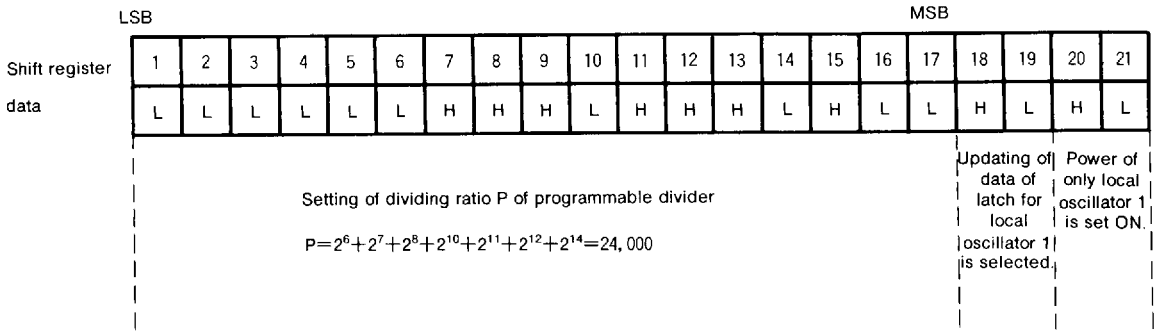
(1) Setting:reference frequency 12.5kHz, two systems of local oscillator 1 and local oscillator 2 off

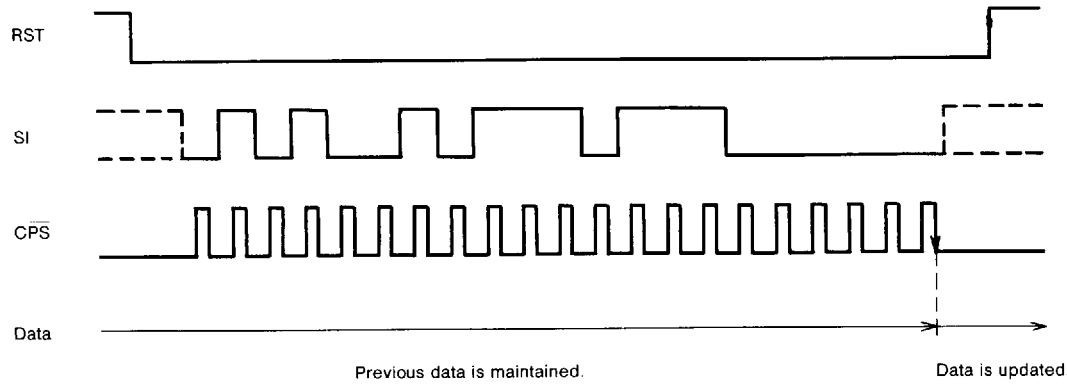




Note 7 : Total dividing ratio of reference frequency N (f_{REF}) is set at :
N (f_{REF})=8x P=8x128=1,024
When 12. 8MHz crystal oscillator is used,
f_{REF}=12,800/1,024=12.5kHz

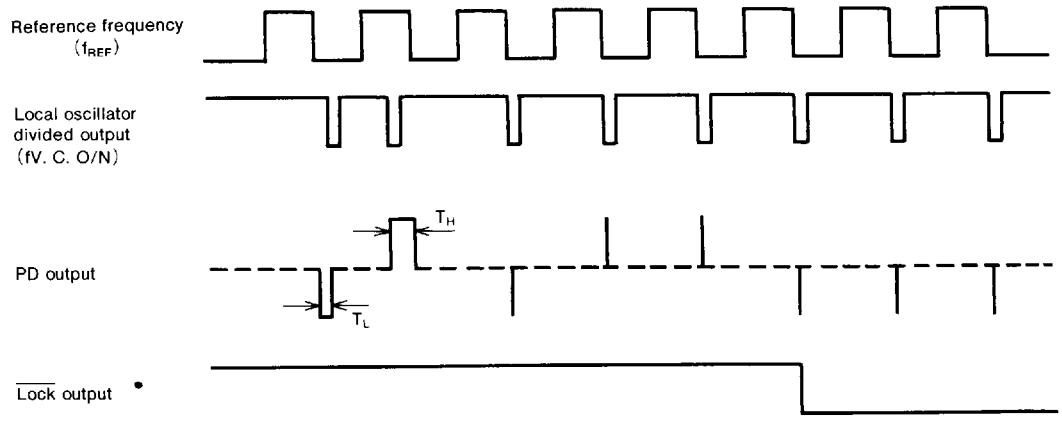
(2) Setting : dividing ratio of local oscillator 24,000, only local oscillator 1 ON





Note 8 : If PLL is locked when the reference frequency is set to 12.5kHz ;
fv. c. o. 1=12.5x24,000=300,000kHz=300MHz

5. PD, $\overline{\text{Lock}}$ SIGNAL DETECTION



Note 9 : PD output becomes "L" when the phase of local oscillator divided output (fv. c. o/N) is faster than that of reference frequency (f_{REF}) and "H" when it is behind.

10 : ·····indicates high impedance status.

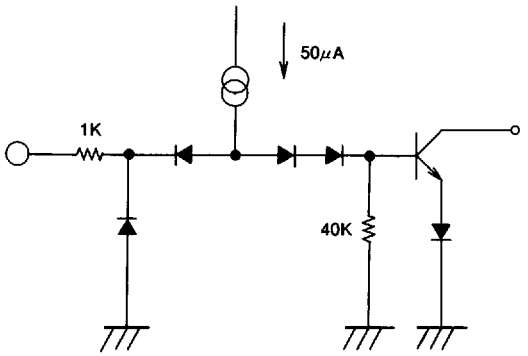
11 : Lock output becomes "L" when the phase differences T_L and T_H are kept below 625nS ** for more than three cycles of reference frequency (f_R).

* : The above explanation is the case when P/N input (11 pin) is at "H".
When P/N input is at "L", polarity of PD output is reversed.

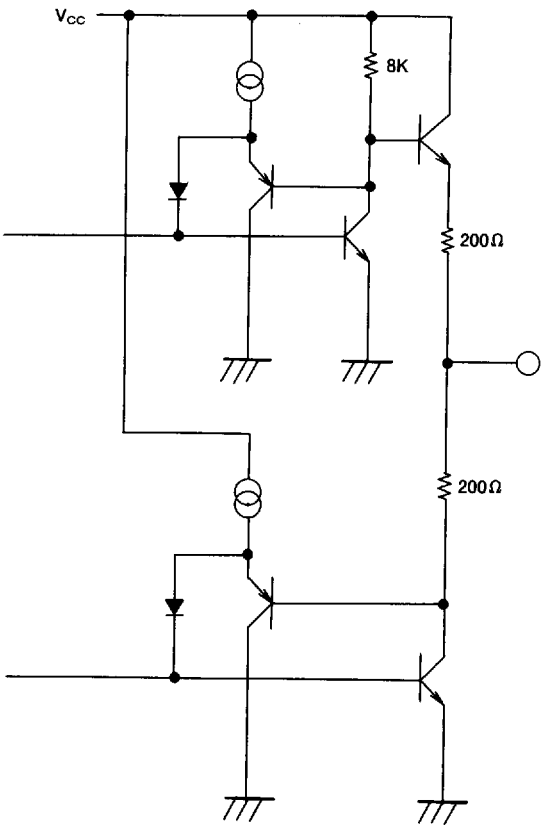
** : It is the case when 12.8MHz oscillator is used for reference oscillator frequency.

INPUT/OUTPUT CIRCUIT DRAWING

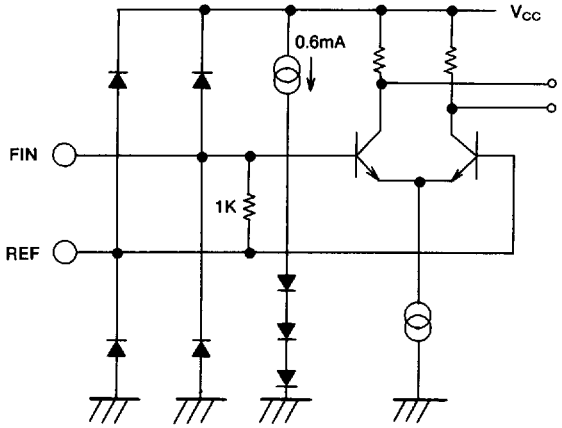
1 Each input of RST, $\overline{CPS}$, SI, and P/N



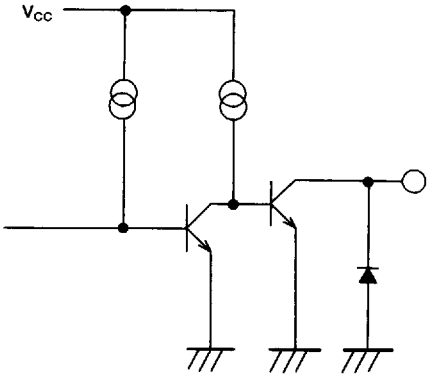
2 PD Output



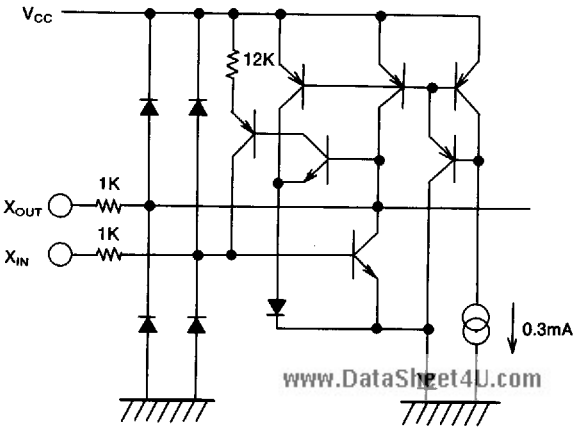
3 Each input of FIN and REF



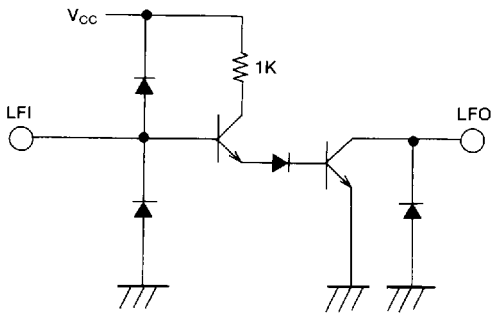
4 $\overline{Lock}$ Output



5 OSC Circuit



6 Circuit drawing of transistor for LPF



Note 12 : Resistance and power source are standard values when V_{CC}=5V and T_a=25℃.

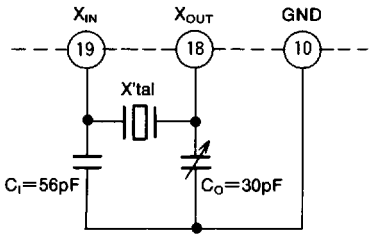
ABSOLUTE MAXIMUM RATINGS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min.	Max.		
V_{CC}	Supply voltage		−0.5	6.0	V	
V_I	Input voltage	Each input	−0.5	6.0	V	
V_O	Output voltage	Each output	−0.5	6.0	V	
Pd	Power dissipation	T_a=75℃		350	mW	Allowable power dissipation of package
Topr	Operating ambient temperature		−20	75	℃	
Tstg	Storing ambient temperature		−40	125	℃	

RECOMMENDED OPERATING CONDITIONS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	F_{IN}=80~400MHz	3.5		5.5	V	
		F_{IN}=200~400MHz	3.0		5.5		Transistor for LPF is external
V_{IN}	Input amplitude	F_{IN}= 80~400MHz	200		800	mVp-p	
F_{IN}	Input frequency	V_{CC}=3.5~5.5V	80		400	MHz	
		V_{CC}=3.0~5.5V	200		400		
I_{OL}	Low-level output current	Each output of Lock 1, Lock 2, LFO1 and LFO2			1	mA	
V_{XIN}	X_{IN} input amplitude	V_{CC}=3.0~5.5V, fosc=10~15MHz sine wave	0.5		2	V_{p-p}	15.2
fosc	Reference oscillator frequency	V_{CC}=3.0~5.5V, V_{XIN}=0.5~2Vp-p	10	12.8	15	MHz	15.2

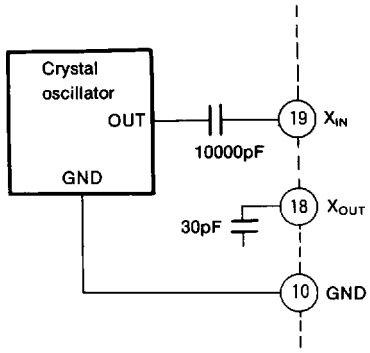
Connection of crystal oscillator



Load capacity of X'tal 20pF

Effective resistance 100Ω or less

Connection of crystal oscillator



ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Terminal	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=3.0~5.5V	2		5.5	V
V_{IL}	Low-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=3.0~5.5V	0		0.6	V
I_{IH}	High-level input current	SI, $\overline{CPS}$, RST, P/N	V_{CC}=5.5V, V_{IH}=5.5V			10	μA
I_{IL}	Low-level input current	SI, $\overline{CPS}$, RST, P/N	V_{CC}=5.5V, V_{IL}=0V		−30	−100	μA
V_{OL}	Low-level input voltage	$\overline{Lock\ 1}$, $\overline{Lock\ 2}$	V_{CC}=3.0V, I_{OL}=1mA			0.4	V
V_{OHP1}	PD High-level output voltage	PD1, PD2	V_{CC}=5V, I_{OH}=−1mA	3.5			V
V_{OHP2}	PD High-level output voltage	PD1, PD2	V_{CC}=3.0V, I_{OH}=−0.1mA	2			V
V_{OLP1}	PD Low-level output voltage	PD1, PD2	V_{CC}=5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD Low-level output voltage	PD1, PD2	V_{CC}=3.0V, I_{OL}=0.1mA			1	V
I_{PD1}	PD leak current	PD1, PD2	V_{CC}=5.5V, V_O=0.8V~4.7V			±1	μA
I_{PD2}	PD leak current	PD1, PD2	V_{CC}=5V, V_O=2.5V			±100	nA
I_{CC1}	Supply current	V_{CC}	V_{CC}=3V		20	45	mA
I_{CC2}			V_{CC}=5.5V		40	60	
I_{O1K}	Output leak current	$\overline{Lock\ 1}$, $\overline{Lock\ 2}$, LFO1, LFO2	V_{CC}=5.5V, V_{OH}=5.5V			5	μA
I_{BIAS}	Input bias current	LFI1, LFI2	V_{CC}=5V, I_C=1mA, V_C=2.5V			±1	μA
I_{CC3}	Supply current	V_{CC}	V_{CC}=3.5V, T_a=25℃		32	43	mA

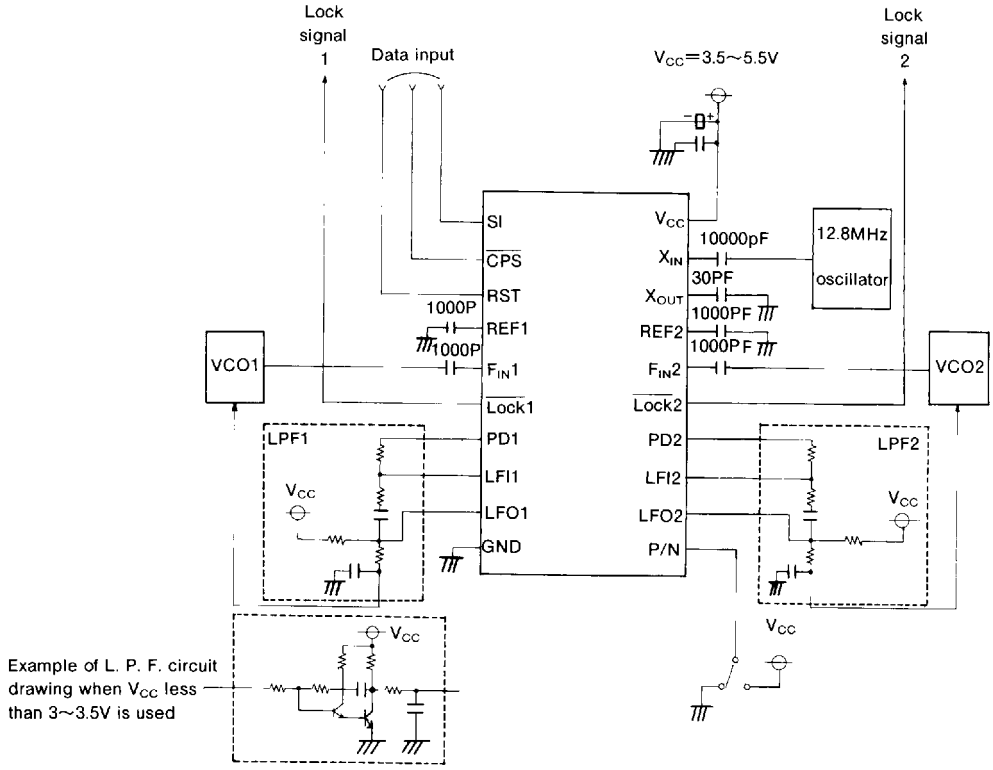
Note 13 : GND terminal (10 pin) of the circuit is the reference (0V) for all the voltages.

14 : Current flowing into the circuit is positive (no symbol) and that flowing out is negative (−symbol), and maximum and minimum values are indicated in absolute values.

15 : Typical value is that when T_a=25℃.

APPLICATION EXAMPLE

This application circuit drawing is for the circuit when V_{CC}=3.5~5.5V is used. When V_{CC} below 3.0~3.5V is used, provide a transistor for L. P. F externally.



HANDLING PRECAUTIONS

Elements of fine structure are used in this IC for higher function. Care should be taken so that surge voltage by static electricity is not applied to this IC.

20P2N Plastic 20pin 300mil(200mil body)SOP

Dimension in mm