Micro Linear

Application Note 44

Designing Fast Ethernet and FDDI-UTP Transceivers

OVERVIEW

The ML6673 is a complete monolithic transceiver for 125 Mbaud MLT-3 (Multi Level Threshold, 3 levels) encoded data transmission. The significance of this chip becomes evident when you consider today's requirement for wide-bandwidth transmission between computers and workstations. These computers, which may transmit applications involving color graphics, need high performance but a lower cost connectivity solution. The use of UTP (Unshielded Twisted Pair) reduces the cost of Fast Ethernet and FDDI networks by replacing expensive fiber optic cable and components with low cost copper wiring.

The key technical challenges in transmitting high speed data are controlling the emission and overcoming the bandwidth limitation of UTP. Therefore, in order to transmit data over UTP, the ANSI committee developed the X3T9.5 TP-PMD (twisted pair physical medium dependent) standard for twisted pair wiring. This standard allows the use of UTP category 5 and STP (Shielded Twisted Pair) cables. The TP-PMD standard applies to FDDI transmission over twisted pair. The TP-PMD standard was later adopted by the Fast Ethernet 100BASE-TX standard, IEEE 802.3. To achieve the high transfer rates three tasks must be performed: scrambling/descrambling, encoding/decoding and equalization. The latter two are performed by the ML6673.

The first requirement is a two level NRZI scrambling of the transmitted data. Once the data is scrambled to a two level NRZI and input to the chip, it gets converted to a multilevel threshold using the MLT-3. After the data has made its journey through the twisted pair, the receiver uses adaptive equalization to compensate for phase distortion and level attenuation. The data is subsequently converted back to NRZI format and descrambled.

This application note will define these terms and standards and explain the benefits of each in achieving a low cost, high performance copper twisted pair network.

MLT-3 LINE CODE

The MLT-3 code is used for Fast Ethernet and FDDI networks using copper media. MLT-3 is very similar to the NRZI (Non Return to Zero, Inverted) code used in the existing fiber FDDI network. NRZI, is a two level unipolar code (0 and V) representing a "one" by a transition between two levels and a "zero" is represented by no transition as shown in Figure 1. MLT-3 is a three level bipolar code (+V, 0 and –V) representing a "one" by a transition between two levels and "zero" as no transition as shown in Figure 1. Hence, the maximum fundamental frequency of the MLT-3 is one-half that of NRZI. Figure 2 shows the power spectral density for MLT-3 and NRZI. Essentially, the use of the MLT-3 line code shifts much of the spectral energy to below 30MHz (as compared to NRZI). With the MLT-3 coding scheme, 90% of the spectral energy is below 40MHz versus 70MHz for NRZI, which achieves the same data rate but does not require a wideband transmission medium.

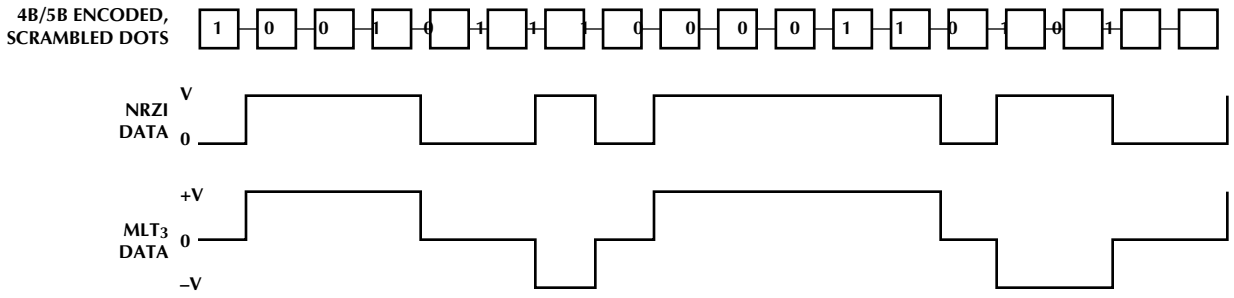


Figure 1. NRZI and MLT-3 Waveforms

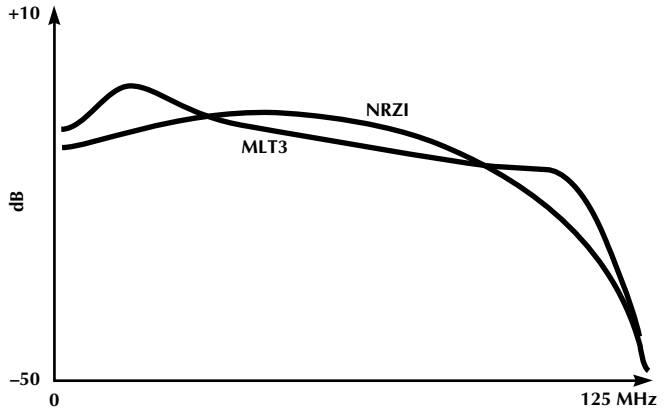


Figure 2. Power Density Spectra for NRZI and MLT-3

SCRAMBLING/DESCRAMBLING

In general, the robustness of a digital transmission system often depends on the statistical nature of the digital sources. For example, long strings of 0's and 1's can cause loss of the sychronization since the receiver clock is derived from the received data. Therefore, data must contain adequate transitions to assure that the timing recovery circuit will stay in sychronization.

The Fast Ethernet and FDDI protocols allow for some repetitive data patterns. These patterns create energy peaks in the power spectral density of the line signal. These peak discrete spectral components are not desirable and must be suppressed.

The utilization of scrambling spreads these patterns and suppresses discrete spectral components by 20 to 25dB. This is due to the effect of randomization of the data and averages out the signal over a period of time. Thus, the peak energy is eliminated and emission improved. The ANSI committee has chosen Stream-Cipher scrambling as the technique for the TP-PMD network. The Stream-Cipher scrambler encodes a plain text NRZ bit stream by addition (modulo 2) of a key stream to produce a cipher text bit stream. It is implemented by adding an 11 bit linear Feedback Shift Register (LFSR) whose input bit is the exclusive-OR of its 11th and 9th previous bit, and which contains at least one non-zero bit. The shift register generates the key stream sequence which can be added to valid plain text streams with an average run length of approximately two consecutive zeros and a maximum run length of approximately 60 consecutive zeros.

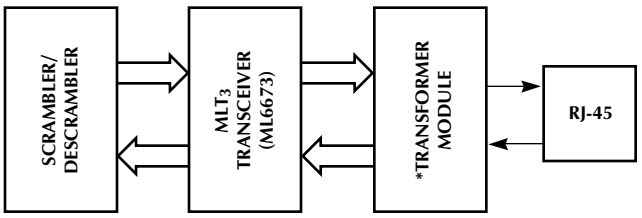
EQUALIZATION

During transmission of data over UTP distortion and ISI (intersymbol interference) are caused by dispersion in the cable. To overcome this signal corruption and distortion, the transmitted signal must be reconstructed from the incoming signal at the receiver. Equalization is used to overcome this signal corruption. However, the distortion is frequency dependent and loop length dependent. Since in most practical cases, the TP port characteristic is unknown and it is impractical to tune the equalizer specifically to each individual port. Hence, an adaptive equalizer is used in the TP-PMD standard to ensure proper compensation of the received signal.

By using an adaptive equalizer, the receiver automatically compensates for different lengths of cable without over equalizing or under-equalizing the line. The ML6673 monitors the energy of the received signal to determine the cable length and adjust the equalizer accordingly. The input signal level is inversely proportional to the cable length. Therefore, as the signal level decreases, the amount of equalization is increased to compensate for the line loss.

TP-PMD

The TP-PMD standard for Fast Ethernet and FDDI networks is intended to be a physical replacement of the ODL (Optical Data Link) transceiver. It contains a scrambler/descrambler, a MLT-3 transceiver (ML6673) and a transformer-common mode choke module as shown in Figure 3. NRZI coded data is sent to the TP-PMD and the TP-PMD transmits the 125Mbit/s MLT-3 coded data to the media. At the receive side, the MLT-3 coded data is received and equalized and then is converted into NRZI coded data.



*Contact Belfuse or, Valor, regarding Transformer Module
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Valor Phone: (619) 537-2619

Figure 3. Block Diagram of the TP-PMD

Transmit Function

The ML6673 receives an NRZI code bit stream, which is at positive differential ECL (PECL) levels at the TXIN inputs. PECL level scrambled NRZI data is received by the ML6673 and then converted into MLT-3 line code. The current driven transmitter then sends the data to the transformer/common-mode choke module. Since the output structure of the twisted pair drivers is current driven, it has the following advantages when driving the UTP medium:

- The differential outputs are well matched for balanced signal transmission. Balanced transmission is crucial for meeting tight regulations on signal shapes.
- Current driven outputs produce lower common-mode voltages for a lower EMI radiation. This can be a very significant issue in meeting FCC regulations.
- The output drive can be easily adjusted to compensate for losses in the transformer module.

An external resistor between pin 17 and 18, RTSET1 and RTSET2, sets the output level. The value of the resistor across pins 17 and 18 is as follows:

$$RTSET = \frac{64 \times 1.25}{I_{OUT}}$$

For FDDI UTP and Fast Ethernet applications, the ANSI X3T9.5 standard specifies the transmit voltage amplitude to be $2V_{P-P}$ or 1V ± 60mV. The UTP connection requires a termination impedance of 100Ω, each transmitter output is terminated by one 50Ω (R_L) resistor to provide the 100Ω termination impedance. Therefore,

$$I_{OUT} = \frac{2V(P-P)}{R_L} = \frac{2V}{50\Omega} = 40mA$$

The value of RTSET is

$$RTSET = \frac{64 \times 1.25}{40mA} = 2K$$

Using a 2K resistor sets the transmit level to $2V_{P-P}$ with 0dB loss at the transformer module and zero meter cable. If the transformer module attenuates the transmit signal level, the value of RTSET should be decreased to generate $2V_{P-P}$ signal after the transformer.

The transmitter may be disabled by the TXOFF pin When this pin is pulled low. Then, the transmitter's output goes to a high impedance state and shuts off transmit bias current.

Receive Function

The receive circuit of the ML6673 consists of an adaptive equalizer and MLT-3 to NRZI converter. The equalizer adjusts its gain and frequency response as a function of the received signal. The equalization level is based on the energy level of the received signal. As the signal level decreases, due to higher attenuation by a longer cable, the amount of equalization is increased. The equalizer is designed to operate over a distance of 0 to 100 meters of category 5 type cable.

The ML6673 detects the MLT-3 coded signal from the transformer module signal and activates the SD ± output signal when the input is above a preset the voltage level. This preset voltage threshold level is 25% of the maximum equalization setting.

After the signal is equalized, it is converted to NRZI. *The ML6673 sends data out in NRZI form.*

Link Status Function

The ML6673 monitors the line integrity and detects linkage with the signal detect circuit. A differential output pair SD± to the host indicates the status of the link. They are active when a data signal is presented with an amplitude exceeding a preset threshold. Otherwise, the signal detect circuit drives SD+ low and SD– high indicating an invalid link.

Loopback Function

Loopback is controlled through the LPBK pin coming from the PHY chip. When this pin is low, loopback is enabled and signal detect is asserted. During loopback, the transmitted data from TXIN± does not transmit to the TXOUT±. Instead it is looped back to the receive data RXOUT± by an internal mux.

TP-PMD CIRCUIT

Figure 4 shows a complete schematic of TP-PMD circuit using ML6673 with an external transformer module. This TP-PMD transceiver is designed to replace an existing 1408U ODL FDDI transceiver. The external resistors and capacitors are chosen to meet the following conditions:

ECL Line Terminations

RXOUT± and SD± are emitter-followers generating positive ECL (PECL) levels when terminated by a pair of resistors. The resistors form a thevinin equivalent 50Ω termination. The following two equations are used to calculate the values of these resistors:

$$R_b = 2.6 \times Z_O = 2.6 \times 50\Omega = 130\Omega$$

$$R_a = \frac{R_b}{1.6} = \frac{130\Omega}{1.6} = 81\Omega$$

The same concept applies to the TXIN± outputs coming from the PHY. RXOUT±, SD± and TXIN± are not terminated in the TP-PMD schematic since they are terminated at the other end in the adapter cards and concentrator boards.

Media Termination

Two 50Ω resistors at TPOUT± and TPIN± implement 100Ω terminating impedance for UTP when looking back through the filter-transformer module. The TPOUT± must be terminated by a 50Ω resistor to +5V.

Common Mode

The received signal coming from UTP at TPIN± must be biased by the CMREF pin as shown in the schematic. The transmitted signal from the TPOUT± is biased to +5V through the center top of the transformer module.

Equalizer and Link Detect Timings

The resistor across RRSET1 and RRSET2 sets the time constants controlling the equalizer's transfer function. A 5K, 1% resistor across these pins limits the cable length to 100 meters.

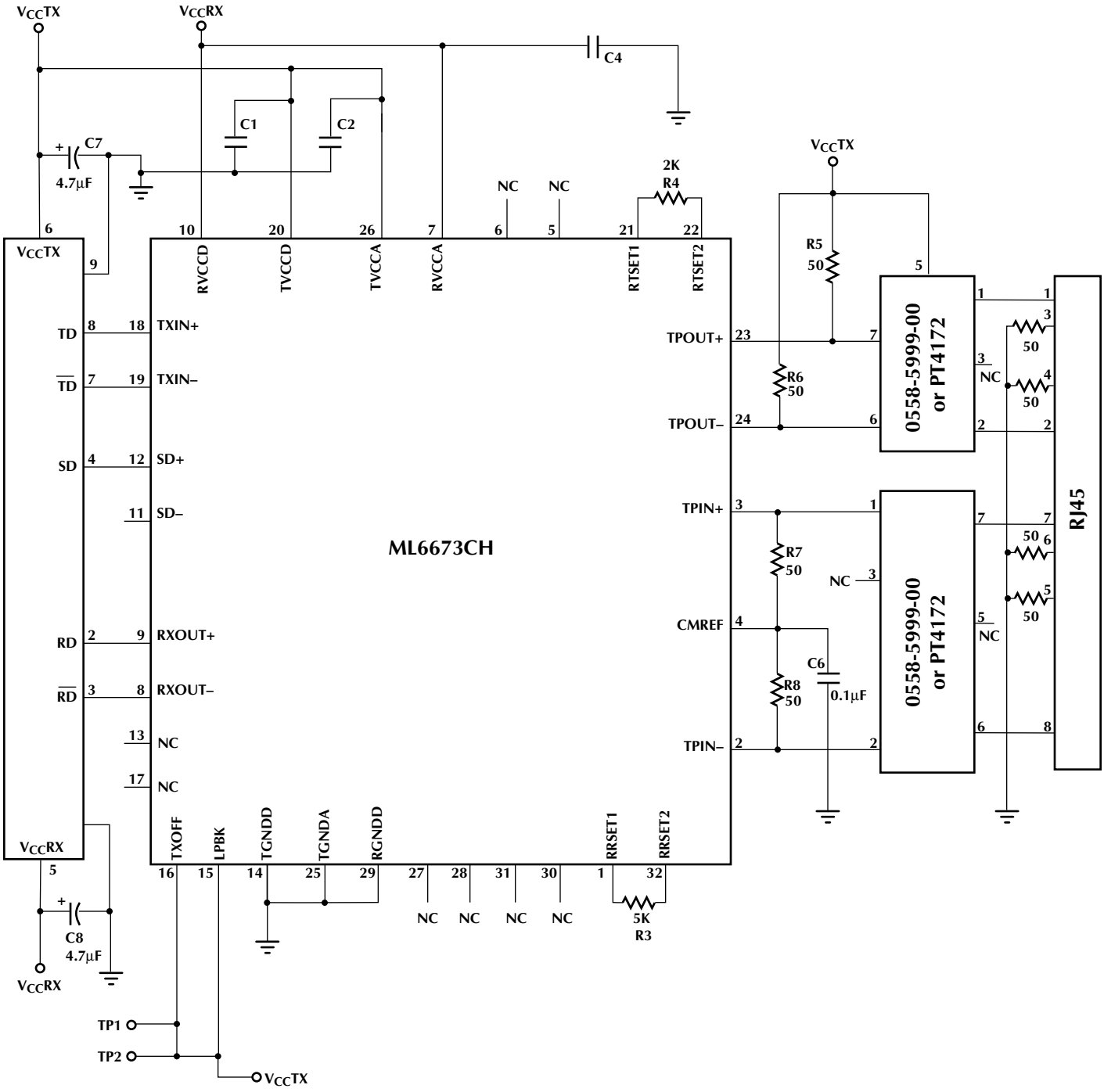

Figure 4. Schematic of the TP-PMD using the ML6673

PERFORMANCE DATA

The ML6673 can be evaluated in the ML6673EVAL board. The ML6673 evaluation board provides access to all receive and transmit signals and waveforms required to test and evaluate the ML6673. As shown in Figures 5 to 10, the ML6673 meets the standards for Fast Ethernet and FDDI.

Receive Waveforms

The ML6673 Evaluation board operates with different cable lengths. Figures 5 through 8 show the typical eye pattern of the NRZI signals at the RXOUT pin, which is recovered by the internal adaptive equalizer for different cable lengths. In all cases, the jitter is held below 2.0ns.

Also the ML6673 is capable of handling baseline wander generated by a different pattern. Baseline wander is the term used to describe what happens to the DC reference for a signal when voltage offsets cause the threshold to change. This issue occurs when a signal is being transmitted by using AC coupling to the transmission media, which, in this case, is twisted pair copper wire. This offset is what is called "baseline wander."

The TP-PMD standard defines a good symbol frame known as a killer frame in Annex A.2. The killer frame produces a near worst case baseline wander condition of approximately 750mV. Figures 9 and 10 show the typical eye pattern of the recovered NRZI data at the RXOUT pin for 0 (zero) and 117 meter cable lengths. In both cases the jitter is held below 2ns.

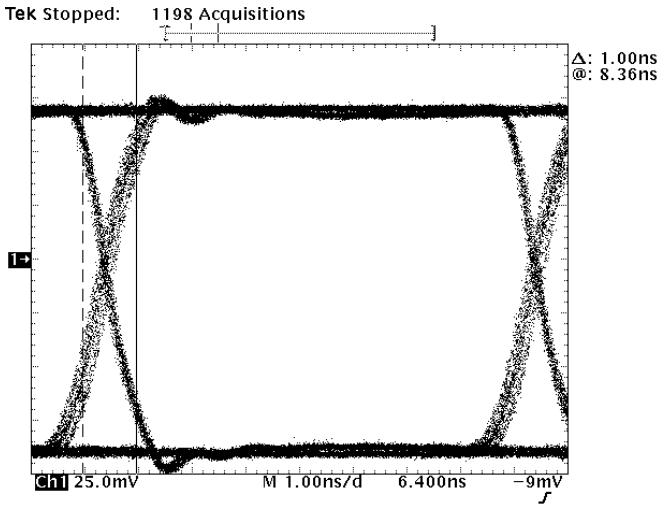

Figure 5. MLT Eye Pattern from the ML6673 EVAL Board (0 meter UTP cable)

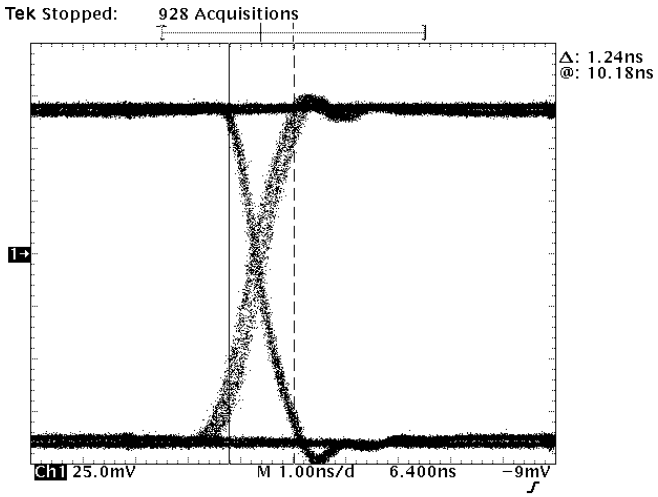

Figure 6. MLT Eye Pattern from the ML6673 EVAL Board (25 meters UTP cable)

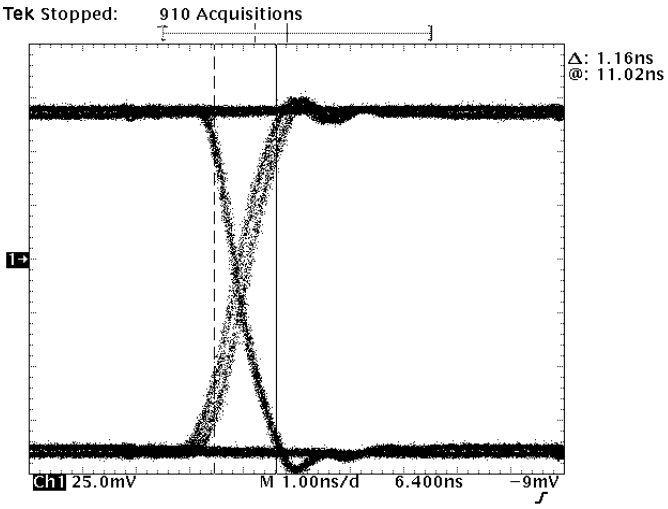

Figure 7. MLT Eye Pattern from the ML6673 EVAL Board (50 meters UTP cable)

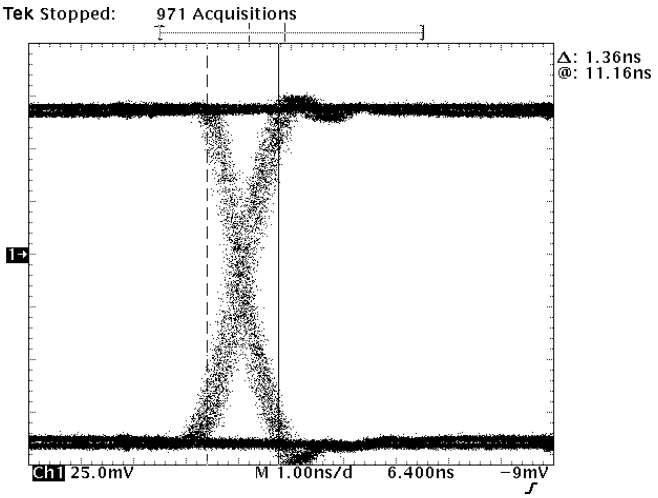

Figure 8. MLT-3 Eye Pattern from the ML6673 EVAL Board (117 meters UTP cable)

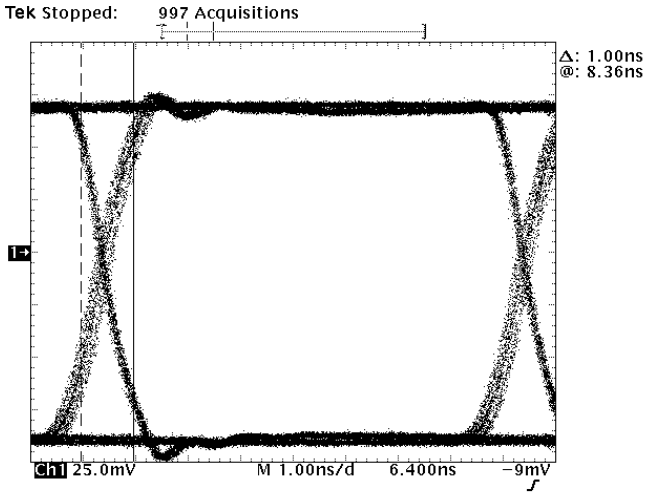

Figure 9. Recovered NRZI Data (killer frame) at the RXOUT Pin for 0 (zero) meter cable length.

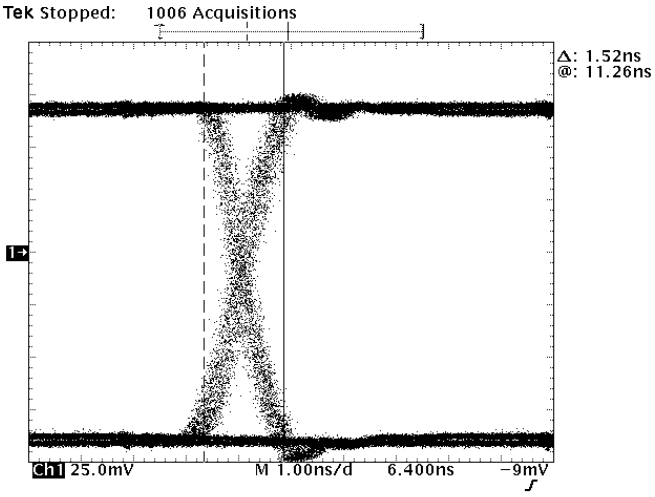

Figure 10. Recovered NRZI Data (killer frame) at the RXOUT Pin for 117 meters cable length.

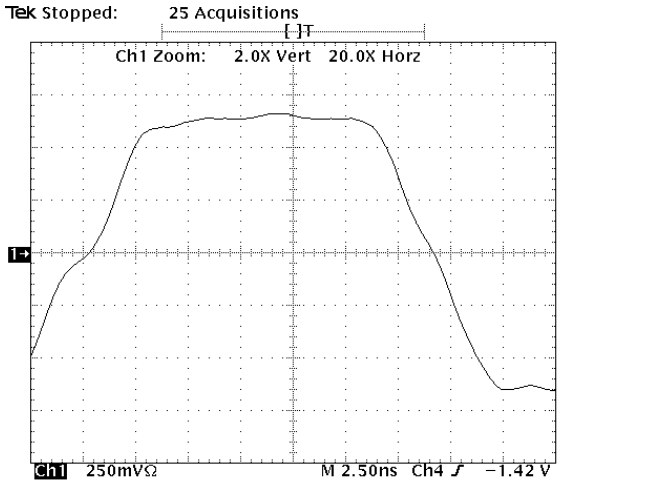

Figure 11. Rise and Fall Time of the Output Transmit Signal from the ML6673 EVAL Board.

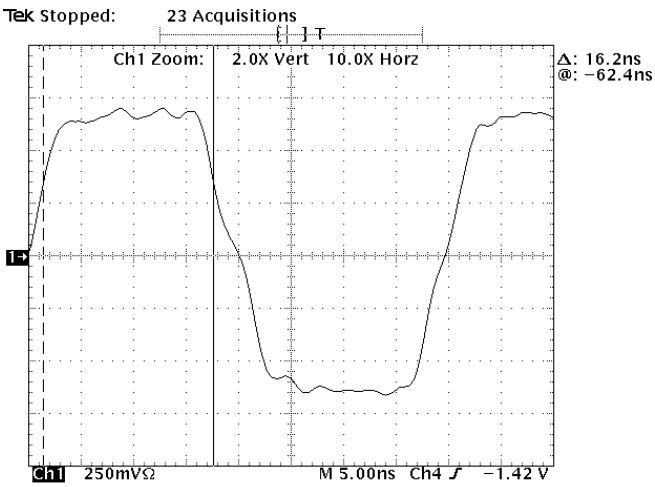

Figure 12. Duty Cycle Distortion of the Transmitter.

Transmit Waveforms

Typical rise time and fall time for the transmitted output after the transformer is approxiamately 2 to 3ns, as shown in Figure 11.

Duty cycle distortion (DCD) is measured at the 50% voltage points on the rise and fall transitions as shown in Figure 12. The 50% points at four successive transitions of MLT-3 are used when the binary bit sequence is 01010101. The deviations of the 50% crossing points from a best fit to a time grid of 16ns spacing does not exceed ±0.25ns.

LAYOUT CONSIDERATIONS

To obtain optimum performance from the TP-PMD transceiver, careful attention must be given to the layout of the board. The routing of sensitive input traces relative to other components and traces must be considered in great detail. Data lines must be of controlled impedance and properly terminated to minimize reflections that might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering. To achieve this, the following should be considered:

- Use a two layer printed wiring board with a large ground plane.
- Use enough decoupling capacitors on the receive, transmit, digital, and analog VCC pins of the ML6673 to clean up the noise. Locate these capacitors as close as possible to the appropriate pins of the ML6673.
- The receiver pins, and the traces connected to them, should be shielded by placing a ground trace between the pins, the traces and any other high-level paths to minimize the coupling of unwanted noise into the receiver. If shielding is not possible, route the transmitter-input traces and other traces carrying high-level signals as far as possible from the receiver pins.
- When laying out the traces for the data lines (TXD, RXOUT, SD), signal lines should be an overshoot, as well as to simplify timing considerations arising from the propagation delay of a signal conductor. Ringing and overshoot are due to the intrinsic inductance and capacitance at the end of the line. Intrinsic inductance and capacitance are reduced by shortening the lines. The same concept applies to the TPOUT and TPIN high speed input and output signal lines.
- Each ECL data line should be terminated at the end of the line. A bypass capacitor, 0.01 to 1µF, must be provided on the voltage side of the resistor for each termination resistor. The termination helps to minimize the reflection due to mismatch.
- Avoid controlled impedance interruption (i.e., 90° bends) on all high speed lines. PC traces should be treated as transmission lines with continuous ground plane or power plane beneath each line.
- All 50Ω termination resistors at TPOUT and TPIN should be placed as close as possible to the pins of the ML6673.
- Use the same +5V to pull up the two 50Ω resistors at the TPOUT± and the center tap of the transformer. Adding a decoupling capacitor at this point is recommended.
- To improve the EMI performance, terminate the unused pins of the RJ45. Different termination methods are available such as:

  a) Adding a 50Ω resistor to ground on each unused pin of RJ45.
  b) Adding an RC network on each unused pin to build a low pass filter, filtering high frequency components (higher than 40MHz).

- All paired lines (differential pairs) should be of equal length, especially TPOUT traces.
- The resistors across RTSET1 adn RTSET2 should be 2kΩ, 1% and close to the pins.
- A copy of the ML6673EVAL kit Gerber files is included on the 3.5" floppy disk as a reference.

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