DATA SHEET

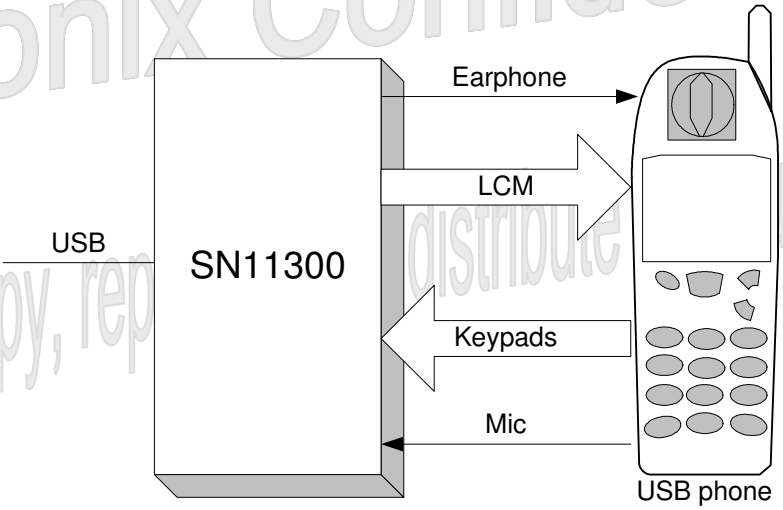
SN11300

3 In 1 USB Audio Controller

V1.3

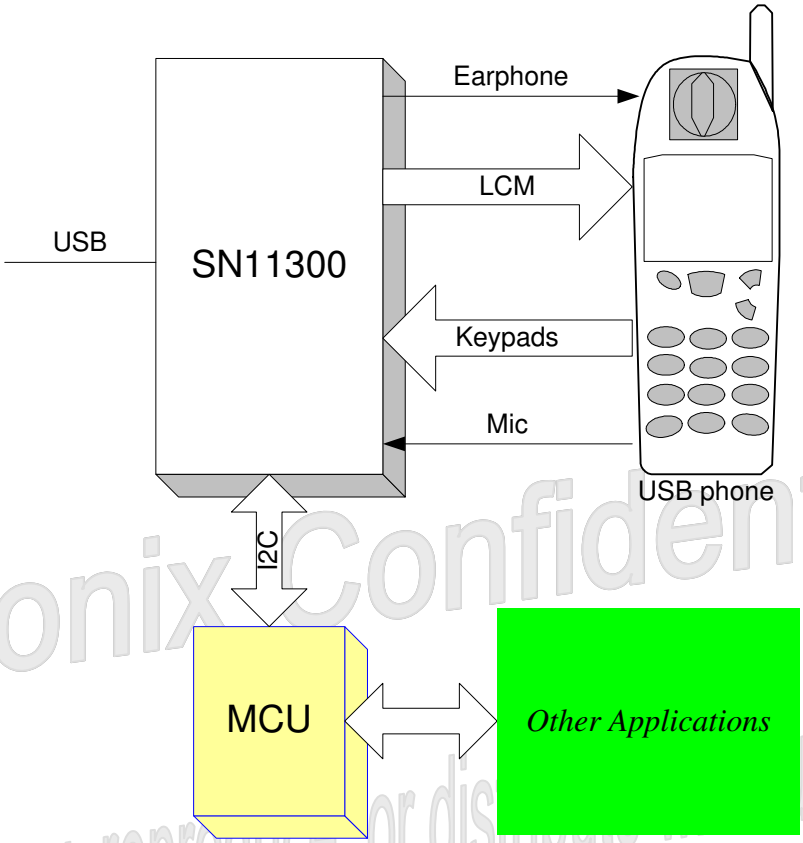
I. Description

SONiX SN11300 is a highly integrated single chip USB audio controller that suitable for VoIP USB phone applications. It includes USB1.1 audio control, a 16-bit multi-bit sigma-delta mono audio CODEC, an 8-bit MCU, PLL, regulator. It has maximum 16 GPIO pins can constitute a 64 key matrix directly support keypad control function. It's also support buzzer output pin and LCM for VoIP application. It supports 8 to 48 KHz sampling rates in analog playback and recording via EEPORM setting. Moreover, SN11300 provided two series bus interface with external MCU application for advanced functions. With so many features and low-lost cost, SN11300 is an ideal chip to build a USB VoIP phone solution.



Basic VoIP phone solution

The basic function for SN11300 is to be the USB wire phone single chip solution. It can control LCM display, keypads scan as well as the audio playback and audio record.



Advance system block diagram

The advance application for SN11300 is to add external MCU for the extended application, ex. USB HID devices for keyboard and mouse.

Totally one control pipe, two isochronous pipes, and two interrupt pipes are supported by SN11300.

II. Features

USB

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB audio device class specification v1.0
- Full-duplex playback/ recording audio stream without sound card in PC
- Compatible with Win2000/ WinXP and MacOS10.2/MacOS10.4 without additional driver
- Plug-and-Play operation with Microsoft OS or MacOS default drivers
- USB bus power or self power option
- USB audio function topology has two input terminals, two output terminals, and two feature units
- USB alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive
- Isochronous transfer uses adaptive and asynchronous synchronization
- Include two isochronous pipes, one Controller pipe and two HID pipes by default, and external MCU can modify the descriptors.

Voice

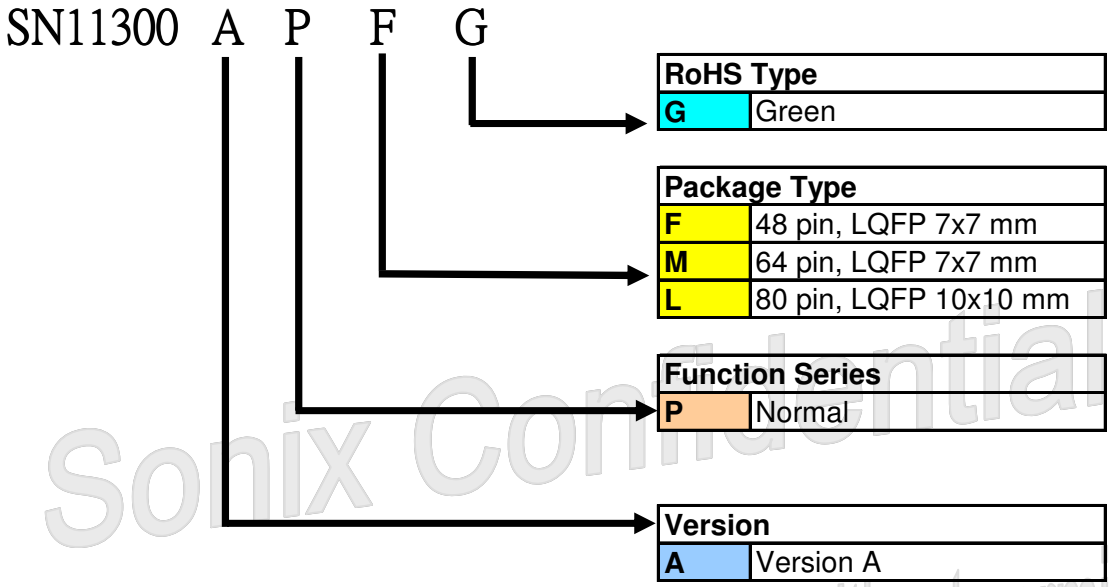
- Embedded high-performance multi-bit sigma-delta mono audio CODEC.
- 8KHz, 11.025KHz, 16KHz, 22.05KHz, 24KHz, 32KHz, 44.1KHz and 48KHz sampling rates for mono playback and recording
- 12MHz crystal input with on-chip PLL and embedded transceiver for USB
- On-chip PLL for synchronized with USB host for CODEC interface
- Compliant with USB HID class specification v1.1; pin control for volume up / down, play mute, and record mute
- Claim variable max packet size for saving USB bandwidth; according to sampling rate setting
- DAC SNR 91dB (A-weighted) at 1.8V
- ADC SNR 81dB (A-weighted) at 1.8V
- Mono single-ended ADC input with 1Vpp
- Mono single-ended DAC headphone output with 1Vpp
- 16-level programmable volume control form +33 dB to -12 dB in 3.0dB pre step for MIC/ADC input PGA
- 20-dB MIC gain boost control

- 28-level programmable volume control form 0 dB to -40.5dB in 1.5 dB pre step for headphone amplifier
- linear headphone amplifier for 32/16Ω load
- ADC PCM data range from +16383 to -16383

Peripheral

- Embedded 3.3 V to 1.8 V regulator
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps(Fast-mode)
- Features programmable by EEPROM values, for examples customized USB Ids, strings and option setting
- Support two EEPROM interfaces which are SPI interface(93C46, 93C56, 93C66) and I2C interface(24C01, 24C02, 24C04).
- HID interrupt interval can be modified via EEPROM
- EEPROM content can be read from application programming interface
- 1.8 V core operation and 3.3 V I/O
- System on chip solution: low cost and easy implementation without external memory
- LED indicator pins for playback and recording mute
- A GPIO pins controlled via application programming interface
- Programmable transfer length up to 3K bytes from host to device and 8 bytes from device to host by HID pipes
- Fast display speed for dot matrix LCD module or color STN LCD module
- A ring-tone editor for customized ring-tone

III. Ordering information



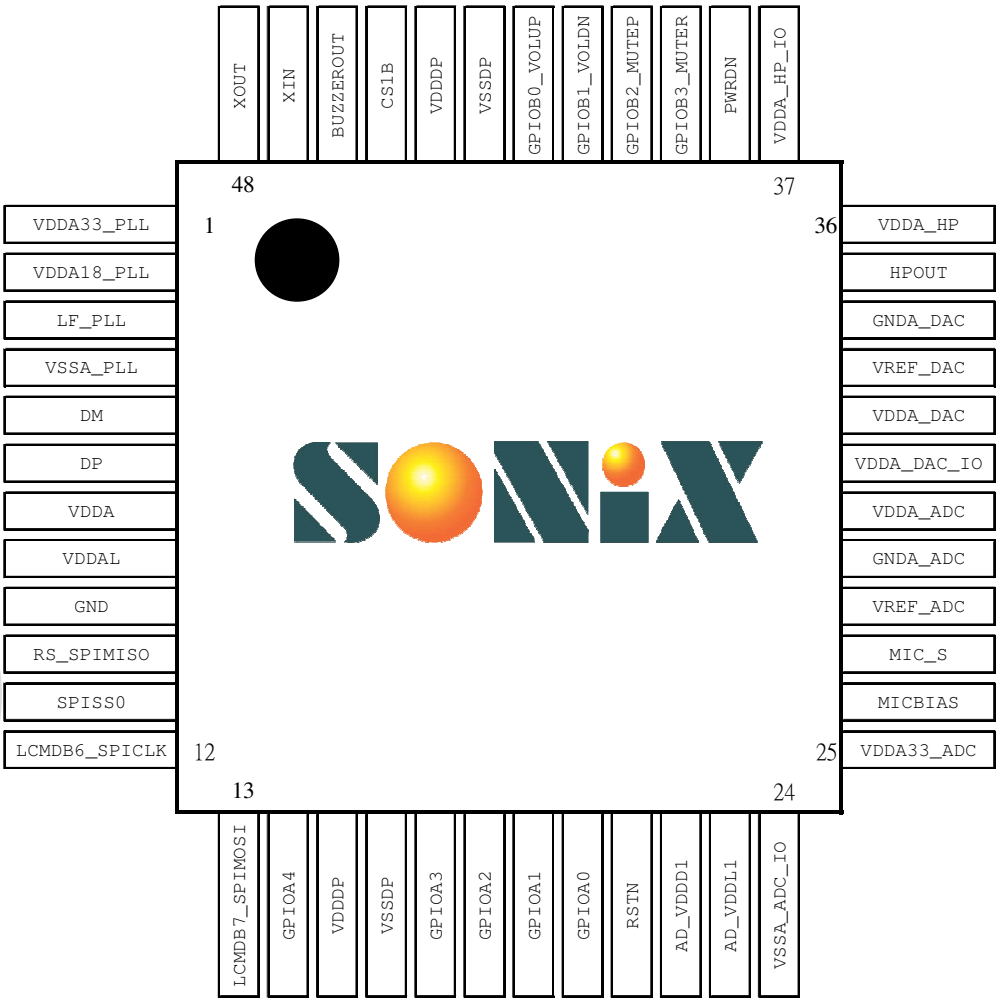
*1 Note: Please contact SONiX sales for detail.

Package comparison:

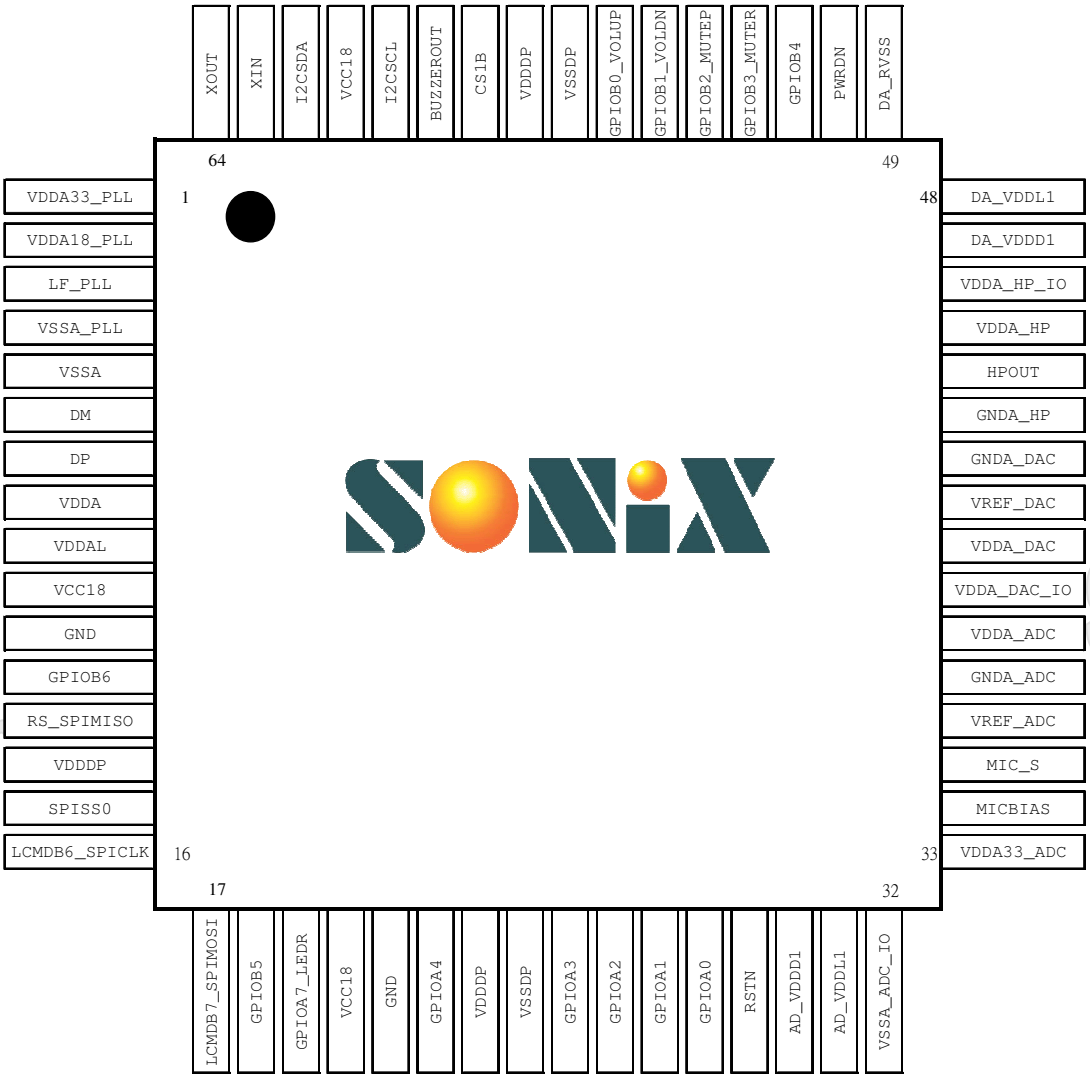
Function	SN11300A×LG(80 pin)	SN11300A×MG(64 pin)	SN11300A×FG(48 pin)
GPIO	16 pin	13 pin	9 pin
I^2C slave interface for External MCU	Yes	Yes	No
LCM interface	Parallel data interface Type of 6800/8080	Serial Peripheral Interface	Serial Peripheral interface
Embed 1.8V LDO	Core, ADC, DAC	Core, ADC, DAC	Core, CODEC
LED indicator	MUTER: Pin23 PLAY: Pin14	MUTER: Pin19	No

IV. Pin description

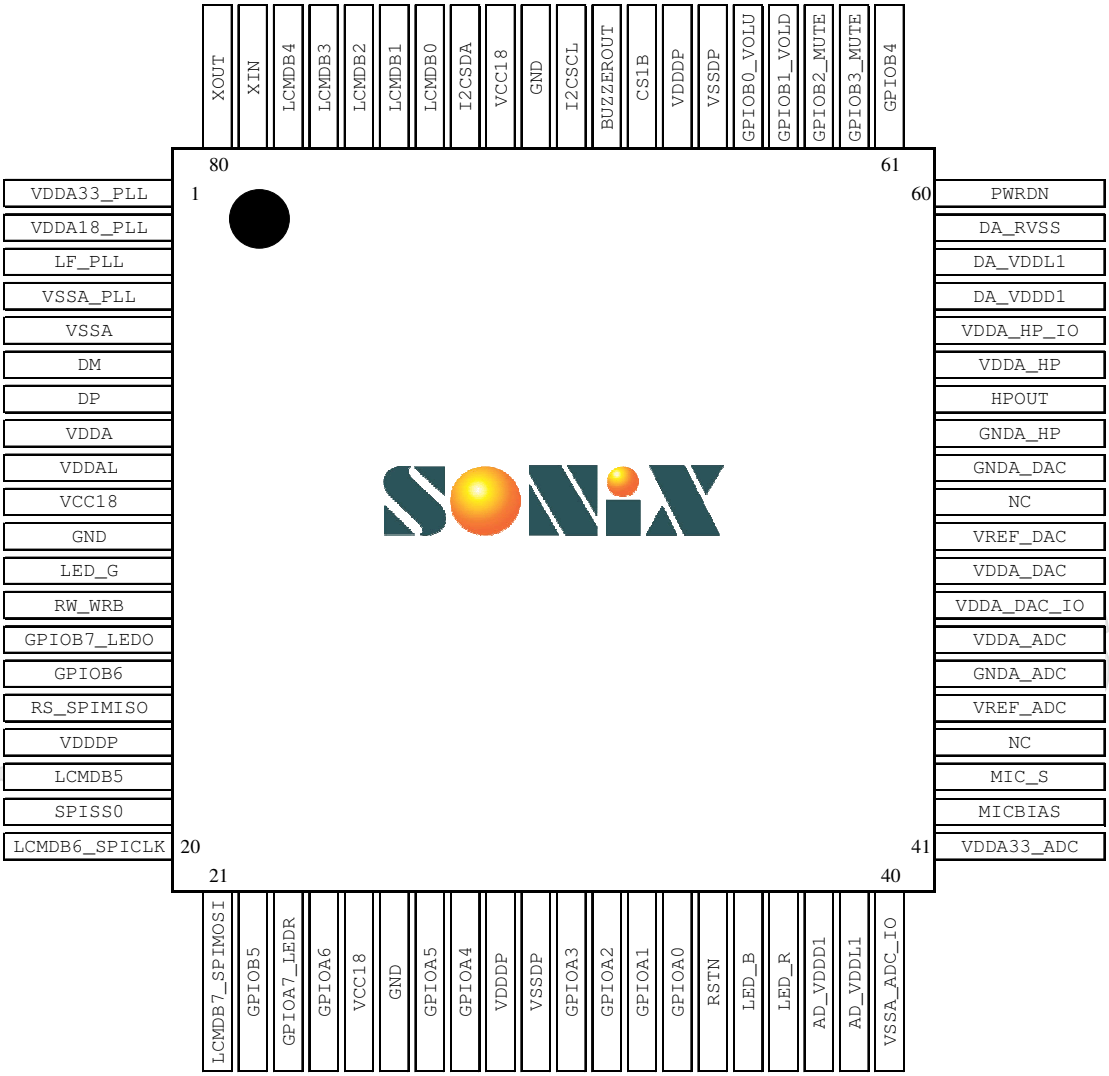
4.1 SN11300 pin chart (48-pin LQFP)



4.2 SN11300 pin chart (64-pin LQFP)



4.3 SN11300 pin chart (80-pin LQFP)



4.4 Pin assignment and description (48-pin LQFP)

Pin#	Pin name	Pin Type	Description
48			
1	VDDA33_PLL	AP	PLL IO 3.3 V power pin
2	VDDA18_PLL	AP	PLL core 1.8 V power pin
3	LF_PLL	AIO	Filter for internal PLL
4	VSSA_PLL	AP	PLL GND
5	DM	AIO	USB data minus
6	DP	AIO	USB data plus
7	VDDA	AP	3.3 V VDD of regulator
8	VDDAL	AP	1.8 V regulator output
9	GND	DP	Core ground
10	RS_SPIMISO	I/O, 4 mA	LCM Data/Register select pin or EEPROM data input
11	SPISS0	O, 4 mA, SR	EEPROM chip select, low active
12	LCMDB6_SPICLK	I/O, 4 mA	LCM data6 pin or EEPROM clock pin
13	LCMDB7_SPIMOSI	I/O, 4 mA	LCM data7 pin or EEPROM data output
14	GPIOA4	I/O, 4 mA	GPIOA4 pin
15	VDDDP	DP	3.3 V I/O power
16	VSSDP	DP	3.3 V I/O ground
17	GPIOA3	I/O, 4 mA	GPIOA3 pin
18	GPIOA2	I/O, 4 mA	GPIOA2 pin
19	GPIOA1	I/O, 4 mA	GPIOA1 pin
20	GPIOA0	I/O, 4 mA	GPIOA0 pin
21	RSTN	I, ST	System reset pin, low active
22	AD_VDDD1	AP	3.3 V VDD of regulator for CODEC(ADC and DAC)
23	AD_VDDL1	AP	1.8 V regulator output for CODEC(ADC and DAC)
24	VSSA_ADC_IO	AP	ADC I/O ground
25	VDDA33_ADC	AP	ADC I/O 3.3 V power

26	MICBIAS	AO	ADC MicroPhone Bias output
27	MIC_S	AI	Microphone single-ended In
28	VREF_ADC	AO	ADC reference voltage about 0.9 volts
29	GNDA_ADC	AP	ADC core ground
30	VDDA_ADC	AP	ADC core 1.8 V power
31	VDDA_DAC_IO	AP	DAC I/O 3.3 V power
32	VDDA_DAC	AP	DAC core 1.8 V power
33	VREF_DAC	AO	DAC reference voltage about 0.9 volts
34	GNDA_DAC	AP	DAC core ground
35	HPOUT	AO	DAC headphone out
36	VDDA_HP	AP	HeadPhone core 1.8 V power
37	VDDA_HP_IO	AP	HeadPhone I/O 3.3 V power
38	PWRDN	OD, 4 mA, SR	Power down switch control 0: normal mode, 1: power down mode
39	GPIOB3_MUTER	I/O, 4 mA	GPIOB3 pin/ Default MUTER key
40	GPIOB2_MUTEP	I/O, 4 mA	GPIOB2 pin/ Default MUTEP key
41	GPIOB1_VOLDN	I/O, 4 mA	GPIOB1 pin/ Default VOLDN key
42	GPIOB0_VOLUP	I/O, 4 mA	GPIOB0 pin/ Default VOLUP key
43	VSSDP	DP	3.3 V I/O ground
44	VDDDP	DP	3.3 V I/O power
45	CS1B	O, 4 mA, SR	LCM chip select, low active
46	BUZZEROUT	O, 4 mA, SR	Buzzer Output Pin
47	XIN	AI	12 MHz clock osc pin for PLL
48	XOUT	AO	12 MHz clock osc pin for PLL

4.5 Pin assignment and description (64-pin LQFP)

Pin#	Pin name	Pin Type	Description
64			
1	VDDA33_PLL	AP	PLL IO 3.3 V power pin
2	VDDA18_PLL	AP	PLL core 1.8 V power pin
3	LF_PLL	AIO	Filter for internal PLL
4	VSSA_PLL	AP	PLL GND
5	VSSA	AP	GND pin for USB transceiver
6	DM	AIO	USB data minus
7	DP	AIO	USB data plus
8	VDDA	AP	3.3 V VDD of regulator
9	VDDAL	AP	1.8 V regulator output
10	VCC18	DP	Core Power, 1.8V
11	GND	DP	Core ground
12	GPIOB6	I/O, 4 mA	GPIOB6 pin
13	RS_SPIMISO	I/O, 4 mA	LCM Data/Register select pin or EEPROM data input
14	VDDDP	DP	3.3 V I/O power
15	SPISS0	O, 4 mA, SR	EEPROM chip select, low active
16	LCMDB6_SPICLK	I/O, 4 mA	LCM data6 pin or EEPROM clock pin
17	LCMDB7_SPIMOSI	I/O, 4 mA	LCM data7 pin or EEPROM data output
18	GPIOB5	I/O, 4 mA	GPIOB5 pin
19	GPIOA7_LEDR	I/O, 4 mA	GPIOA7 pin/ LED for Record mute
20	VCC18	DP	Core Power, 1.8V
21	GND	DP	Core ground
22	GPIOA4	I/O, 4 mA	GPIOA4 pin
23	VDDDP	DP	3.3 V I/O power
24	VSSDP	DP	3.3 V I/O ground
25	GPIOA3	I/O, 4 mA	GPIOA3 pin
26	GPIOA2	I/O, 4 mA	GPIOA2 pin

27	GPIOA1	I/O, 4 mA	GPIOA1 pin
28	GPIOA0	I/O, 4 mA	GPIOA0 pin
29	RSTN	I, ST	System reset pin, low active
30	AD_VDDD1	AP	3.3 V VDD of regulator for ADC
31	AD_VDDL1	AP	1.8 V regulator output for ADC
32	VSSA_ADC_IO	AP	ADC I/O ground
33	VDDA33_ADC	AP	ADC I/O 3.3 V power
34	MICBIAS	AO	ADC MicroPhone Bias output
35	MIC_S	AI	Microphone single-ended In
36	VREF_ADC	AO	ADC reference voltage about 0.9 volts
37	GNDA_ADC	AP	ADC core ground
38	VDDA_ADC	AP	ADC core 1.8 V power
39	VDDA_DAC_IO	AP	DAC I/O 3.3 V power
40	VDDA_DAC	AP	DAC core 1.8 V power
41	VREF_DAC	AO	DAC reference voltage about 0.9 volts
42	GNDA_DAC	AP	DAC core ground
43	GNDA_HP	AP	HeadPhone ground
44	HPOUT	AO	DAC headphone out
45	VDDA_HP	AP	HeadPhone core 1.8 V power
46	VDDA_HP_IO	AP	HeadPhone I/O 3.3 V power
47	DA_VDDD1	AP	3.3 V VDD of regulator for DAC
48	DA_VDDL1	AP	1.8 V regulator output for DAC
49	DA_RVSS	AP	3.3 V GND of regulator for DAC
50	PWRDN	OD, 4 mA, SR	Power down switch control 0: normal mode, 1: power down mode
51	GPIOB4	I/O, 4 mA	GPIOB4 pin

52	GPIOB3_MUTER	I/O, 4 mA	GPIOB3 pin/ Default MUTER key
53	GPIOB2_MUTEP	I/O, 4 mA	GPIOB2 pin/ Default MUTEP key
54	GPIOB1_VOLDN	I/O, 4 mA	GPIOB1 pin/ Default VOLDN key
55	GPIOB0_VOLUP	I/O, 4 mA	GPIOB0 pin/ Default VOLUP key
56	VSSDP	DP	3.3 V I/O ground
57	VDDDP	DP	3.3 V I/O power
58	CS1B	O, 4 mA, SR	LCM chip select, low active
59	BUZZEROUT	O, 4 mA, SR	Buzzer Output Pin
60	I2CSCL	OD	Clock pin of two-wire serial port for external MCU control
61	VCC18	DP	Core Power, 1.8V
62	I2CSDA	OD	Data pin of two-wire serial port for external MCU control
63	XIN	AI	12 MHz clock osc pin for PLL
64	XOUT	AO	12 MHz clock osc pin for PLL

** All input pin are TTL level and Schmitt trigger, all output pins are slew rate control

I – input pin , O – output pin, DP,AP – power pin, ST – Schmitt trigger, SR – slew rate control, PU/PD – pull up or pull down, AI/AO/AIO – Analog PAD, OD – Open drain

4.6 Pin assignment and description (80-pin LQFP)

Pin#	Pin name	Pin Type	Description
80			
1	VDDA33_PLL	AP	PLL IO 3.3 V power pin
2	VDDA18_PLL	AP	PLL core 1.8 V power pin
3	LF_PLL	AIO	Filter for internal PLL
4	VSSA_PLL	AP	PLL GND
5	VSSA	AP	GND pin for USB transceiver
6	DM	AIO	USB data minus
7	DP	AIO	USB data plus
8	VDDA	AP	3.3 V VDD of regulator
9	VDDAL	AP	1.8 V regulator output
10	VCC18	DP	Core Power, 1.8V
11	GND	DP	Core ground
12	LED_G	O, 4 mA	LCM backlight Green
13	RW_WRB	I/O, 4 mA	LCM Data/Register select pin
14	GPIOB7_LEDO	I/O, 4 mA	GPIOB7/Play,Record LED
15	GPIOB6	I/O, 4 mA	GPIOB6 pin
16	RS_SPIMISO	I/O, 4 mA	LCM Data/Register select pin or EEPROM data input
17	VDDDP	DP	3.3 V I/O power
18	LCMDB5	O, 4 mA	LCM data5 pin
19	SPISS0	O, 4 mA, SR	EEPROM chip select, low active
20	LCMDB6_SPICLK	I/O, 4 mA	LCM data6 pin or EEPROM clock pin
21	LCMDB7_SPIMOSI	I/O, 4 mA	LCM data7 pin or EEPROM data output
22	GPIOB5	I/O, 4 mA	GPIOB5 pin
23	GPIOA7_LEDR	I/O, 4 mA	GPIOA7 pin/ LED for Record mute
24	GPIOA6	I/O, 4 mA	GPIOA6 pin
25	VCC18	DP	Core Power, 1.8V

26	GND	DP	Core ground
27	GPIOA5	I/O, 4 mA	GPIOA5 pin
28	GPIOA4	I/O, 4 mA	GPIOA4 pin
29	VDDDP	DP	3.3 V I/O power
30	VSSDP	DP	3.3 V I/O ground
31	GPIOA3	I/O, 4 mA	GPIOA3 pin
32	GPIOA2	I/O, 4 mA	GPIOA2 pin
33	GPIOA1	I/O, 4 mA	GPIOA1 pin
34	GPIOA0	I/O, 4 mA	GPIOA0 pin
35	RSTN	I, ST	System reset pin, low active
36	LED_B	O, 4 mA	LCM backlight Blue
37	LED_R	O, 4 mA	LCM backlight Red
38	AD_VDDD1	AP	3.3 V VDD of regulator for ADC
39	AD_VDDL1	AP	1.8 V regulator output for ADC
40	VSSA_ADC_IO	AP	ADC I/O ground
41	VDDA33_ADC	AP	ADC I/O 3.3 V power
42	MICBIAS	AO	ADC MicroPhone Bias output
43	MIC_S	AI	Microphone single-ended In
44	NC	-	-
45	VREF_ADC	AO	ADC reference voltage about 0.9 volts
46	GNDA_ADC	AP	ADC core ground
47	VDDA_ADC	AP	ADC core 1.8 V power
48	VDDA_DAC_IO	AP	DAC I/O 3.3 V power
49	VDDA_DAC	AP	DAC core 1.8 V power
50	VREF_DAC	AO	DAC reference voltage about 0.9 volts
51	NC	-	-
52	GNDA_DAC	AP	DAC core ground
53	GNDA_HP	AP	HeadPhone ground
54	HPOUT	AO	DAC headphone out
55	VDDA_HP	AP	HeadPhone core 1.8 V power

56	VDDA_HP_IO	AP	HeadPhone I/O 3.3 V power
57	DA_VDDD1	AP	3.3 V VDD of regulator for DAC
58	DA_VDDL1	AP	1.8 V regulator output for DAC
59	DA_RVSS	AP	3.3 V GND of regulator for DAC
60	PWRDN	OD, 4 mA, SR	Power down switch control 0: normal mode, 1: power down mode
61	GPIOB4	I/O, 4 mA	GPIOB4 pin
62	GPIOB3_MUTER	I/O, 4 mA	GPIOB3 pin/ Default MUTER key
63	GPIOB2_MUTEP	I/O, 4 mA	GPIOB2 pin/ Default MUTEP key
64	GPIOB1_VOLDN	I/O, 4 mA	GPIOB1 pin/ Default VOLDN key
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66	VSSDP	DP	3.3 V I/O ground
67	VDDDP	DP	3.3 V I/O power
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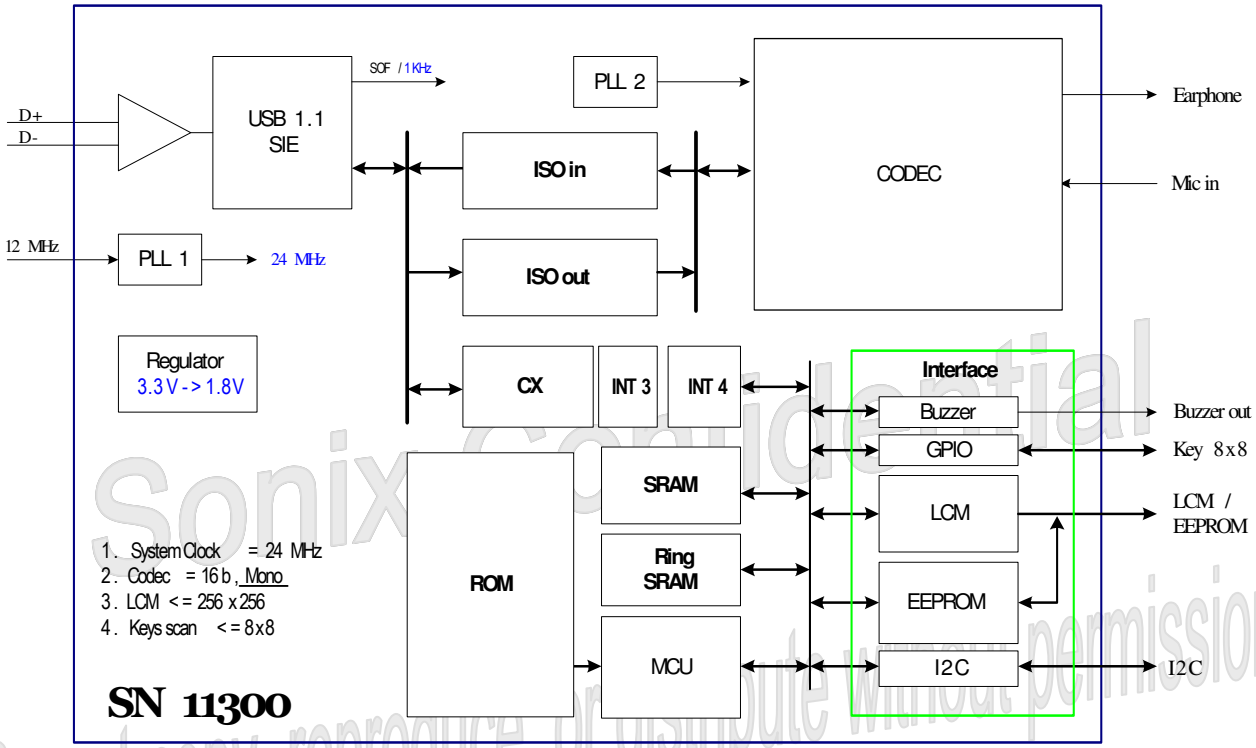
69	BUZZEROUT	O, 4 mA, SR	Buzzer Output Pin
70	I2CSCL	OD	Clock pin of two-wire serial port for external MCU control
71	GND	DP	Core ground
72	VCC18	DP	Core Power, 1.8V
73	I2CSDA	OD	Data pin of two-wire serial port for external MCU control
74	LCMDB0	O, 4 mA	LCM data0 pin
75	LCMDB1	O, 4 mA	LCM data1 pin
76	LCMDB2	O, 4 mA	LCM data2 pin
77	LCMDB3	O, 4 mA	LCM data3 pin
78	LCMDB4	O, 4 mA	LCM data4 pin

79	XIN	AI	12 MHz clock osc pin for PLL
80	XOUT	AO	12 MHz clock osc pin for PLL

** All input pin are TTL level and Schmitt trigger, all output pins are slew rate control

I – input pin , O – output pin, DP,AP – power pin, ST – Schmitt trigger, SR – slew rate control, PU/PD – pull up or pull down, AI/AO/AIO – Analog PAD, OD – Open drain

V. Block diagram (80 Pin)



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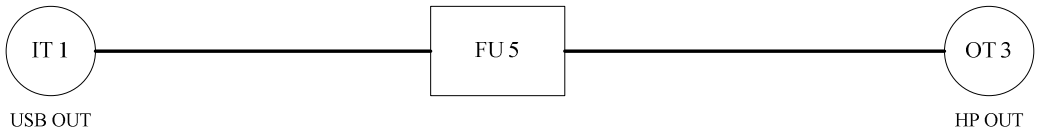
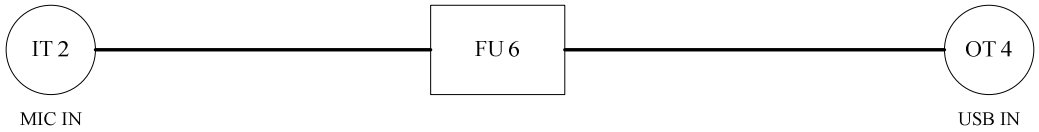




VI. EEPROM contents arrangement

The SN11300 supports an external EEPROM to be installed for the system manufacturers to customize the USB VID, PID and the vendor/product strings being

displayed in the OS to differentiate their own products with the others. Some of the features supported by the chip can also be programmed through setting proper values in the EEPROM. Any modification will be active after re-plug USB cable. The table below shows the format of the EEPROM. The detail is described in the following sub-section.

SONiX TAG:

The SN11300 supports total 6 kind of external EEPROM, This filed indicate the EEPROM type. The default value is 0x53, 0x4E (93C46).

USB VID and PID：

The default USB VID of SN11300 is 0x0C45. The default PID is 0x1300. The VID can be changed by program EEPROM byte 0~1, and PID by byte 2~3. It should be noted that the VID and PID values can not be set to 0x0000 or 0xFFFF.

Control byte 1:

The control byte 1 is located in byte 0x06 of EEPROM. Bit 0 to 3 is the HID3 interval time. It can be 2ms~20ms. Bit6 is Self-powered bit, and Bit7 indicate that the MaxPower in USB descriptor（"1" is 500mA, "0" is 100mA）.

Control byte 2:

The control byte 2 is located in byte 0x07 of EEPROM. Bit0 is HID key control bit. By default, SN11300 support 4 HID key (volume up, volume down, mute play, mute record). Set this bit to zero will disable HID key function. Bit 4 to 7 is Audio sampling rate. SN11300 support eight kind of sampling rate, default sampling rate is 48K Hz.

Control byte 3:

The control byte 3 is located in byte 0x08 of EEPROM. Bit 0 to 3 is the HID4 interval time. It can be 2ms~20ms.

LCM control byte:

The LCM control byte is located in byte 0x0C of EEPROM. Bit 2 to 3 is HID3 report out size. It supports two kind of report out size - 1K+32, 2K+32 bytes.

Control byte 4:

The control byte 4 is located in byte 0x0D of EEPROM. Bit 0 is external LCM exist bit. Default value is zero. Set 1 to this bit will disable internal LCM display function. Bit 1 is external key exist bit. Default value is zero. Set 1 to this bit will disable internal key function. Bit 2 to 5 is I2C timeout filed, SN11300 can communicate with external MCU by I2C interface, and this filed indicate SN11300 should wait how long when I2C interface fail to avoid system enter the dead loop. Bit 6 and Bit7 are reserved, set to 0.

Language ID

The language ID filed indicates the codes representing languages supported by SN11300. The default value is 0x04, 0x03, 0x09, and 0x04.

USB Manufacturer, Product and Serial string length:

The length of the vendor, product and serial string is user define. They are sequentially located in byte 0x14 to 0x16 of EEPROM. The only limitation is the sum of the all string length and API reserved bytes can't be over EEPROM size.

USB Manufacturer, Product and Serial string:

The USB string entity is start from byte 0x17 of EEPROM. They are sequentially Manufacturer, Product and Serial string.

API reserved bytes:

The last 16 bytes of EEPROM is reserved for API used.

EEPROM setting table:

USB AUDIO HIDDEN SECTOR DEFINITION -- > 128 BYTES (BAESD) AND 256 / 512 BYTES (EXTEND) FORMAT.			
Offset	Length	Definition (MP default)	Note
00 ~ 01 LSB ~ MSB	2 bytes	SONiX TAG (0x4E53)	SPI type: [0x53, 0x4E] → default (128bytes). [DEF] [0x52, 0x2A] → 256bytes. [0x53, 0x3A] → 512bytes. I2C type: [0x73, 0x01] → 128bytes [0x72, 0x02] → 256bytes. [0x73, 0x04] → 512bytes. The TAG is depending on hidden sector real size. ***If the TAG does not exist, all parameter is default value in FW ROM code.***
02 ~ 03 LSB ~ MSB	2 bytes	VID (0x0C45)	Vender ID [0x45,0x0C]
04 ~ 05 LSB ~ MSB	2 bytes	PID (0x1300)	Product ID [0x00,0x13]
06	1 byte	Control byte 1 (0x04)	Bit 3~0: HID3 interval 0000: 2 ms 0001: 4 ms 0010: 6 ms. 0011: 8 ms 0100: 10 ms [DEF] …. 1001:20 ms Others: Reserved Bit 4: Reserved, set to 0 Bit 5: Reserved, set to 0

			Bit 6: 1: self-powered. 0: Bus-powered. [DEF] Bit 7: 1: Maximum power = 500mA. 0: Maximum power = 100mA. [DEF]
07	1 byte	Control byte 2 (0x81)	Bit 0: HID Vol / Mute enable 1: HID report In include Vol / Mute .[DEF] 0: HID no Vol / Mute key field (HID enable means windows can recognize the 4 key without API) Bit 1~3: Reserve 0x00 Bit 7~4: Sampling rate 1000 : 48KHz [DEF] 1001 : 24KHz 0100 : 44.1KHz 0101 : 22.05KHz 0111 : 11.025KHz 0000 : 32KHz 0001 : 16KHz 0011 : 8KHz
08	1 byte	Control byte 3 [0x04]	Bit 3~0: HID4 interval 0000: 2 ms 0001: 4 ms 0010: 6 ms. 0011: 8 ms 0100: 10 ms [DEF] …. 1001:20 ms Others: Reserved Bit4~7: Reserve 0x00[DEF]
09	1 byte	USB connect delay time[0x0A]	USB connect delay time 0: No delay 1: delay 10ms[DEF]

			2: delay 20ms .... 255: delay 2550 ms
0A~0B	3 byte	Reverse for User's[0x00]	Reserve for User data[0x00]
C	1 bytes	LCM control [0x00]	Bit 0~1: Reserve 0x00 Bit 2~3: HID3 size for LCM 00: 1K+32 bytes [DEF] 01: 2K+32 bytes Others: Reserved (In general, 1k+32 is for mono LCM and 2k+32 is for color LCM) Bit 4~7: Reserve 0x00
D	1 bytes	Control byte4 (0x00)	Bit 0: extern LCM exist 1: extern LCM exist 0: extern LCM not exist [DEF] Bit 1: extern Key exist 1: extern Key exist 0: extern Key not exist [DEF] Bit2~5: I2C Timeout 0000: 500ms 0001: 1000 ms 0010: 1500ms ..... 1111: 4000ms Bit 6: Reserved, set to 0 Bit 7: Reserved, set to 0
E~F	2 bytes	Reverse for User's[0x00]	Reserve for User data[0x00]
10 ~ 13	4 bytes	Language ID (0x04030904)	English → [0x04,0x03,0x09,0x04]
14	1 byte	USB *Manufacturer*	USB *Manufacturer* string length

		string length (0x10)	[0x10]
15	1 byte	USB product string length (0x22)	USB product string length [0x22]
16	1 byte	USB serial string length (0x16)	USB serial string length [0x16]
17 ~ 26	16 bytes	USB *Manufacturer* string (GENERIC)	USB vendor string (depend on EEPROM size and string length) [0x10,0x03,0x47,0x00,0x45,0x00,0x4E,0x00,0x45,0x00,0x52,0x00,0x49,0x00,0x43,0x00]
27 ~ 48	34 bytes	USB product string (USB Audio Device)	USB Product String (depend on EEPROM size and string length) [0x22,0x03,0x55,0x00,0x53,0x00,0x42,0x00,0x20,0x00,0x41,0x00,0x75,0x00,0x64,0x00,0x69,0x00,0x6F,0x00,0x20,0x00,0x44,0x00,0x65,0x00,0x76,0x00,0x69,0x00,0x63,0x00,0x65,0x00]
49 ~ 5E	22 bytes	USB serial string (0000000000)	USB serial number. [0x16,0x03,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00]
5F ~ 6F	17 bytes	Reserve for User's (0x00)	Reserve for User data[0x00]
70 ~ 7F	16 bytes	Reserve for API (0x00)	Reserve for User data[0x00]

VII. HID bytes arrangement

The SN11300 is equipped with a special feature to let the host software to communicate with the USB downstream devices via the HID pipes. Using this feature, the system manufacturers can easily upgrade or increase the functions of their product by just updating the software installed on the PC. The detail is described in the *HID application note.*

VIII. Two-wire serial port definition

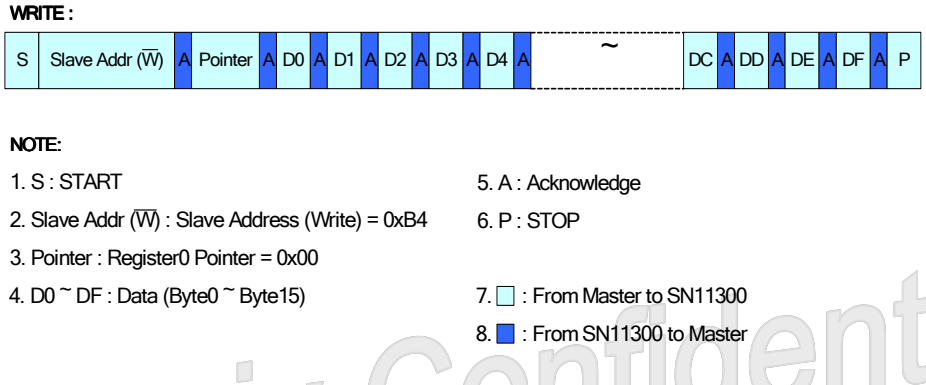
To provide extension capability, SN11300 contains a two wire series bus circuitry as an interface to external MCU. The two wire series bus serves as a slave device with bit rate up to 400Kbps（fast mode）. External MCU can write 16 bytes to the SN11300 with 7-bit register address 0x5A. MCU can also read 16 bytes from SN11300 with 7-bit register address 0x59. The detail is described in the *EXT-MCU application note and EXT-MCU programming guide.*

READ :

NOTE:

1. S : START
2. Sr : Repeated START
3. Slave Addr ($\overline{W}$) : Slave Address (Write) = 0xB2
4. Slave Addr (R) : Slave Address (Read) = 0xB3
5. Pointer : Register0 Pointer = 0x00
6. A : Acknowledge
7. $\overline{A}$: Not Acknowledge
8. D0 ~ DF : Data (Byte0 ~ Byte15)
9. P : STOP
10. □: From Master to SN11300
11. ■: From SN11300 to Master

READ



WRITE

IX. GPIO and Key function

SN11300 supports maximum 16 GPIO pins. Under the default setting, there are two LED indicator pins (GPIOB7, GPIOA7) for playback/recode and recording mute. And there are four button pins for volume up (GPIOA0+GPIOB0), volume down (GPIOA0+GPIOB1), playback mute (GPIOA0+GPIOB2) and recode mute (GPIOA0+GPIOB3). In addition, all GPIO pins can be control via application programming interface and support maximum 64 key matrix keypad functions or control maximum 16 independent GPIO functions.

X. LCM function

SN11300 supports maximum 256-column x 256-row dot matrix LCD module or color STN LCD module. We offer a simple and fast application programming interface to control and send Bitmap data from Host to LCM. SN11300 supports 8-bit parallel interface with 6800-series or 8080-series (80pin only) and 4 pin SPI interface to control LCM.

XI. Buzzer output function

SN11300 provide 128-bytes SRAM that contents ring-tone parameter for Buzzer output. The ring-tone parameter is easy to update by application programming interface when customers want to change their ring. We also provide a ring-tone editor for customers to make their own ring.

XII. Software support

SN11300 provides the following software to customers.

1. The Software Development Kit (SDK): The customers can use SDK to develop their own features, for example key definition, LCM display or ring-tone.
2. The application programming interface.

Note: Please contact SONiX sales for detail.

XIII. External-MCU Firmware support

SN11300 provides the following firmware and document to customers.

1. Standard 8051 C source code, it's convenient to include directly for 8051 type microprocessor.
2. Detail programming guide and function flowchart for other type microprocessor porting firmware.

XIV. Operating rating and electrical characteristics

14.1 Absolute maximum rating

Symbol	Parameter	Rating	unit
VDDDP	Power supply	-0.3 to 3.6	V
VDD	Power supply	-0.18 to 1.98	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
T_{stg}	storage temperature range	-40 to +125	^{0}C

14.2 ESD Performance

Symbol	Parameter	Rating	unit
ESD (HBM)	ESD human body mode	2000	V
ESD (MM)	ESD machine mode	200	V
I_{latch}	minimum latch up current	200	mA

14.3 Operation conditions

Symbol	Parameter	value	unit
VDDDP, VDDA33_PLL	Digital I/O and PLL IO supply voltage	+3.3 (typ)	V
VDDA, DA_VDDD1, AD_VDDD1	Regulator in supply voltage	+3.3 (typ)	V
VDDA33_ADC, VDDA_DA_IO, VDDA33_DAC, VDDA_HP_IO	CODEC IO supply voltage	+3.3 (typ)	V
VDD18	Digital core supply voltage	+1.8 (typ)	V
VDD18_PLL	PLL core supply voltage	+1.8 (typ)	V
AD_VDDL1, DA_VDDL1	Regulator output voltage	+1.8 (typ)	V
VDDA_ADC, VDDA_DAC, VDDA_HP	CODEC core power supply voltage	+1.8 (typ)	V
VREF_ADC, VREF_DAC	CODEC reference voltage	+0.9 (typ)	V
MICBIAS	Microphone bias output voltage	+2.6 (typ)	V
T_A	operating ambient temperature range	25 (typ)	^{O}C

14.4 DC electrical characteristics

Symbol	parameter	test condition	Value	unit
V_{DI}	differential input sensitivity	| (D+) – (D-) |	0.2 (min)	V
V_{CM}	differential common mode range	Included V_{DI} range	0.8 (min) 2.5 (max)	V
V_{SE}	single ended receiver threshold		0.8 (min) 2.0 (max)	V
V_{IH}	high level input voltage		2.0 (min)	V
V_{IL}	low level input voltage		0.8 (max)	V
I_{OH}	drive current	V_{OH} = 2.3V	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{OL}	sink current	V_{OL}= 0.5 V	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{o_max}	maximum current in operation		60 (max)	mA
Isuspend	supply current in suspend		400 (max)	µA

14.5 AC electrical characteristics

14.5.1 Operation clocks

symbol	parameter	value	unit
XIN	system clock input to PLL	12 (typ)	MHz
	XIN duty cycle	50 ± 2	%

14.5.2 Codec electrical parameters

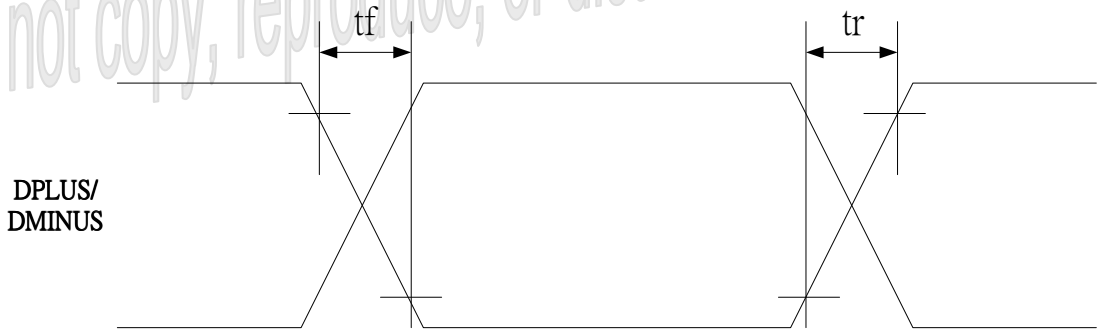
VDDA_ADC=VDDA_DAC= 1.8V, VDDA33_ADC= 3.1V, MICBIAS= 2.5V, Ta= +25℃, 1kHz signal, 16-bit audio data, 48kHz sampling rate

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC) to MONO input						
Signal to Noise Ratio (note2)	SNR	A-weighted, 0dB gain		81		dB
Dynamic range (note3)	DR	A-weighted, 0dB gain		81		dB
Total Harmonic Distortion(note4)	THD	Full-scale, 0dB gain		-75		dB
Full-scale Input Signal Level (0dB)	-	-		0.42 1.2		Vrms Vpp

Microphone input (ADC) gain						
Boost Gain	-	-	-	20	-	dB
Gain Adjustment Range	-	-	-12	-	33	dB
Gain Adjustment Steps	-	-	-	16	-	Steps

Digital to Analogue Converter (DAC) to MONO output						
Signal to Noise Ratio (note5,6)	SNR	A-weighted, 0dB gain		91		dB
Dynamic range (note3)	DR	A-weighted, 0dB gain		91		dB
Total Harmonic Distortion	THD	RL=10KΩ		-81		dB
		RL=32Ω		-72		dB
		RL=16Ω		-67		dB
Full-scale Output Signal Voltage (0dB)	-	RL=10K		0.5 1.4		Vrms Vpp
		RL=32Ω		0.42 1.2		Vrms Vpp
		RL=16Ω		0.38 1.0		Vrms Vpp
Digital to Analogue Converter (DAC) amplification						
Volume Control Level	-	-	-40.5	-	0	dB
Volume Control Step	-	-	-	28	-	Steps

14.5.3 USB transceiver signal (full speed mode)



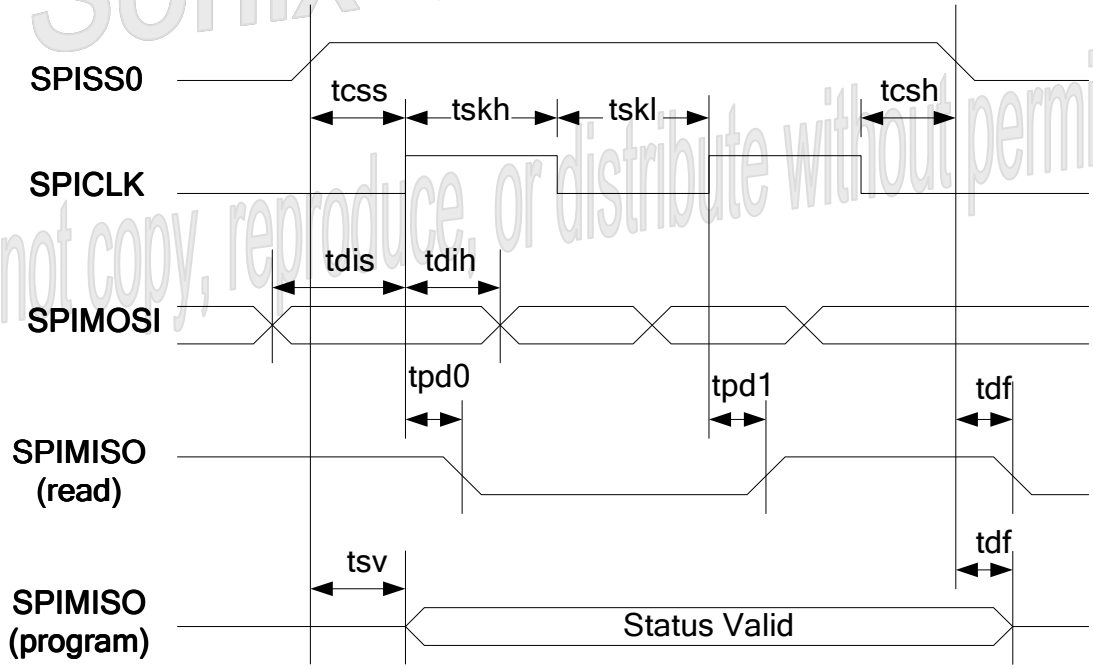
Symbol	parameter	test condition	Min	max	unit
Tr	transition rise time for USBDP or USBDM		4	20	ns
Tf	transition fall time for USBDP or USBDM		4	20	ns
Trfm	rise / fall time matching	(Tr / Tf) * 100	90	110	%
Vo(crs)	signal crossover voltage		1.3	2.0	V

14.5.4 Embedded Regulator

T_A=25C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		3	3.3	3.6	V
V_{OUT}	Output Voltage		1.62	1.8	1.98	V
I_{MAX}	Maximum Load Current	VDDA=3.3V	100			mA
V_{DROP}	Dropout Voltage	VDDA=3.3V, 100mA Loading			30	mV

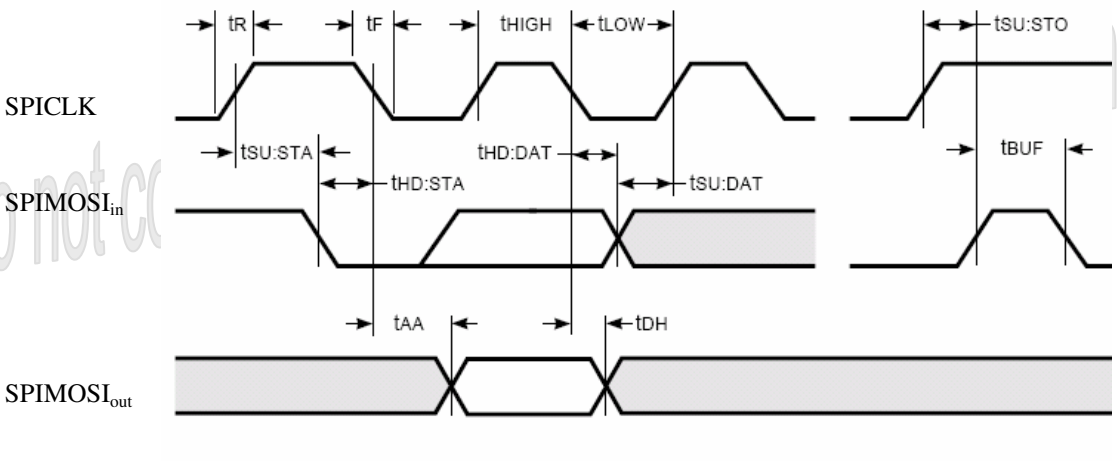
14.5.5 EEPROM Interface (93Cxx)



symbol	parameter	min	typ	max	unit
tsk	SPICLK clock frequency	-	400	-	kHz
tskh	SPICLK high time		1200		ns
tskl	SPICLK low time		1200		ns
tcs	Minimum SPISS0 low time		2400		ns

tcss	SPISS0 setup time		2400		ns
tdis	SPIMOSI setup time		1200		ns
tcsh	SPISS0 hold time		1200		ns
tdih	SPIMOSI hold time		1200		ns
tpd1	SPIMISO delay to “1”			250	ns
tpd0	SPIMISO delay to “0”			250	ns
tsv	SPISS0 to status valid			250	ns
tdf	SPISS0 to SPIMISO high impedance			250	ns

14.5.6 EEPROM Interface (24C0x)



Symbol	Parameter	STANDARD-MODE		FAST-MODE		Unit
		Min.	Max.	Min.	Max.	
fSCL	SPICLK Clock Frequency	0	100	0	400	KHz
tLOW	Clock LOW Period	4.7	—	1.2	—	μs
tHIGH	Clock HIGH Period	4	—	0.6	—	μs
tBUF	Bus Free Time Before New Transmission(1)	4.7	—	1.2	—	μs
tSU:STA	Start Condition Setup Time	4.7	—	0.6	—	μs
tSU:STO	Stop Condition Setup Time	4.7	—	0.6	—	μs
tHD:STA	Start Condition Hold Time	4	—	0.6	—	μs

tHD:STO	Stop Condition Hold Time	4	—	0.6	—	μs
tSU:DAT	Data In Setup Time	200	—	100	—	ns
tHD:DAT	Data In Hold Time	0	—	0	—	ns
tDH	Data Out Hold Time	100	—	50	—	ns
tAA	Clock to Output	0.1	4.5	0.1	0.9	μs
tR	SCL and SDA Rise Time(1)	—	1000	—	300	ns
tF	SCL and SDA Fall Time(1)	—	300	—	300	ns

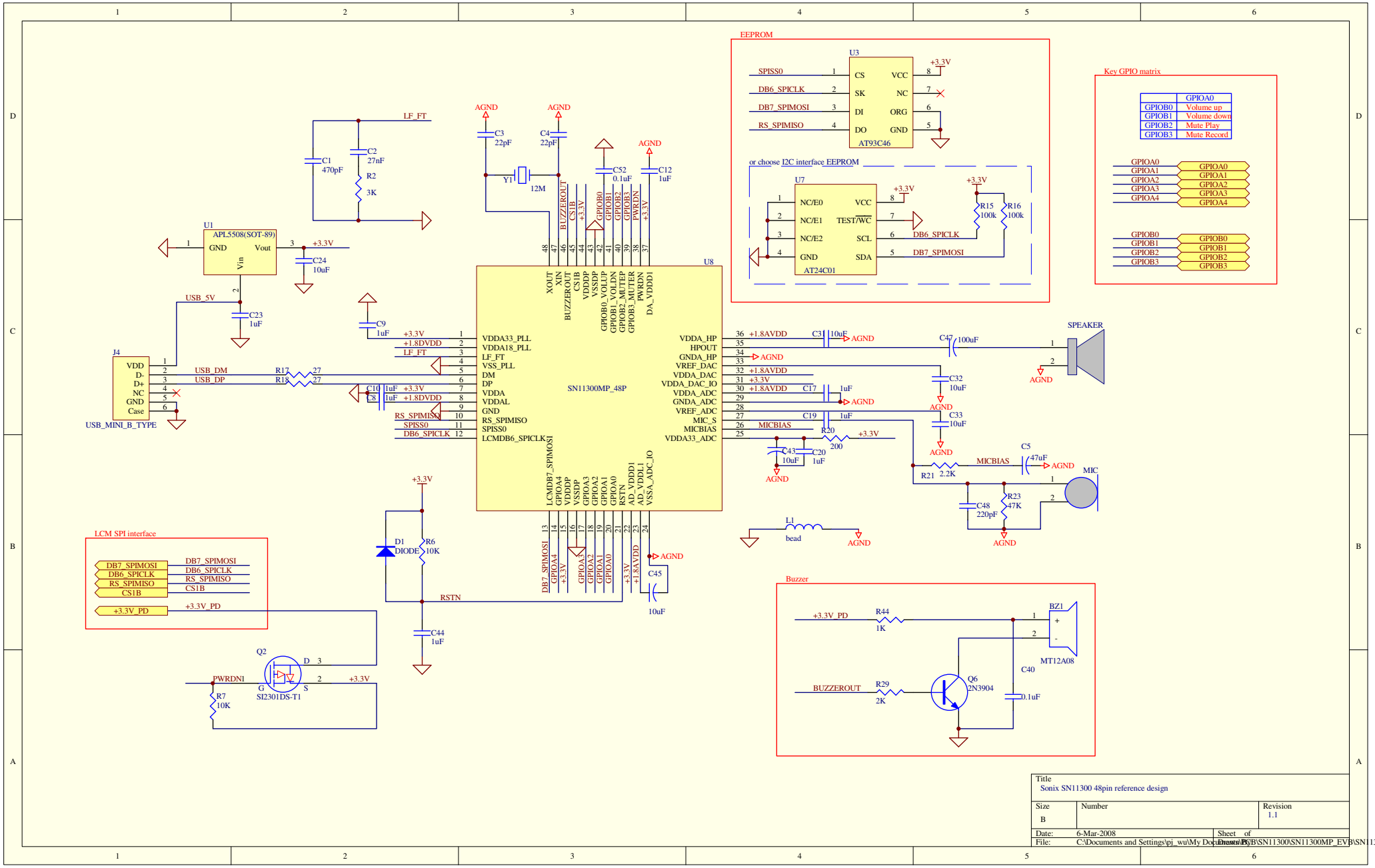
Note:1. This parameter is characterized but not 100% tested.

XV. Reference design

15.1 48pin reference Bill of Material

No.	Part Type	Designator	Description
1	MT12A08	BZ1	Magnetic Buzzer
2	0.1uF	C40	C-0603
3	0.1uF	C52	C-0603
4	10uF	C24	C-1206, CL31F106ZOHNNNE, SAMSUNG
5	1uF	C10	C-0603
6	1uF	C12	C-0603
7	1uF	C17	C-0603
8	1uF	C19	C-0603
9	1uF	C20	C-0603
10	1uF	C23	C-0603
11	1uF	C8	C-0603
12	1uF	C9	C-0603
13	220pF	C48	C-0603
14	22pF	C3	C-0603
15	22pF	C4	C-0603
16	27nF	C2	C-0603
17	470pF	C1	C-0603
18	100uF	C47	RV2-16V101MS-R, 100uF, 16V, ±20%, ELNA
19	10uF	C43	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
20	10uF	C45	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
21	10uF	C31	C-1206, CL31F106ZOHNNNE, SAMSUNG
22	10uF	C32	C-1206, CL31F106ZOHNNNE, SAMSUNG
23	10uF	C33	C-1206, CL31F106ZOHNNNE, SAMSUNG
24	1uF	C44	C-0603
25	47uF	C5	AVX, TAJB476M010RNJ
26	DIODE	D1	DIODE, 1N4148
27	SN11300MP_48P	U8	SN11300APFG, 48pin, LQFP7x7mm
28	AT93C46	U3	EEPROM AT93C46(128x8bit), ATMEL
29	bead	L1	PBY160808T-300Y-N, Z=30 ohm, ±25%, YAGEO
30	12M	Y1	Crystal 12MHz ±30ppm
31	27	R17	R-0603
32	27	R18	R-0603
33	200	R20	R-0603
34	10K	R6	R-0603
35	10K	R7	R-0603
36	1K	R44	R-0603
37	2.2K	R21	R-0603
38	2K	R29	R-0603
39	3K	R2	R-0603
40	47K	R23	R-0603
41	APL5508	U1	LDO, 5V to 3.3V, Iout<500mA, ANPEC
42	2N3904	Q6	BJT, NPN
43	SI2301DS-T1	Q2	MOSFET, P-channel
44	USB_MINI_B_TYPE	J4	USB-M5P

15.2 48pin reference design

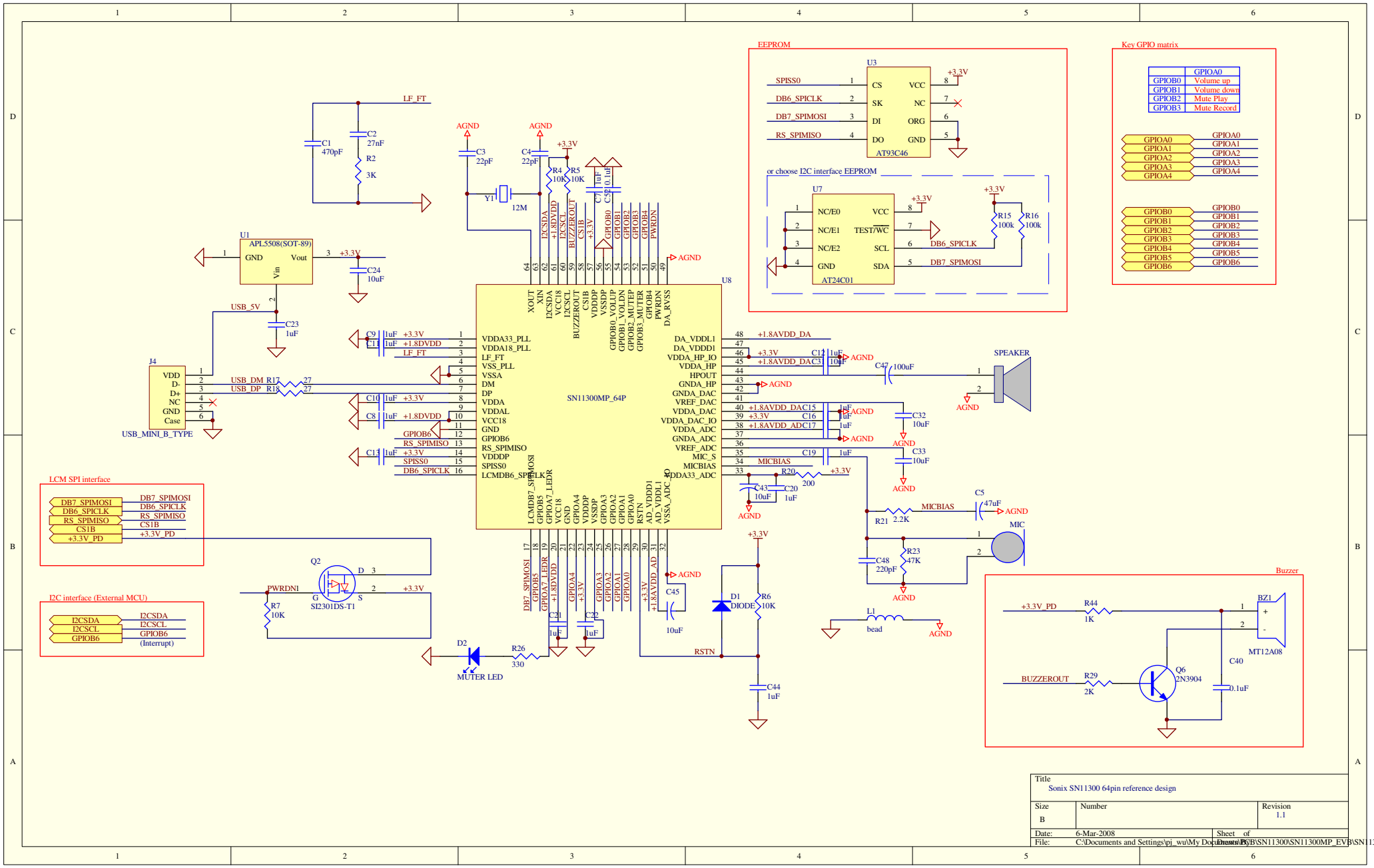


15.3 64pin reference Bill of Material

No.	Part Type	Designator	Description
1	MT12A08	BZ1	Magnetic Buzzer
2	0.1uF	C40	C-0603
3	0.1uF	C52	C-0603
4	10uF	C24	C-1206, CL31F106ZOHNNNE, SAMSUNG
5	1uF	C10	C-0603
6	1uF	C11	C-0603
7	1uF	C12	C-0603
8	1uF	C13	C-0603
9	1uF	C15	C-0603
10	1uF	C16	C-0603
11	1uF	C17	C-0603
12	1uF	C19	C-0603
13	1uF	C20	C-0603
14	1uF	C21	C-0603
15	1uF	C22	C-0603
16	1uF	C23	C-0603
17	1uF	C7	C-0603
18	1uF	C8	C-0603
19	1uF	C9	C-0603
20	220pF	C48	C-0603
21	22pF	C3	C-0603
22	22pF	C4	C-0603
23	27nF	C2	C-0603
24	470pF	C1	C-0603
25	100uF	C47	RV2-16V101MS-R, 100uF, 16V, ±20%, ELNA
26	10uF	C43	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
27	10uF	C45	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
28	10uF	C31	C-1206, CL31F106ZOHNNNE, SAMSUNG
29	10uF	C32	C-1206, CL31F106ZOHNNNE, SAMSUNG
30	10uF	C33	C-1206, CL31F106ZOHNNNE, SAMSUNG
31	1uF	C44	C-0603
32	47uF	C5	AVX, TAJB476M010RNJ
33	DIODE	D1	DIODE, 1N4148
34	SN11300MP_64P	U8	SN11300APMG, 64pin, LQFP7x7mm
35	AT93C46	U3	EEPROM AT93C46(128x8bit), ATMEL
36	bead	L1	PBY160808T-300Y-N, Z=30 ohm, ±25%, YAGEO
37	MUTER LED	D2	LED-D-1
38	12M	Y1	Crystal 12MHz ±30ppm
39	27	R17	R-0603
40	27	R18	R-0603
41	200	R20	R-0603
42	330	R26	R-0603
43	10K	R4	R-0603
44	10K	R5	R-0603
45	10K	R6	R-0603
46	10K	R7	R-0603
47	1K	R44	R-0603
48	2.2K	R21	R-0603

49	2K	R29	R-0603
50	3K	R2	R-0603
51	47K	R23	R-0603
52	APL5508	U1	LDO, 5V to 3.3V, Iout<500mA, ANPEC
53	2N3904	Q6	BJT, NPN
54	SI2301DS-T1	Q2	MOSFET, P-channel
55	USB_MINI_B_TYPE	J4	USB-M5P

15.4 64pin reference design

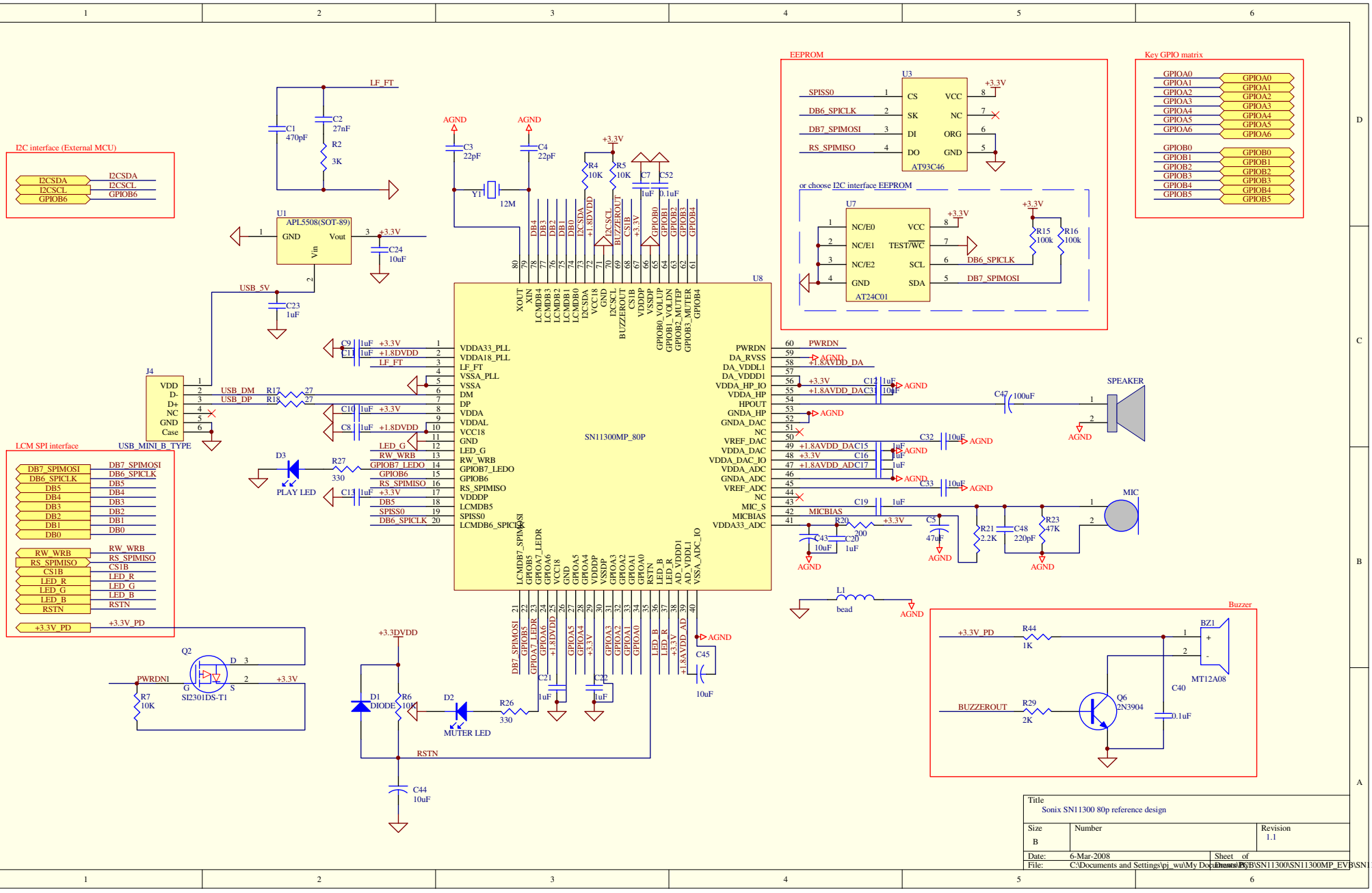


15.5 80pin reference Bill of Material

No.	Part Type	Designator	Description
1	MT12A08	BZ1	Magnetic Buzzer
2	0.1uF	C40	C-0603
3	0.1uF	C52	C-0603
4	10uF	C24	C-1206, CL31F106ZOHNNNE, SAMSUNG
5	1uF	C10	C-0603
6	1uF	C11	C-0603
7	1uF	C12	C-0603
8	1uF	C13	C-0603
9	1uF	C15	C-0603
10	1uF	C16	C-0603
11	1uF	C17	C-0603
12	1uF	C19	C-0603
13	1uF	C20	C-0603
14	1uF	C21	C-0603
15	1uF	C22	C-0603
16	1uF	C23	C-0603
17	1uF	C7	C-0603
18	1uF	C8	C-0603
19	1uF	C9	C-0603
20	220pF	C48	C-0603
21	22pF	C3	C-0603
22	22pF	C4	C-0603
23	27nF	C2	C-0603
24	470pF	C1	C-0603
25	100uF	C47	RV2-16V101MS-R, 100uF, 16V, ±20%, ELNA
26	10uF	C43	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
27	10uF	C45	RV2-16V100MU-R, 10uF, 16V, ±20%, ELNA
28	10uF	C31	C-1206, CL31F106ZOHNNNE, SAMSUNG
29	10uF	C32	C-1206, CL31F106ZOHNNNE, SAMSUNG
30	10uF	C33	C-1206, CL31F106ZOHNNNE, SAMSUNG
31	1uF	C44	C-0603
32	47uF	C5	AVX, TAJB476M010RNJ
33	DIODE	D1	DIODE, 1N4148
34	SN11300MP_80P	U8	SN11300APLG, 80pin, LQFP10x10mm
35	AT93C46	U3	EEPROM AT93C46(128x8bit), ATMEL
36	bead	L1	PBY160808T-300Y-N, Z=30 ohm, ±25%, YAGEO
37	MUTER LED	D2	LED-D-1
38	PLAY LED	D3	LED-D-1
39	12M	Y1	Crystal 12MHz ±30ppm
40	27	R17	R-0603
41	27	R18	R-0603
42	200	R20	R-0603
43	330	R26	R-0603
44	330	R27	R-0603
45	10K	R4	R-0603
46	10K	R5	R-0603
47	10K	R6	R-0603
48	10K	R7	R-0603

49	1K	R44	R-0603
50	2.2K	R21	R-0603
51	2K	R29	R-0603
52	3K	R2	R-0603
53	47K	R23	R-0603
54	2N3904	Q6	BJT, NPN
55	SI2301DS-T1	Q2	MOSFET, P-channel
56	APL5508	U1	LDO, 5V to 3.3V, Iout<500mA, ANPEC
57	USB_MINI_B_TYPE	J4	USB-M5P

15.6 80pin reference design

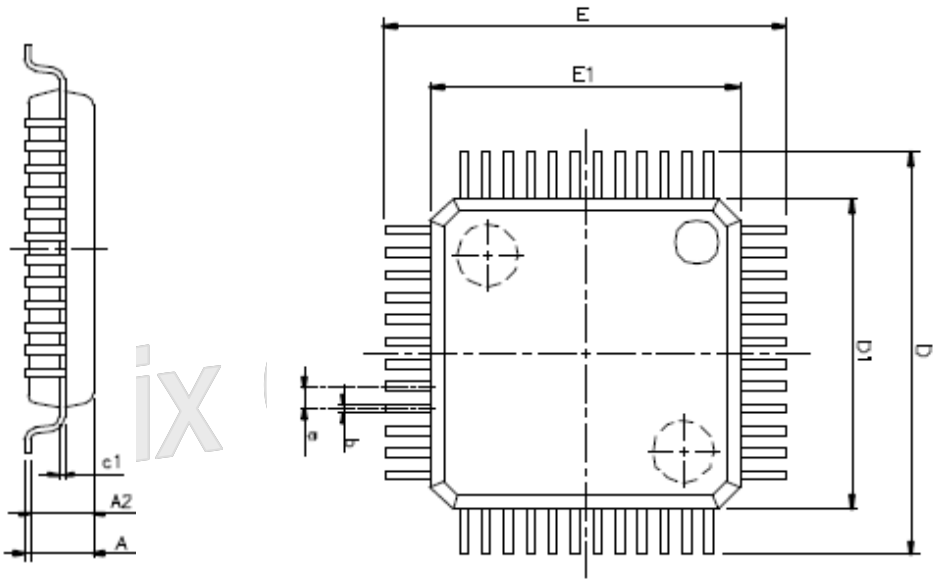


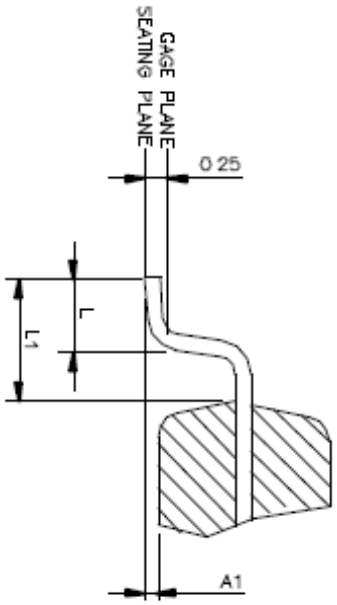
XVI. PCB Layout note

1. USB D+ and D- lines must as short as possible on PCB, it avoids mismatch on PCB line's impedance. In Sonix's evaluation board, D+ and D- line length had less than 50 mm.
2. C1, C2 and R2 are the group of PLL's LPF. Those must close to the pin of LF_FT.
3. Place power supply bypass capacitors as close as possible to SN11300 power input pins, in order to minimize the return path impedance. The components included C7, C8, C9, C10, C11, C12, C13, C15, C16, C17, C21, C22, C23, C24, C31, C20, C43, and C45.
4. VREF_DAC and VREF_ADC bypass capacitor C32 and C33 must close to those two pins.
5. Crystal circuit must close to pin XOUT and pin XIN, it avoids EMI/EMC effect.

XVII. Package dimension

17.1 48 pin package dimension

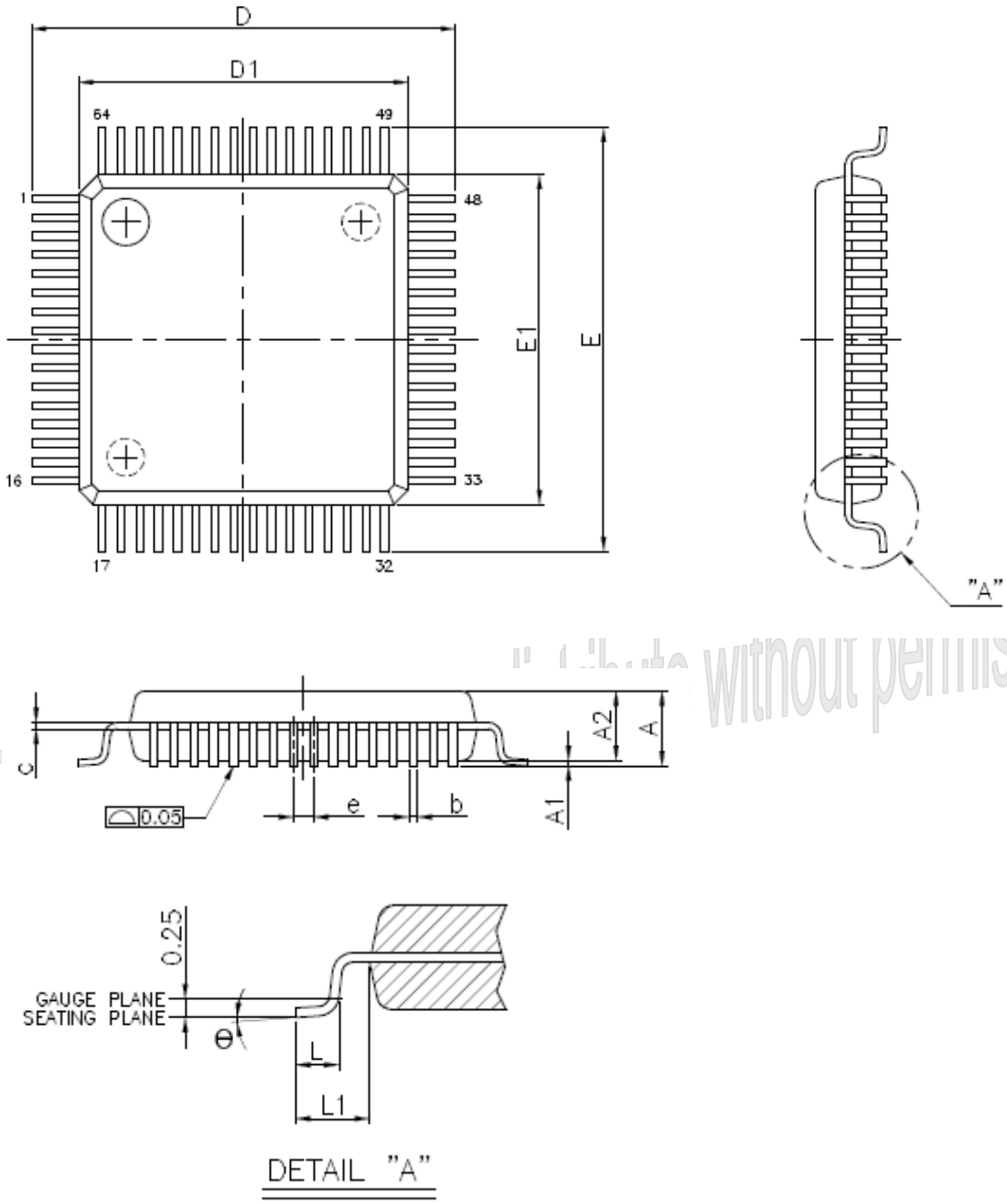




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0 15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

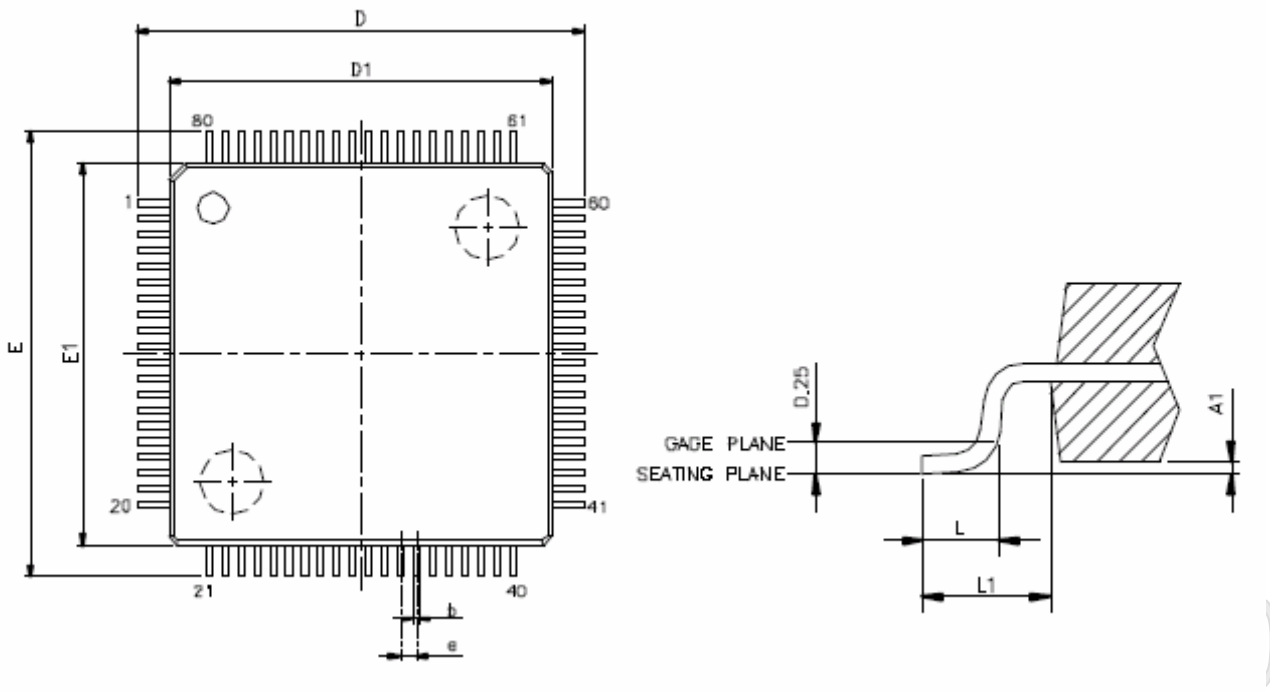
17.2 64 pin package dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

17.3 80 pin package dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

Revision History

Revision	*Revision Date*	*Description of changes*
V1.0	Mar 15, 2007	
V1.1	Jun 20, 2007	1. Modify Ⅳ.Pin description 2. Modify 14.5.2 Codec electrical parameters 3. Modify ⅩⅤ. Reference design 4. Add ⅩⅥ. PCB Layout note
V1.2	Aug 2, 2007	1. Modify Ⅲ. Ordering information 2. Removed the remote wake-up 3. Add the description in section 15.1, 15.3, 15.5 BOM
V1.3	March 6, 2008	1. Modify ⅩⅤ. Reference design, add C5 (47uF) at microphone bias.

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