

### 8 M-BIT CMOS 3.0 V-ONLY FLASH MEMORY 1 M-WORD BY 8-BIT (BYTE MODE)

#### Description

The  $\mu$ PD29F008L is an electrically programmable/erasable high-speed 3.0 V-only flash memory with a 8,388,608-bit configuration. It possesses an automatic single Byte program function and an automatic block erase function that are effected by command register input.

This memory consists of 19 blocks: one protection block (16 K byte), two condition blocks (8 K byte by 2 blocks), and sixteen main blocks (32 K byte by 1 block, 64 K byte by 15 blocks).

The  $\mu$ PD29F008L comes in two types: the type T with the protection block located at the top address and the type B with the protection block located at the bottom address.

The  $\mu$ PD29F008L is packed in 40-pin TSOP (I) (10 × 20 mm).

#### Features

- 1,048,576 words by 8 bit
- Two types of protection block locations
  - type T : protection block at the top address
  - type B : protection block at the bottom address
- Fast access time : 120, 150 ns (MAX.)
- Fast program/erase time.
  - Program: 9  $\mu$ s (TYP.)
- Block erase
  - Protection block : 1.0 s (TYP.)
  - Condition block : 1.0 s (TYP.)
  - Main block : 1.0 s (TYP.)
- Command register input
- Automatic program function
- Hardware reset
- Ready (/Busy) output (RY (/BY))
- Data polling and toggle bit
- Automatic erase function
- Functions for automatic erasure:
  - Erase suspend and resume functions
- Minimum number of repetitions for program/erase:
  - 100,000 times
- Directly drive TTL or CMOS
- Low power dissipation
  - Reset mode : 5.0  $\mu$ A (MAX.)
  - Standby mode : 5.0  $\mu$ A (MAX.)
  - Operating mode : 35 mA (MAX.)
- Voltage range
  - V<sub>cc</sub>: 3.0 V + 20 %/-10 % (Extend voltage)

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Protection block	Package
μPD29F008LGZ-B12T-LJH	120 ns	The top address	40-pin plastic TSOP (I) (10 × 20 mm) (Normal bent)
μPD29F008LGZ-B15T-LJH	150 ns		
μPD29F008LGZ-B12B-LJH	120 ns	The bottom address	
μPD29F008LGZ-B15B-LJH	150 ns		
μPD29F008LGZ-B12T-LKH	120 ns	The top address	40-pin plastic TSOP (I) (10 × 20 mm) (Reverse bent)
μPD29F008LGZ-B15T-LKH	150 ns		
μPD29F008LGZ-B12B-LKH	120 ns	The bottom address	
μPD29F008LGZ-B15B-LKH	150 ns		

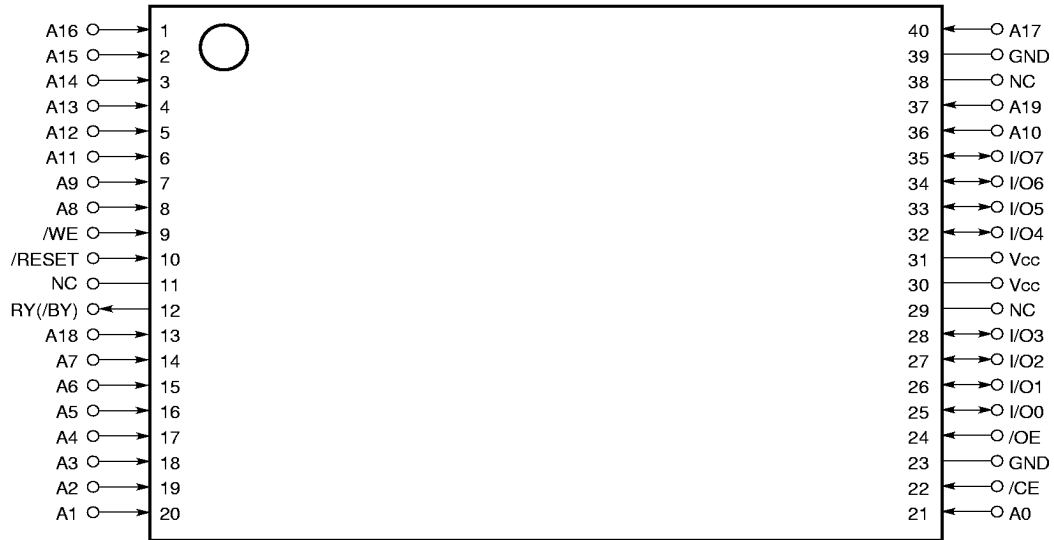
**Remark** For the address locations of the blocks, see the memory maps in **Erase Block Layout**.

Pin Configuration (Marking Side)

40-pin plastic TSOP (I) (10 × 20 mm) (Normal bent)

μPD29F008LGZ-xxxT-LJH

μPD29F008LGZ-xxxB-LJH



- A0 to A19 : Address inputs
- I/O0 to I/O7 : Data inputs/outputs
- /CE : Chip enable
- /WE : Write enable
- /OE : Output enable
- /RESET : Hardware reset input
- RY (/BY) : Ready (/Busy) output
- Vcc : Supply voltage
- GND : Ground
- NC<sup>Note</sup> : No connection

**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

40-pin plastic TSOP (I) (10 × 20 mm) (Reverse bent)

μPD29F008LGZ-xxxT-LKH

μPD29F008LGZ-xxxB-LKH



- A0 to A19 : Address inputs
- I/O0 to I/O7 : Data inputs/outputs
- /CE : Chip enable
- /WE : Write enable
- /OE : Output enable
- /RESET : Hardware reset input
- RY (/BY) : Ready (/Busy) output
- V<sub>cc</sub> : Supply voltage
- GND : Ground
- NC<sup>Note</sup> : No connection

**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

## Input/Output Pin Functions

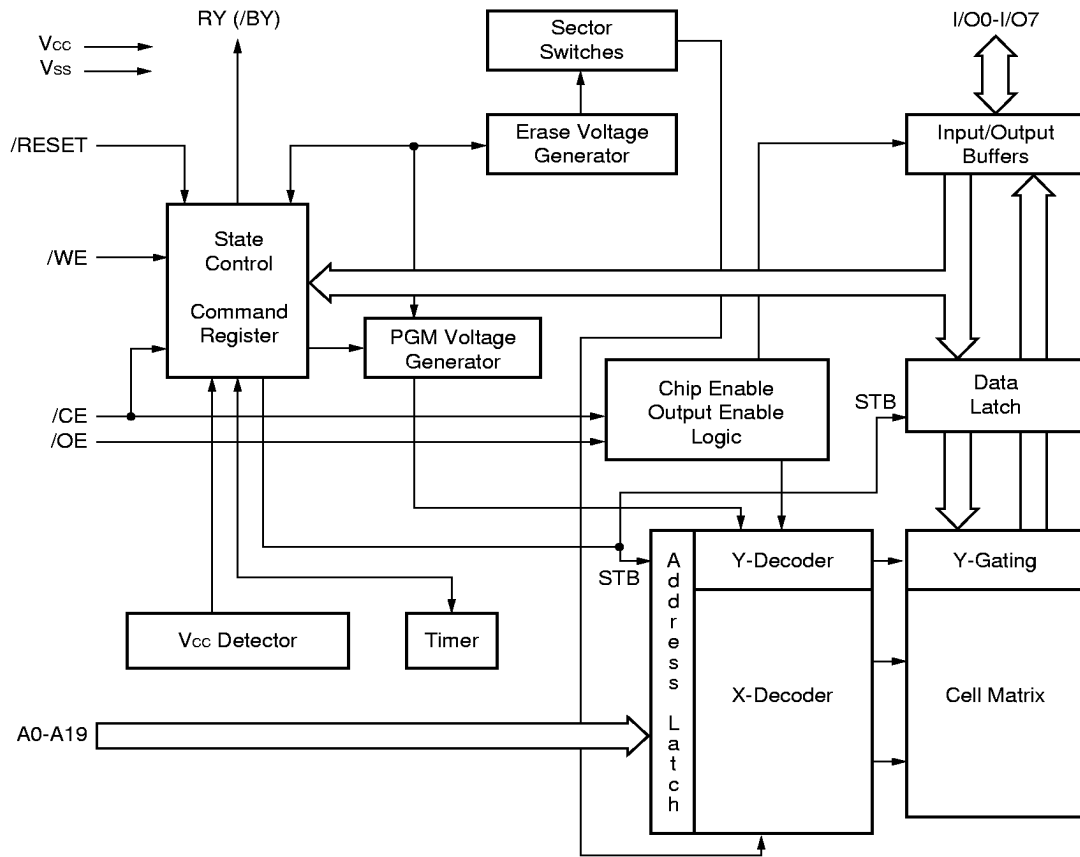
Pin Name	Inout/Output	Function
A0-A19	Input	Address inputs.
A9	Input	Address input. When A9 is at 11.5 V to 12.5 V, the signature mode is accessed. During this mode A0 decodes between the manufacturer and device IDs. A0 = "L": Manufacturer ID, A0 = "H": Device ID.
I/O0-I/O7	Input/Output	Data inputs/outputs.
/CE	Input	Chip enable signal. High level input: Standby mode
/OE	Input	Output enable signal. High level input: Output disable mode
/WE	Input	Write enable signal. Low level input: Block Erase/Program and Command input
/RESET	Input	Hardware reset input. Low level input: Reset mode
RY (/BY)	Output	The pin for indicating that automatic erase (or automatic program) operation is either in progress or have been completed. This pin is an open-drain output pin. Low level output: The device is busy with automatic erase (or automatic program) operation. High level output: The device is ready for new operations, in the erase suspend mode or in reset mode.
V <sub>cc</sub>	–	Supply voltage
GND	–	Ground
NC	–	No connecton: Not internally connected. (The signal can be connected.)

Erase Block Layout

μPD29F008Lxx-xxxT	Address
Protection Block (16 K bytes)	FFFFFH
Condition Block (8 K bytes)	FC000H FBFFFFH
Condition Block (8 K bytes)	FA000H F9FFFFH
Main Block (32 K bytes)	F8000H F7FFFFH
Main Block (64 K bytes)	F0000H EFFFFH
Main Block (64 K bytes)	E0000H DFFFFH
Main Block (64 K bytes)	D0000H CFFFFH
Main Block (64 K bytes)	C0000H BFFFFH
Main Block (64 K bytes)	B0000H AFFFFH
Main Block (64 K bytes)	A0000H 9FFFFH
Main Block (64 K bytes)	90000H 8FFFFH
Main Block (64 K bytes)	80000H 7FFFFH
Main Block (64 K bytes)	70000H 6FFFFH
Main Block (64K bytes)	60000H 5FFFFH
Main Block (64 K bytes)	50000H 4FFFFH
Main Block (64 K bytes)	40000H 3FFFFH
Main Block (64 K bytes)	30000H 2FFFFH
Main Block (64 K bytes)	20000H 1FFFFH
Main Block (64 K bytes)	10000H 0FFFFH
Main Block (64 K bytes)	00000H

μPD29F008Lxx-xxxB	Address
Main Block (64 K bytes)	FFFFFH
Main Block (64 K bytes)	F0000H EFFFFH
Main Block (64 K bytes)	E0000H DFFFFH
Main Block (64 K bytes)	D0000H CFFFFH
Main Block (64 K bytes)	C0000H BFFFFH
Main Block (64 K bytes)	B0000H AFFFFH
Main Block (64 K bytes)	A0000H 9FFFFH
Main Block (64 K bytes)	90000H 8FFFFH
Main Block (64 K bytes)	80000H 7FFFFH
Main Block (64 K bytes)	70000H 6FFFFH
Main Block (64 K bytes)	60000H 5FFFFH
Main Block (64 K bytes)	50000H 4FFFFH
Main Block (64 K bytes)	40000H 3FFFFH
Main Block (64 K bytes)	30000H 2FFFFH
Main Block (64 K bytes)	20000H 1FFFFH
Main Block (32 K bytes)	10000H 0FFFFH
Condition Block (8 K bytes)	08000H 07FFFFH
Condition Block (8 K bytes)	06000H 05FFFFH
Protection Block (16 K bytes)	04000H 03FFFFH 00000H

Block Diagram



Operation Mode

Pin Name Mode	/RESET	/CE	/OE	/WE	A9	A6	A1	A0	I/O0-I/O7
Product ID code, Manufacturer code <sup>Note</sup>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	ID
Product ID code, Device code <sup>Note</sup>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	ID
Read	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A9	A6	A1	A0	Data output
Standby	V <sub>IH</sub>	V <sub>IH</sub>	x	x	x	x	x	x	Hi-Z
Output disable	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	x	x	x	x	Hi-Z
Write	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A9	A6	A1	A0	Data input
Enable sector protect	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>H</sub>	Pulse/V <sub>IH</sub>	V <sub>H</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Code
Verify sector protect	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Code
Temporary sector unprotect	V <sub>H</sub>	x	x	x	x	x	x	x	x
Reset	V <sub>IL</sub>	x	x	x	x	x	x	x	Hi-Z

**Note** Manufacturer and device codes may also be accessed via a command register write sequence. Please refer to Command Definition.

**Remark** V<sub>H</sub> = 12.0 V ± 0.5 V  
 x : Don't care (V<sub>IH</sub> or V<sub>IL</sub>)  
 See DC characteristics for voltage levels.

ID = Data Read from Location address during Read product ID code.

- 10H : Manufacturer code
- 3EH : Device code for a Type T
- 37H : Device code for a Type B



**Operation Mode (Command Mode)**

Command Sequence	Bus Cycles	First bus Write cycle		Second bus write cycle		Third bus write cycle		Fourth bus write cycle		Fifth bus write cycle		Sixth bus write cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Reset/Read	1	xxxxH	F0H	-	-	-	-	-	-	-	-	-	-
Read product ID code	4	5555H	AAH	2AAAH	55H	5555H	90H	IA	ID	-	-	-	-
Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD	-	-	-	-
Chip erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	EA	30H
Sector erase suspend	1	xxxxH	B0H	-	-	-	-	-	-	-	-	-	-
Sector erase Resume	1	xxxxH	30H	-	-	-	-	-	-	-	-	-	-

**Remark** x: V<sub>IL</sub> or V<sub>IH</sub>

EA = Block Address of Memory Location to be erased.

PA = Address of Memory Location to be programmed.

PD = Data to be programmed at Location PA.

IA = Identifier Address (00000H: Address for Manufacturer ID, 00001H: Address for Device ID).

ID = Data Read from Location IA during Read product ID code.

10H : Manufacturer code

3EH: Device code for a Type T

37H : Device code for a Type B

**Hardware Sequence Flags**

	Status	I/O7	I/O6	I/O5	I/O3	I/O2	RY(BY)	
In progress	Programming	/I/O7	Toggle	0	0	1	0	
	Auto erase	0	Toggle	0	1	Toggle	0	
	Erase suspend	Erase sector	1	1	0	0	Toggle	1
		Non erase sector	DATA	DATA	DATA	DATA	DATA	1
	Program in suspend	/I/O7	Toggle	0	0	1	0	
Exceeded time limits	Programming	/I/O7	Toggle	1	0	1	0	
	Auto erase	0	Toggle	1	1	N/A	0	
	Program in erase suspend	/I/O7	Toggle	1	0	N/A	0	

**/DATA Polling (I/O7)**

/DATA Polling supports system software by indicating the precise end of write or erase cycles. On this support, the next write or erase cycle can be started as soon as previous cycle has completed.

• How to use /DATA Polling

<Write Operation>

- (1) After writing data by write operation, fix /WE = "H".  
(See /DATA polling During Program or Erase Operation Timing Chart.)
- (2) Compare the read data from I/O7 with just before written data.
- (3) In coincidence with the both data, μPD29F008L will complete its write cycle. Then start the next cycle. In case of still in progress, the data on I/O7 is inverted just before written data.

<Erase Operation>

- (1) After setting erase command by write operation, fix /WE = "H".  
(See /DATA polling During Program or Erase Operation Timing Chart.)
- (2) If the read data on I/O7 is "1", μPD29F008L has completed its erase cycle, and the other means erase cycle is in progress.

**Toggle Bit Function (I/O6)**

Toggle bit function supports system software by indicating the precise end of write or erase cycles, too.

• How to use Toggle bit function

- (1) After writing data by command write operation, fix /WE = "H".  
(See Toggle Bit During Program /Erase Algorithm Operation Timing Chart.)
- (2) Watch the read data on I/O6.
- (3) If the write or erase operation is in progress, the read data from I/O6 will toggle on every reading. And if the operation has completed, the read data will stop toggling.

**Exceed Timing Limit (I/O5)**

Exceed timing limit function supports system software by indicating the write or erase time has exceeded the specific limits.

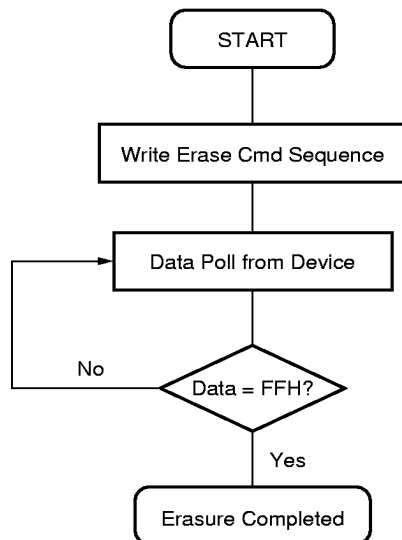
- How to use Exceed Timing Limit function
  - (1) After writing data by command write operation, fix /WE = "H".
  - (2) Watch the read data on I/O5.
  - (3) If the write or erase operation has not successfully completed, I/O5 will indicate "1".

#### **Sector Erase Timer (I/O3)**

Sector erase timer function supports system software by indicating the acceptance of sequential sector erase command write.

- How to use Sector Erase Timer function
  - (1) After writing initial sector erase command sequence, watch the data on I/O3.
  - (2) If the data on I/O3 is "1", μPD29F008L will not accept subsequent command until the erase operation is completed as indicated by Data Polling (I/O7) or Toggle Bit (I/O6).
  - (3) And if the data on I/O3 is "0", μPD29F008L will be able to accept subsequent command.

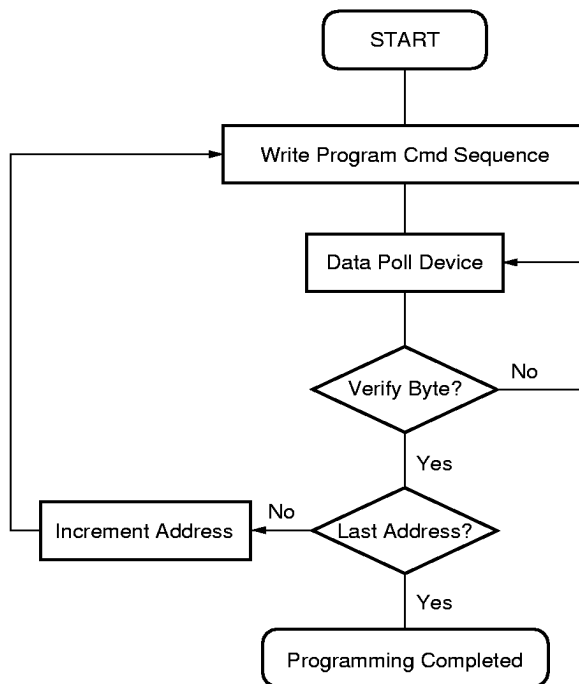
Erase Flowchart



Erase Algorithm

Bus operation	Command sequence	Comments
Standby		
Write	Erase	
Read		/DATA polling to verify erasure
Standby		Compare output to FFH.

Program Flowchart



Program Algorithm

Bus operation	Command sequence	Comments
Standby <sup>Note</sup>		
Write	Program	Valid address/data
Read		/DATA polling to verify programming
Standby <sup>Note</sup>		Compare data output to data expected

**Note** Device is either powered-down, erase inhibit, or program inhibit.

**Electrical Characteristics (Preliminary)**

**Absolute Maximum Ratings**

Parameter	Symbol	Test conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>	with respect to GND	-0.5 to +5.5	V
Input voltage	V <sub>I</sub>	with respect to GND	-0.5 <sup>Note</sup> to +5.5	V
	V <sub>I</sub>	with respect to GND, A9, /RESET, /OE	-0.5 <sup>Note</sup> to +13.5	
Output voltage	V <sub>O</sub>	with respect to GND	-0.5 <sup>Note</sup> to +5.5	V
Operating ambient temperature	T <sub>A</sub>		-20 to +70	°C
Storage temperature	T <sub>stg</sub>		-65 to +125	°C
Storage temperature (under Bias)	T <sub>bias</sub>		-20 to +80	°C

**Note** V<sub>I</sub>, V<sub>O</sub> = -2.0 V (MIN.) for pulse width ≤ 20 ns.

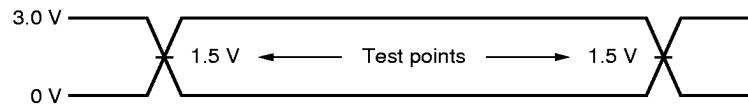
**Caution** Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

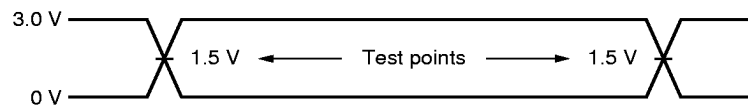
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	V <sub>IN</sub> = 0 V		6.0	7.5	pF
Output capacitance	C <sub>O</sub>	V <sub>OUT</sub> = 0 V		8.5	12.0	pF

**AC Test Conditions**

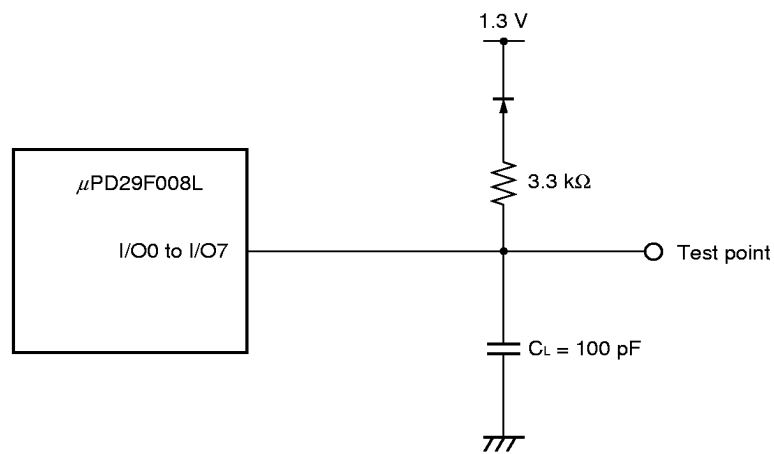
**Input Waveform (Rise/Fall time ≤ 10 ns)**



**Output Waveform**



**Output Load**



**Remark**  $C_L$  includes capacitances of the probe and jig, and stray capacitances.

Read Operation

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
High level input voltage	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5 <sup>Note1</sup>	V
Low level input voltage	V <sub>IL</sub>	-0.5 <sup>Note2</sup>		+0.8	V
Operating ambient temperature	T <sub>A</sub>	-20		+70	°C

- Notes**
1. V<sub>IH</sub> = V<sub>CC</sub> +1.0 V (MAX.) for pulse width ≤ 20 ns
  2. V<sub>IL</sub> = -1.0 V (MIN.) for pulse width ≤ 20 ns

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.0 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)	2.4			V
	V <sub>OH2</sub>	I <sub>OH</sub> = -2.0 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)	0.85V <sub>CC</sub>			V
		I <sub>OH</sub> = -100 μA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)	V <sub>CC</sub> -0.4			
Low level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 4.0 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)			0.45	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 5.8 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)			0.45	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub> , /OE = V <sub>IH</sub>	-1.0		+1.0	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		+1.0	μA
V <sub>CC</sub> supply current	I <sub>CCA1</sub>	V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub> fixed			35	mA
	I <sub>CCA2</sub>	I <sub>OUT</sub> = 0 mA, /CE = V <sub>IL</sub> , minimum cycle time			45	mA
V <sub>CC</sub> standby current	I <sub>CCS1</sub>	/CE = /RESET = V <sub>IH</sub> , V <sub>CC</sub> = V <sub>CC</sub> (MAX.)			250	μA
	I <sub>CCS2</sub>	/CE ≥ V <sub>CC</sub> -0.2 V			5	μA
Reset supply current	I <sub>CCSLP</sub>	/RESET = GND ± 0.2 V			5	μA

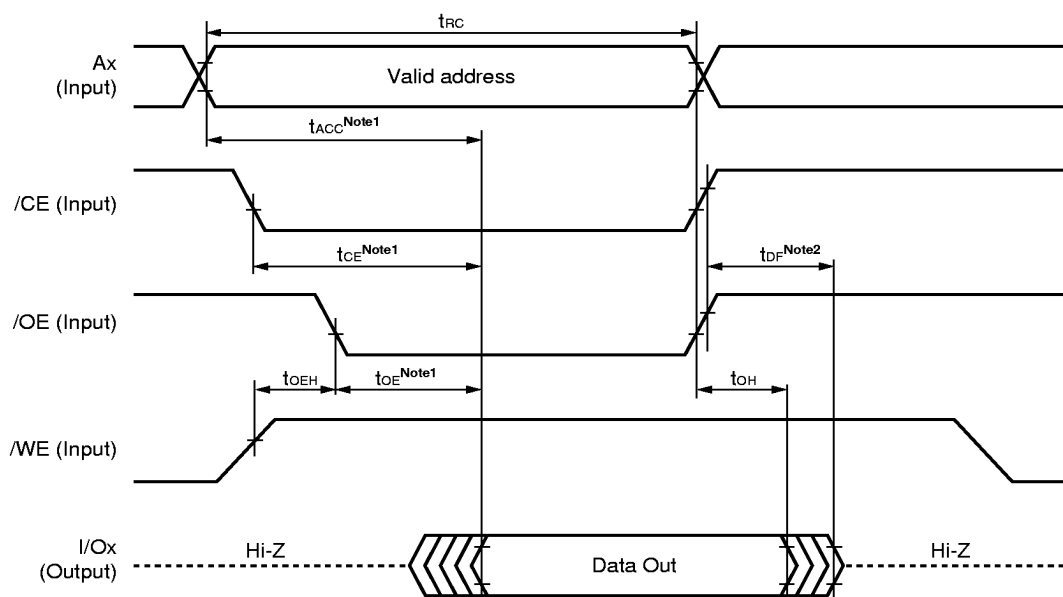


**AC Characteristics (Recommended operating conditions unless otherwise noted)**

Parameter	Symbol	Test condition	μPD29F008L-B12		μPD29F008L-B15		Unit
			MIN.	MAX.	MIN.	MAX.	
Address to output delay	$t_{ACC}$	$/CE = /OE = V_{IL}$		120		150	ns
$/CE$ to output delay	$t_{CE}$	$/OE = V_{IL}$		120		150	ns
$/OE$ to output delay	$t_{OE}$	$/CE = V_{IL}$		50		55	ns
$/OE$ or $/CE$ output float delay	$t_{DF}$	$/CE = V_{IL}$ or $/OE = V_{IL}$		30		40	ns
Address to output hold	$t_{OH}$	$/CE = /OE = V_{IL}$	0		0		ns

**Remark**  $t_{DF}$  is the time from inactivation of  $/CE$  or  $/OE$  to high-impedance state output.

**Read Mode Timing Chart**



**Notes** 1. For read operation, the definition of access time is as follows.

Access time definition	$/CE$ input condition	$/OE$ input condition
$t_{ACC}$	before stabilizing address	before ( $t_{ACC} - t_{OE}$ )
$t_{OE}$		after ( $t_{ACC} - t_{OE}$ )
$t_{CE}$	after stabilizing address	before ( $t_{CE} - t_{OE}$ )
$t_{OE}$		after ( $t_{CE} - t_{OE}$ )

2.  $t_{DF}$  is the time from inactivation of  $/CE$  or  $/OE$  to high-impedance state output.

Program and Erase Operation

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
High level input voltage 1	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5 <sup>Note1</sup>	V
High level input voltage 2	V <sub>IH</sub>	11.5		12.5	V
Low level input voltage	V <sub>IL</sub>	-0.3 <sup>Note2</sup>		+0.8	V
Operating ambient temperature	T <sub>A</sub>	-20		+70	°C

- Notes**
1. V<sub>IH</sub> = V<sub>CC</sub> +0.6 V (MAX.) for pulse width ≤ 20 ns
  2. V<sub>IL</sub> = -0.6 V (MIN.) for pulse width ≤ 20 ns

DC Characteristics (Recommended operating conditions unless otherwise noted)

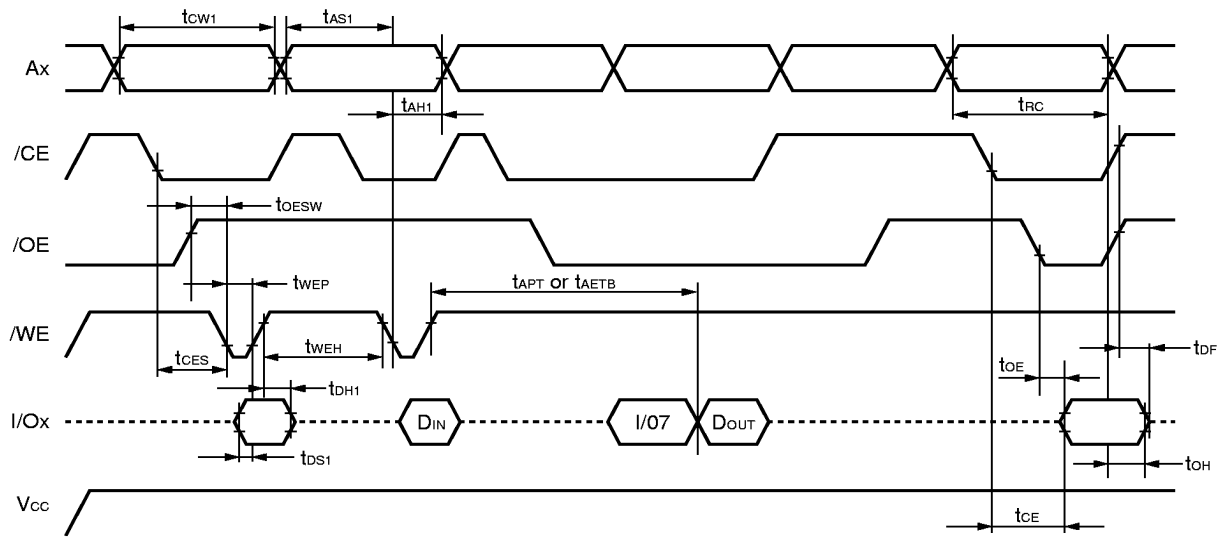
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit	
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.0 mA	2.4			V	
	V <sub>OH2</sub>	I <sub>OH</sub> = -2.0 mA	0.85V <sub>CC</sub>			V	
		I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.4			V	
Low level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 4.0 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)			0.45	V	
	V <sub>OL2</sub>	I <sub>OL</sub> = 5.8 mA, V <sub>CC</sub> = V <sub>CC</sub> (MIN.)			0.45	V	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub> , /OE = V <sub>IH</sub>	-1.0		+1.0	μA	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		+1.0	μA	
V <sub>CC</sub> supply current	Standby	I <sub>CCS1</sub>	/CE = /RESET = V <sub>IH</sub>			250	μA
		I <sub>CCS2</sub>	/CE = /RESET = V <sub>CC</sub> ± 0.2 V			5	μA
	Reset	I <sub>CCSLP</sub>	/RESET = GND ± 0.2 V			5	μA
	Read	I <sub>CCA1</sub>	I <sub>OUT</sub> = 0 mA, /CE = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub> fixed			35	mA
		I <sub>CCA2</sub>	I <sub>OUT</sub> = 0 mA, /CE = V <sub>IL</sub> , minimum cycle time			45	mA
	Program	I <sub>CCP</sub>				35	mA
	Erase	I <sub>CC E</sub>				35	mA
Low V <sub>CC</sub> lock-out voltage	V <sub>LKO</sub>		2.3		2.5	V	

AC Characteristics (1) (/WE Control) (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	μPD29F008L-B12			μPD29F008L-B15			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time	t <sub>CW1</sub>	120			150			ns
Address setup time 1	t <sub>AS1</sub>	0			0			ns
Address hold time 1	t <sub>AH1</sub>	50			65			ns
Data input setup time 1	t <sub>DS1</sub>	50			65			ns
Data input hold time 1	t <sub>DH1</sub>	0			0			ns
/OE setup time	t <sub>OES</sub>	0			0			ns
/OE hold time	Read	t <sub>OEH</sub>	0		0			ns
	Toggle and /DATA polling		10		10			ns
Read recovery time before write	t <sub>OEHC</sub>	0			0			ns
/CE setup time	t <sub>CES</sub>	0			0			ns
/CE hold time (V <sub>IL</sub> )	t <sub>CEL</sub>	0			0			ns
Write pulse width	t <sub>WEP</sub>	50			65			ns
/WE hold time	t <sub>WEH</sub>	30			35			ns
Total program time	t <sub>APT</sub>		9			9		μs
Total erase time	t <sub>AETB</sub>		1			1		s
V <sub>CC</sub> setup time	t <sub>VCS</sub>	50			50			μs
Write Recovery time from RY (/BY)	t <sub>RB</sub>	0			0			ns
/RESET low time	t <sub>RL</sub>	500			500			ns
/RESET high time before read	t <sub>PRHH</sub>	50			50			ns
/RESET to sleep time	t <sub>SLP</sub>	20			20			μs
Program/Erase valid to RY (/BY) delay	t <sub>BUSY</sub>	90			90			ns

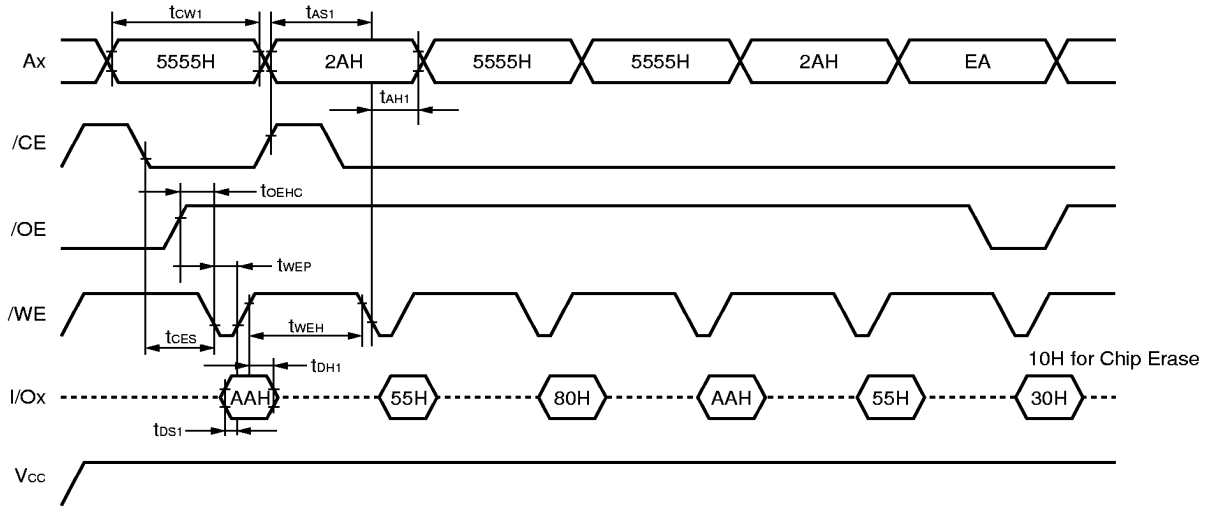
**Remark** Duration of the program or erase operation is variable and is calculated in the internal algorithms.

Write Operation Timing Chart



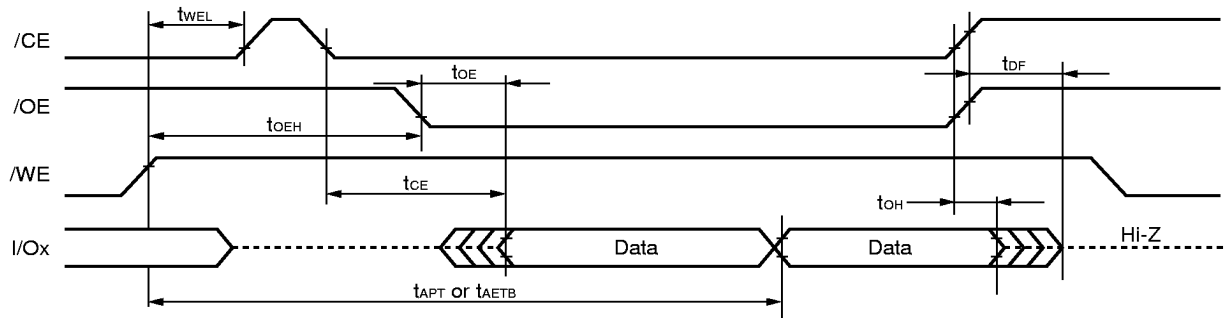
- Remarks**
1.  $D_{IN}$  is DATA input to the device.
  2.  $I/O_7$  is the output of the complement of the data written to the device.
  3.  $D_{OUT}$  is the output of the data written to the device.

Chip/Sector Erase Operation Timing Chart



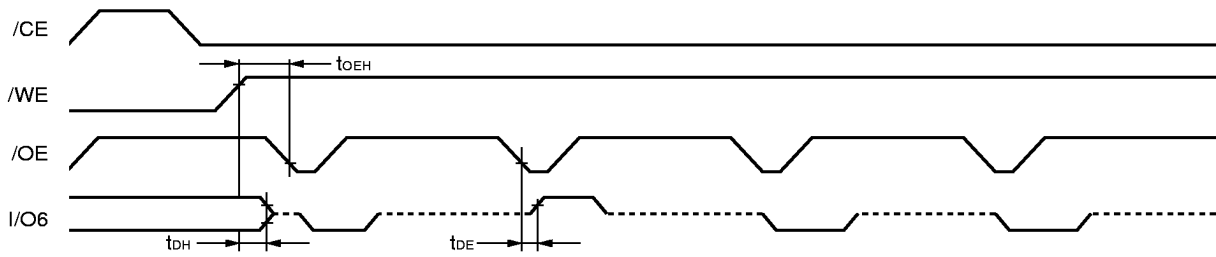
- Remarks**
- EA is the sector address for Sector Erase. Addresses = Don't care for Chip Erase.
  - These waveforms are for the word mode.

/Data Polling During Program or Erase Operation Timing Chart



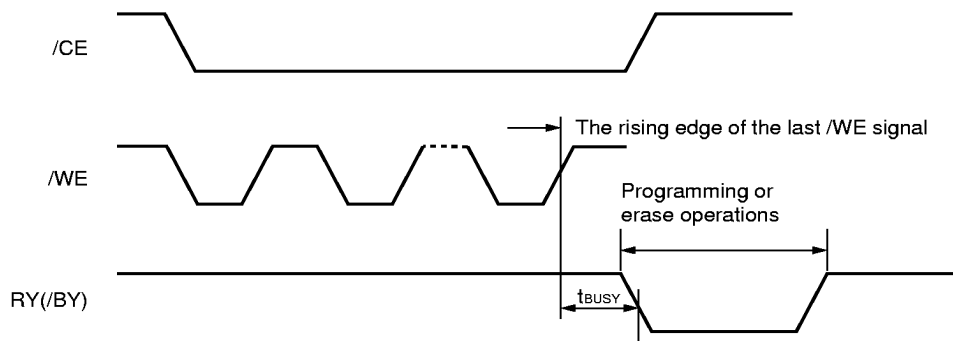
**Remark** I/O7 = Valid Data (The device has completed the Program or Erase operation).

**Toggle Bit During Program/Erase Algorithm Operation Timing Chart**

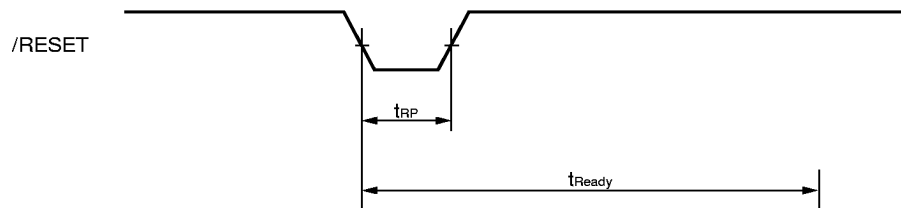


**Remark** I/O6 stops toggling (The device has completed the Program or Erase operation).

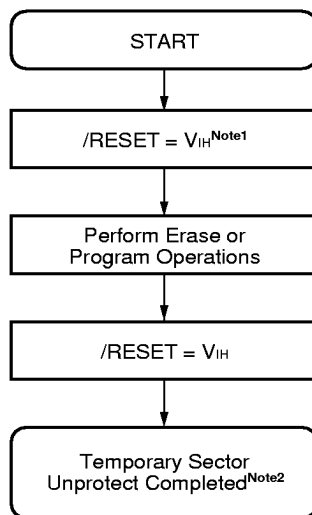
**RY (/BY) Timing Chart Program/Erase Operation**



**/Reset Timing Chart**

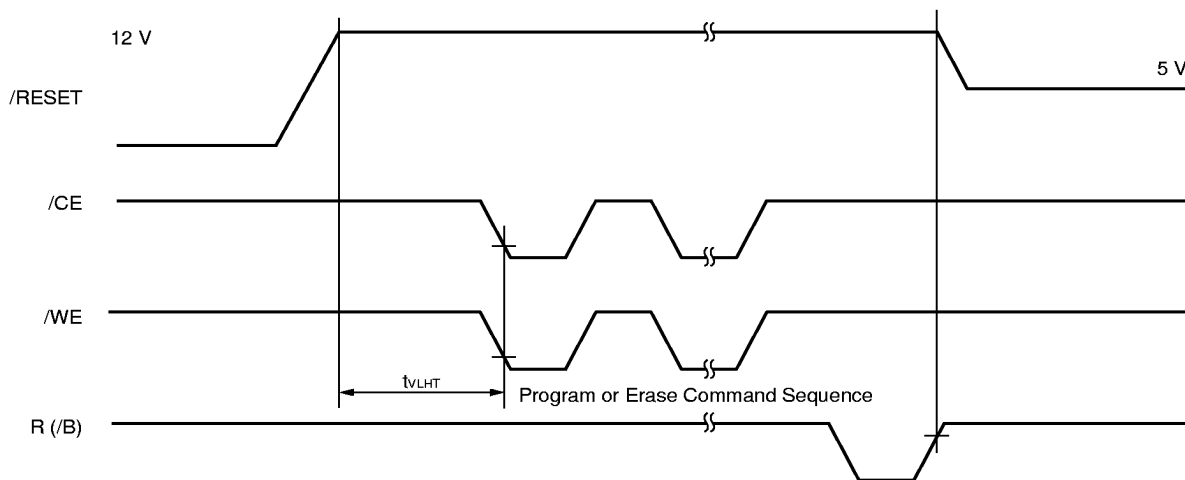


Temporary Sector Unprotect Flowchart



- Notes**
- 1. All protected sectors unprotected.
  - 2. All previously protected sectors are protected once again.

Temporary Sector Unprotect Timing Chart



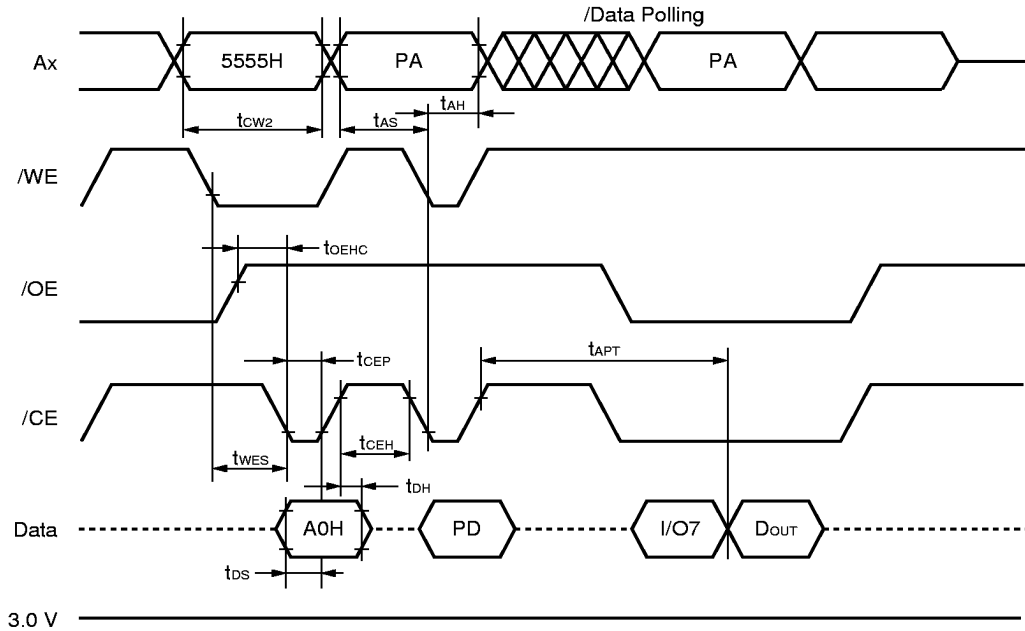
AC Characteristics (2) (/CE Control) (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	μPD29F008L-B12			μPD29F008L-B15			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write cycle time	t <sub>CW2</sub>	120			150			ns
Address setup time 2	t <sub>AS2</sub>	0			0			ns
Address hold time 2	t <sub>AH2</sub>	50			50			ns
Data input setup time 2	t <sub>DS2</sub>	50			50			ns
Data input hold time 2	t <sub>DH2</sub>	0			0			ns
/OE setup time	t <sub>OES</sub>	0			0			ns
/OE hold time	Read	t <sub>OEH</sub>	0		0			ns
	Toggle and /DATA polling		10		10			ns
Read recovery time before write	t <sub>OEHC</sub>	0			0			ns
/WE setup time	t <sub>WES</sub>	0			0			ns
/WE hold time (V <sub>IL</sub> )	t <sub>WEL</sub>	0			0			ns
/CE pulse width	t <sub>CEP</sub>	50			50			ns
/CE pulse width high	t <sub>CEH</sub>	20			20			ns
Total program time	t <sub>APT</sub>		9			9		μs
Total erase time <sup>Note</sup>	t <sub>AETB</sub>		1	10		1	10	s

**Note** This does not include the preprogramming time.



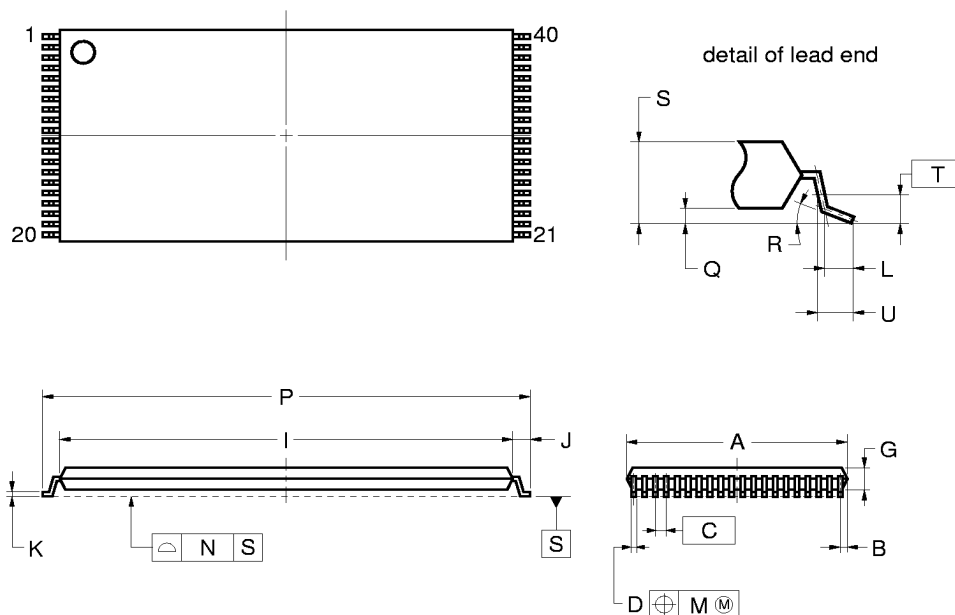
Alternate /CE Controlled Write Operation Timing Chart



- Remarks**
1. PA is address of the memory location to be programmed.
  2. PD is data to be programmed at byte address.
  3. I/O7 is the output of the complement of the data written to the device.
  4. DOUT is the output of the data written to the device.
  5. Figure indicates last two bus cycles of four bus cycle sequence.
  6. These waveforms are for the word mode.

Package Drawings

★ 40 PIN PLASTIC TSOP(I) (10x20)



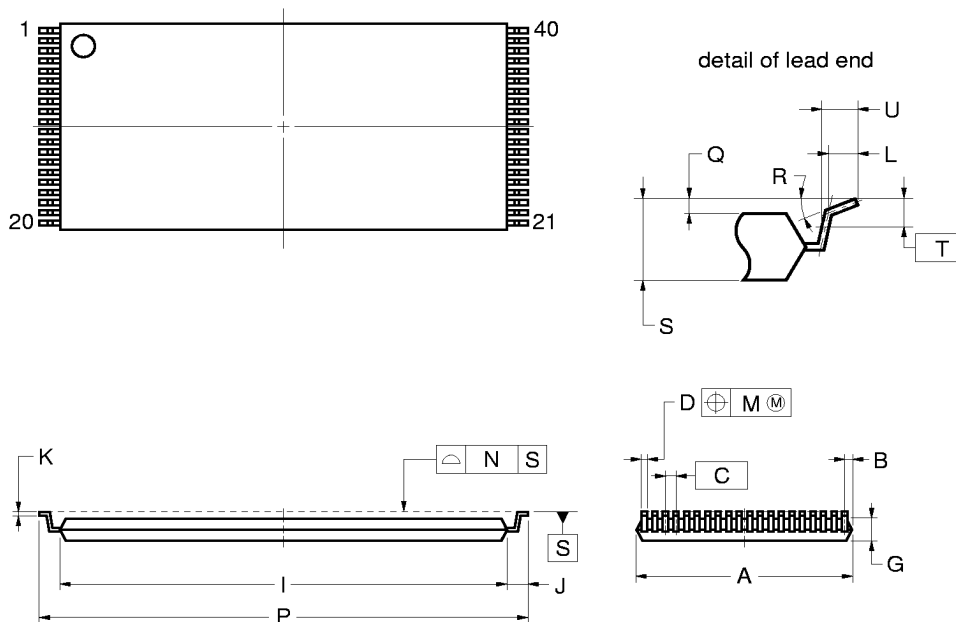
NOTES

1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 10.4 mm MAX. <0.410 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	10.0±0.1	0.394 <sup>+0.004</sup> <sub>-0.005</sub>
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	0.009 <sup>+0.002</sup> <sub>-0.003</sub>
G	0.97±0.05	0.038 <sup>+0.003</sup> <sub>-0.002</sub>
I	18.4±0.1	0.724 <sup>+0.005</sup> <sub>-0.004</sub>
J	0.8±0.1	0.031 <sup>+0.005</sup> <sub>-0.004</sub>
K	0.145±0.05	0.006 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	0.787 <sup>+0.009</sup> <sub>-0.008</sub>
Q	0.1±0.05	0.004 <sup>+0.002</sup> <sub>-0.003</sub>
R	3° <sup>+5°</sup> <sub>-3°</sub>	3° <sup>+5°</sup> <sub>-3°</sub>
S	1.2 MAX.	0.047 MAX.
T	0.25	0.010
U	0.6±0.15	0.024 <sup>+0.006</sup> <sub>-0.007</sub>

S40GZ-50-LJH1

★ 40 PIN PLASTIC TSOP(I) (10x20)



NOTES

1. Controlling dimension — millimeter.
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T	0.25	0.010
U	0.6±0.15	0.024 <sup>+0.006</sup> <sub>-0.007</sub>

S40GZ-50-LKH1