

Description

The μPD4362B is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD4362B a high-speed device that requires very low power and no clock or refreshing.

The μPD4362B is packaged in a standard 22-pin plastic DIP and 24-pin plastic SOJ.

Features

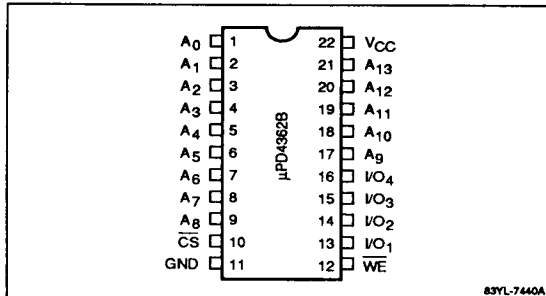
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Standard 300-mil, 22-pin plastic DIP and 24-pin plastic SOJ packaging

Ordering Information

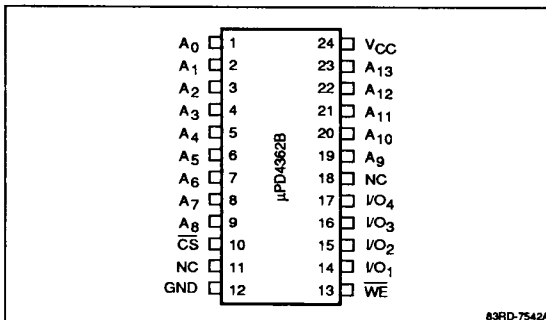
Part Number	Access Time (max)	Package
μPD4362BCR-12	12 ns	22-pin plastic DIP
CR-15	15 ns	
CR-20	20 ns	
μPD4362BLA-12	12 ns	24-pin plastic SOJ
LA-15	15 ns	
LA-20	20 ns	

Pin Configuration

22-Pin Plastic DIP



24-Pin Plastic SOJ



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Pin Identification

Symbol	Function
A ₀ - A ₁₃	Address inputs
I/O ₁ - I/O ₄	Data inputs and outputs
CS	Chip select
WE	Write enable
GND	Ground
V _{CC}	+ 5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{CC}	- 0.5 to + 7.0 V
Input and output voltages, V_{IN} (Note 1)	- 0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to + 70°C
Storage temperature, T_{STG}	- 55 to + 125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

- (1) $V_{IN} = -3.0 \text{ V}$ for 10 ns pulse.

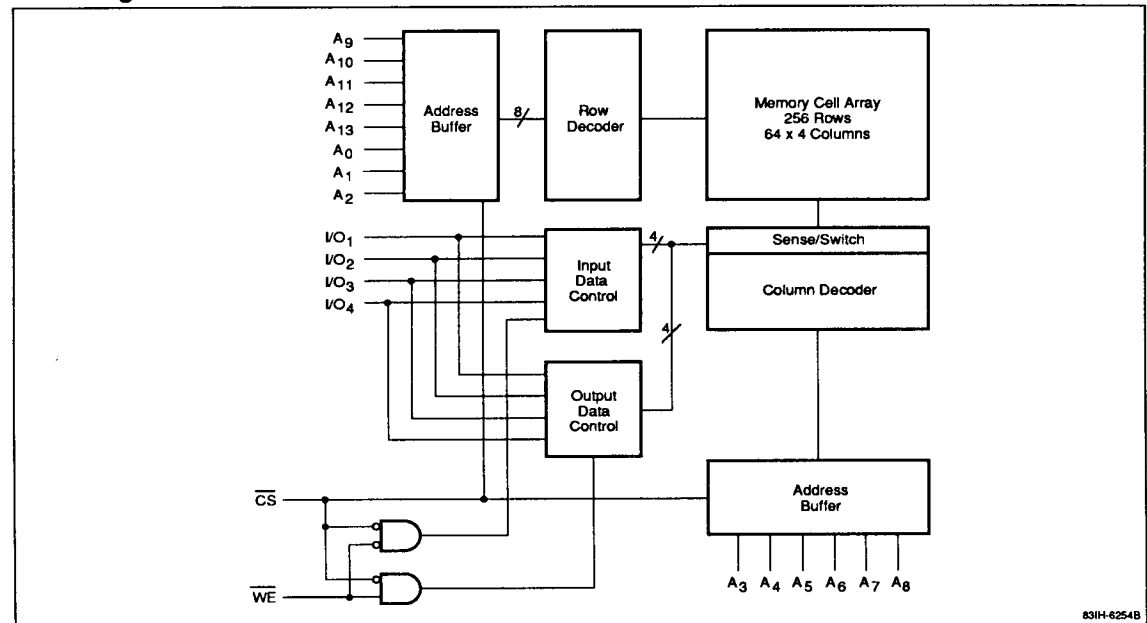
Truth Table

Function	$\overline{\text{CE}}$	$\overline{\text{WE}}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

Notes:

- (1) $X = \text{don't care.}$

Block Diagram



Capacitance

$T_A = 25^{\circ}\text{C}$; $f = 1\text{ MHz}$ (Note 1); V_{IN} and $V_{\text{DOUT}} = 0\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C _{IN}			6	pF
Output capacitance	C _{DOUT}			8	pF

Notes:

- (1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2	$V_{CC} + 0.3$		V
Input voltage, low	V_{IL}	-0.5	0.8		V
Operating temperature	T_A	0	70		°C

Notes:

- (1) $V_{IL} = -3.0 \text{ V}$ for 10 ns pulse.

DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-2		2	μA	$V_{IN} = 0 \text{ V to } V_{CC}; V_{CC} = \text{max}$
Output leakage current	I_{LO}	-2		2	μA	$V_{OUT} = 0 \text{ V to } V_{CC}; \overline{CS} = V_{IH}; V_{CC} = \text{max}$
Standby supply current	I_{SB}			20	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}; V_{IN} \leq 0.2 \text{ V or } \geq V_{CC} - 0.2 \text{ V}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0 \text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0 \text{ mA}$

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	μPD4362B-12		μPD4362B-15		μPD4362B-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Operating supply current	I _{CC}		130		120		110	mA	$\overline{CS} = V_{IL}; I_{DOUT} = 0 \text{ mA}$
Read cycle time	t _{RC}	12		15		20		ns	(Note 2)
Address access time	t _{AA}		12		15		20	ns	
Chip selection access time	t _{ACS}		12		15		20	ns	
Output hold from address change	t _{OH}	2		3		3		ns	
Chip selection to output to low-Z	t _{LZ}	2		3		3		ns	(Note 3)
Chip deselection to output to high-Z	t _{HZ}	0	7	0	7	0	8	ns	(Note 4)
Chip selection to power-up time	t _{PU}	0		0		0		ns	
Chip deselection to power-down time	t _{PD}	0	7	0	15	0	20	ns	
Write Operation									
Write cycle time	t _{WC}	12		15		20		ns	(Note 2)
Chip selection to end of write	t _{CW}	11		13		15		ns	
Address valid to end of write	t _{AW}	11		13		15		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	10		12		14		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	7		7		8		ns	
Data hold time	t _{DH}	0		0		0		ns	
Write enable to output in high-Z	t _{WZ}	0	7	0	7	0	8	ns	(Note 4)
Output active from end of write	t _{OW}	0		0		0		ns	(Note 3)

Notes:

- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.
- (3) Transition is measured at $\pm 200 \text{ mV}$ from steady-state voltage with the loading shown in figure 2.
- (4) Transition is measured at $V_{OL} + 200 \text{ mV}$ and $V_{OH} - 200 \text{ mV}$ with the loading shown in figure 2.

Figure 1. Output Load

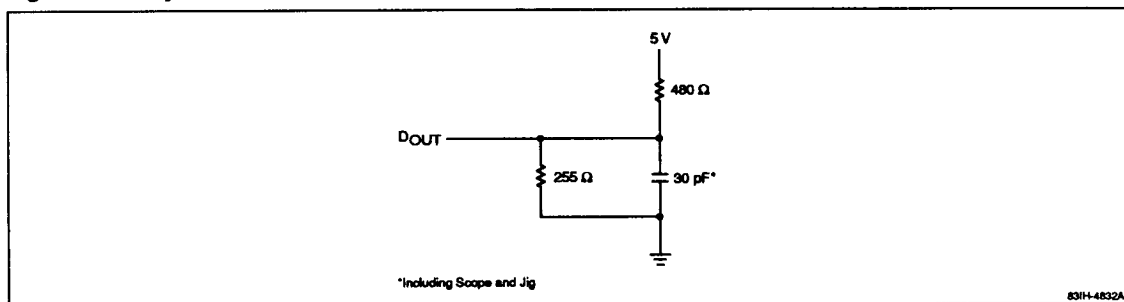
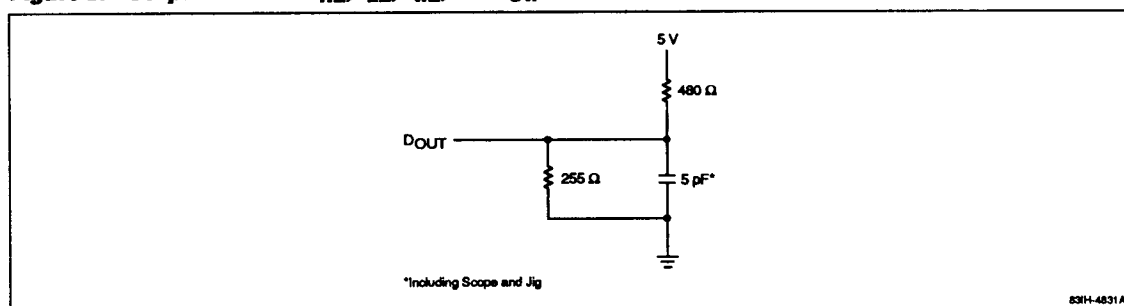
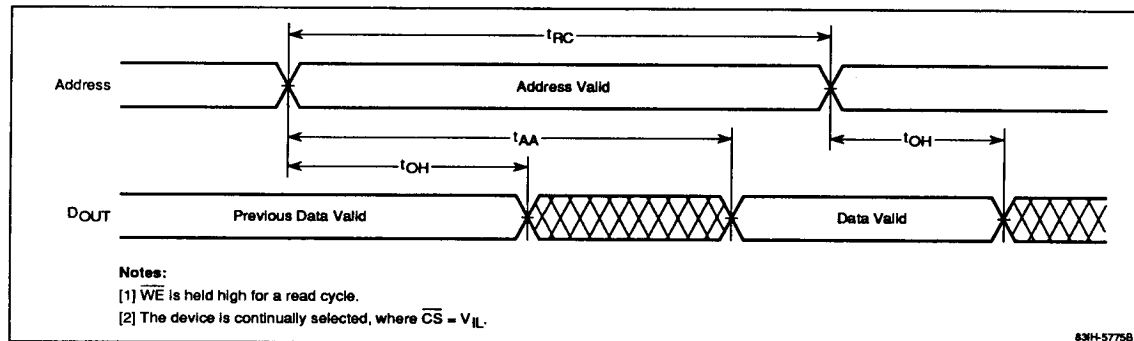


Figure 2. Output Load for t_{HZ} , t_{LZ} , t_{WZ} , and t_{OW}

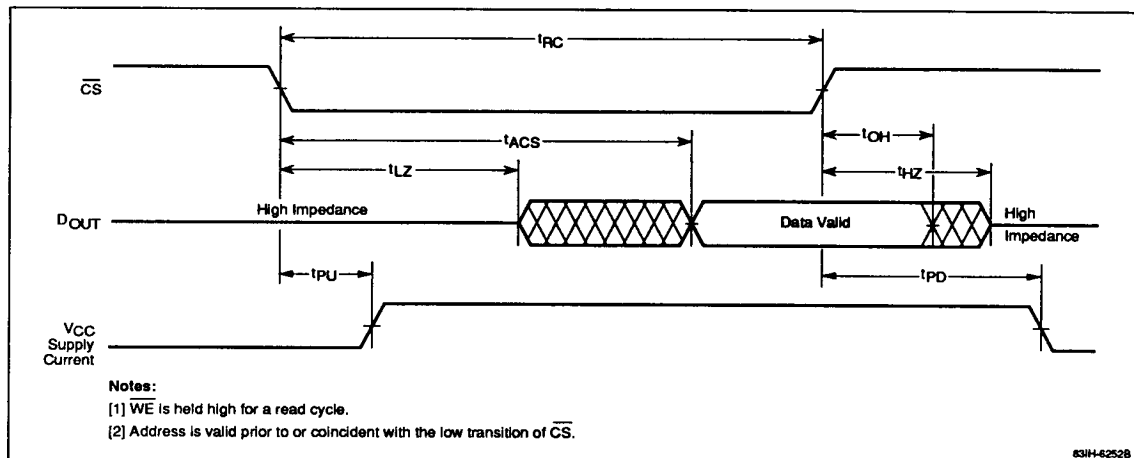


Timing Waveforms

Address Access Cycle



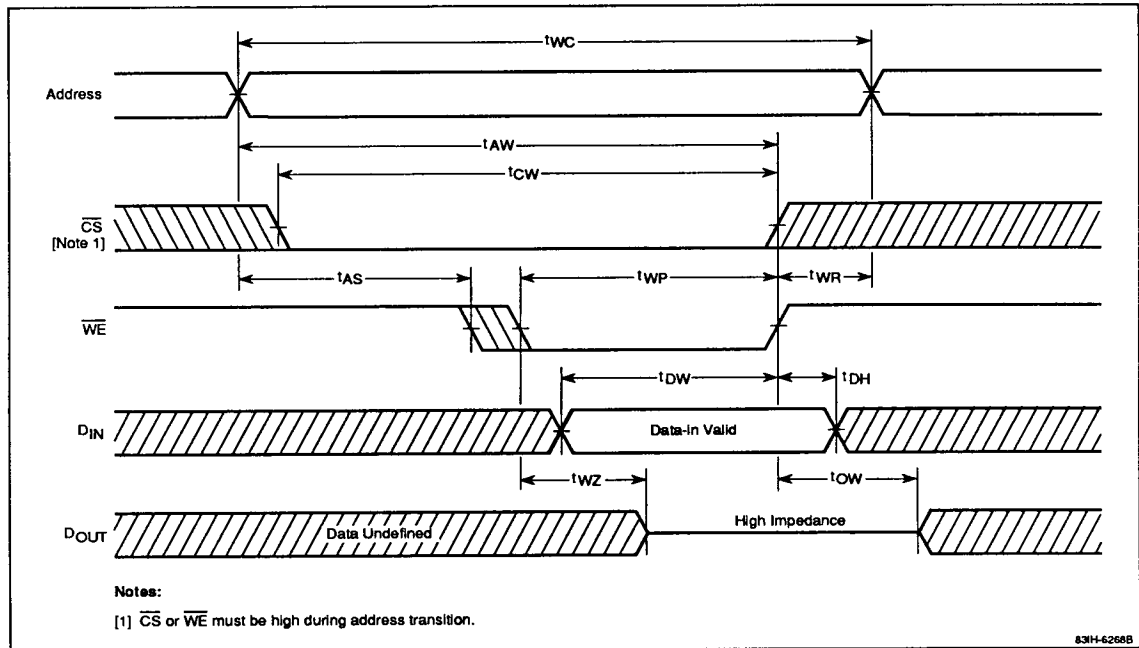
Chip Select Access Cycle



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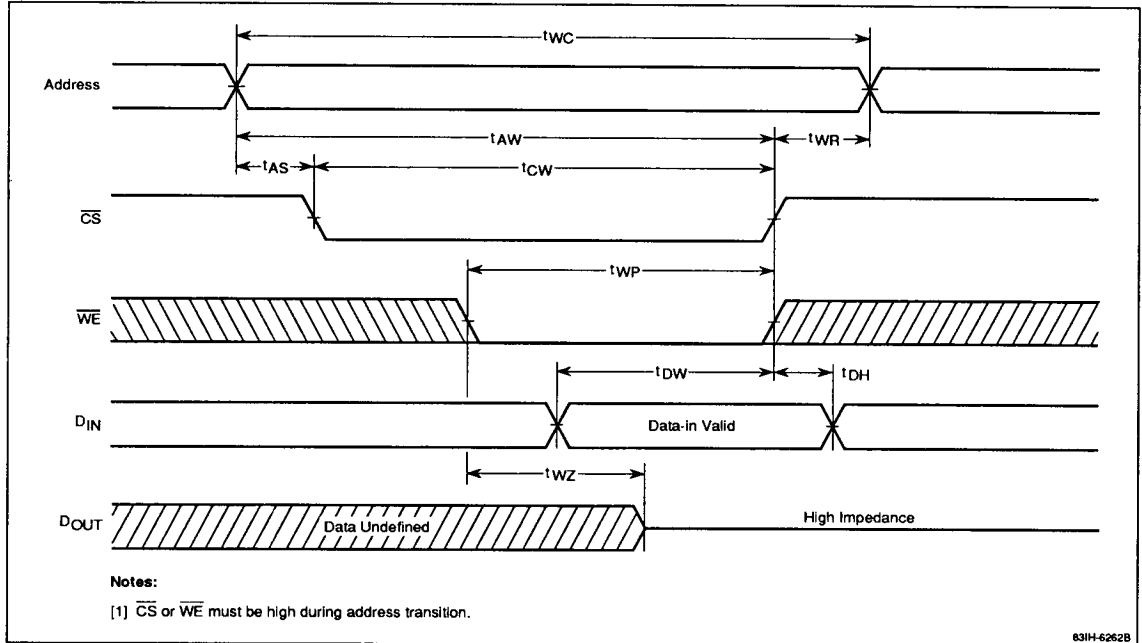
Timing Waveforms (cont)

$\overline{WE}$ -Controlled Write Cycle



Timing Waveforms (cont)

$\overline{CS}$ -Controlled Write Cycle



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