SBE, INC.
MICROCOMPUTER BOARDS AND SYSTEMS

SBE'S VBIC and VSAM GATE ARRAYS
A VMEbus INTERFACE CHIP SET

ADVANCE INFORMATION

VME boards are too small. That, plus the complications of an asynchronous bus interface, has caused board designers to compromise between complete VMEbus support and on-board functionality. And then there's the myriad of jumpers to determine the board's memory address range, I/O space addresses, interrupt lines received, interrupts generated, bus arbitration selection, etc.

SBE provides the solution to all of these problems with a two chip set, the VBIC and VSAM. Together these gate arrays provide the local processor a fully functional bus interface in accordance with VMEbus Specification C.1 while saving a substantial portion of the space required for VMEbus logic. In addition, they support local interrupt handling, multiprocessor communications control, and Slot-1 bus functions. All parameters for both the VBIC and VSAM are set through an 8-bit interface to the local processor, eliminating all jumper requirements except, perhaps, one to enable or disable the Slot-1 functions.

The slave and master capabilities of the VMEbus have been carefully partitioned between the VSAM and VBIC to allow the board designer to use one or both gate arrays as appropriate. The VBIC supplies VMEbus requester, interrupt controller, and Slot-1 functions while the VSAM decodes and remaps VMEbus addresses for access to shared memory, status registers, a mailbox register, and the VMEbus location monitor. Intelligent VMEbus boards that are intended to be exclusively a bus master or a slave can use just one chip and have even more board space available for local functions.

The VBIC and VSAM require only four buffer/driver/receiver chips to interface to the VMEbus and may be directly connected to the local processor's interrupt lines, address and data buses. VMEbus address buffers and timing logic within the VSAM simplifies the task of interfacing to DRAM or SRAM for shared memory.

VBIC FUNCTIONS

- VMEbus Requester
  - Programmable request level (BR0*-BR3*)
  - 2 Programmable release modes
  - Read-Modify-Write transfers supported
- VMEbus Interrupt Generator
  - VMEbus level, 1 to 7, and STATUS/ID programmable
- 68000 Interrupt Controller
  - 7 VMEbus interrupts may be assigned to levels 1-6
  - 10 local interrupt sources, level or edge triggered, 8 may be assigned to levels 1-6, 2 to levels 1-7
  - NMI connections for a SPDT switch
  - Programmable interrupt vectors, autovector, internal vector (within VBIC), or external vector
  - Interval timer with interrupts at 1 or 10 ms intervals
- Slot 1 functions
  - Bus arbitration on fixed priority, round robin or priority round robin
  - Bus timeout timer values from 16us to 128us
  - IACK daisy chain driver

VSAM FUNCTIONS

- Slave address manager for A24 or A32 access support
  - Read-Modify-Write cycles
  - Shared RAM support for SRAM and DRAM
  - Block Move Transfers in D16 and D32 modes
- 16 Independent Mailbox bits
  - Interrupt generated on VMEbus write
  - Interrupt cleared on write by local processor
- Local board status, reset, and I/O registers
- VMEbus Location Monitor
  - Programmable base address, range, and address modifiers
  - Programmable counter controls frequency of generated interrupt