Features

- SPARC V8 High Performance Low-power 32-bit Architecture
  - LEON2-FT 1.0.13 compliant
  - 8 Register Windows
- Advanced Architecture:
  - On-chip Amba Bus
  - 5 Stage Pipeline
  - 16 kbyte Multi-sets Data Cache
  - 32 kbyte Multi-sets Instruction Cache
- On-chip Peripherals:
  - Memory Interface
    - PROM Controller
    - SRAM Controller
    - SDRAM Controller
  - Timers
    - Two 24-bit Timers
    - Watchdog Timer
  - Two 8-bit UARTs
  - Interrupt Controller with 4 External Programmable Inputs
  - 32 Parallel I/O Interface
  - 33MHz PCI Interface Compliant with 2.2 PCI Specification
- Integrated 32/64-bit IEEE 754 Floating-point Unit
- Fault Tolerance by Design
  - Full Triple Modular Redundancy (TMR)
  - EDAC Protection
  - Parity Protection
- Debug and Test Facilities
  - Debug Support Unit (DSU) for Trace and Debug
  - IEEE 1149.1 JTAG Interface
  - Four Hardware Watchpoints
- Speed Optimized Code RAM Interface
  8, 16 and 40-bit boot-PROM (Flash) Interface Possibilities
- Clock: 0MHz up to 100MHz
- Core consumption: 1W
- Performance: 100 MIPS
- Operating range
  - Voltages
    - 3.3V +/- 0.30V for I/O
    - 1.8V +/- 0.15V for Core
  - Temperature
    - -55°C to 125°C
- Radiation Performance
  - Total dose radiation capability (parametric & functional): 100Krads (Si) (target)
  - SEU event rate better than 1 E-5 error/device/day (target)
  - Latch up immunity better than 70 MeV.cm²/mg
- Package MCGA 349
- Mass: 9g

Rad-Hard 32 bit SPARC V8 Processor

AT697E

Advance Information

Summary

Rev. 4226BS–AERO–01/05

Note: This is a summary document. Contact ATMEL for a complete document.

Description

The AT697 is a highly integrated, high-performance 32-bit RISC embedded processor based on the SPARC V8 architecture. The implementation is based on the European Space Agency (ESA) LEON2 fault tolerant model. By executing powerful instructions in a single clock cycle, the AT697 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AT697 is designed to be used as a building block in computers for on-board embedded real-time applications. It brings up-to-date functionality and performance for space application.

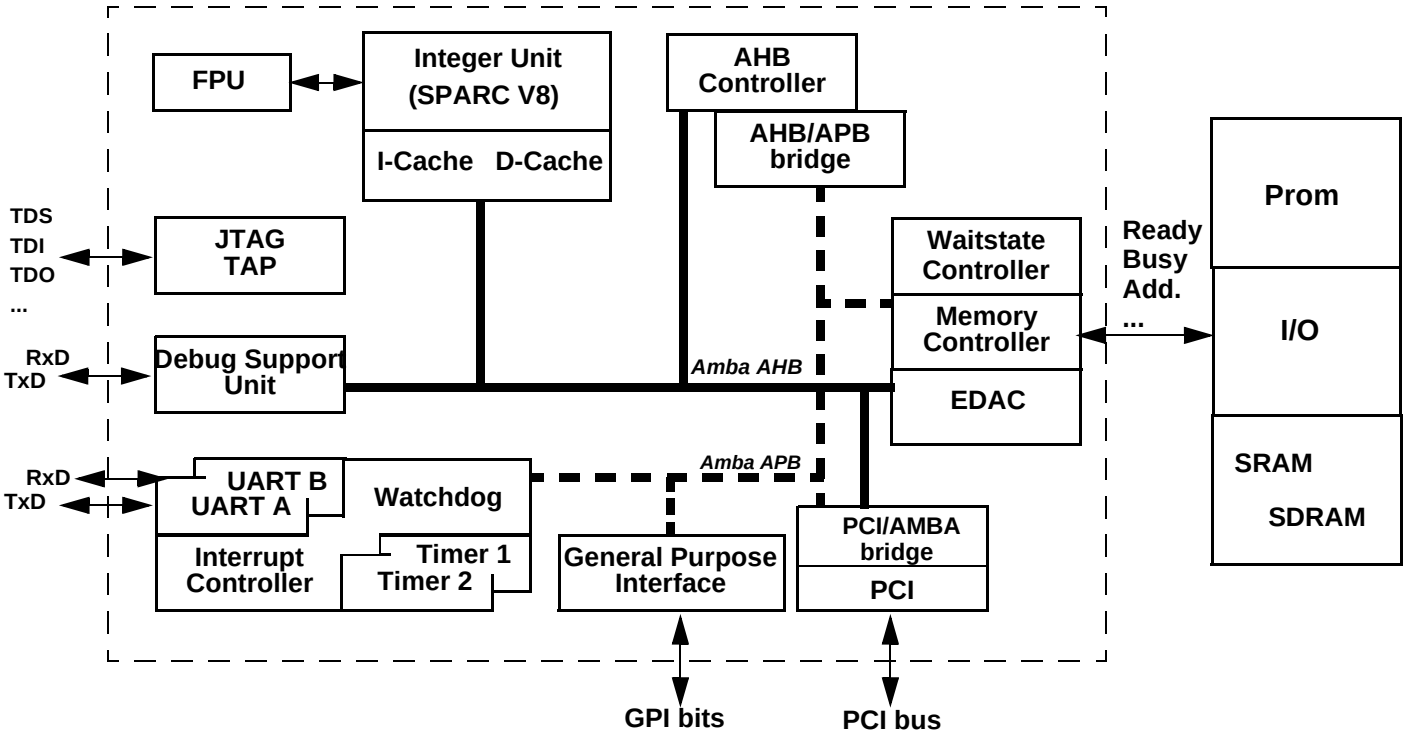
The AT697 only requires memory and application specific peripherals to be added to form a complete on-board computer.

The AT697 contains an on-chip Integer Unit (IU), a Floating Point Unit (FPU), separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 24-bit timers, Parallel and Serial interfaces, a Watchdog, a PCI Interface and a flexible Memory Controller. The design is highly testable with the support of a Debug Support Unit (DSU) and a boundary scan through JTAG interface.

An idle mode stops the CPU while allowing Timer/Counter, Serial ports and Interrupt system to continue functioning.

The processor is manufactured using the Atmel 0.18 µm CMOS process. It has been especially designed for space, by implementing on-chip concurrent transient and permanent error detection and correction.

Figure 1. AT697 Block Diagram



Pin Configuration

Table 1. AT697 pinout

	A	B	C	D	E	F	G
1			VDD18	VSS18	PIO[6]	PIO[1]	$\overline{\text{RAMS[1]}}$
2		VSS18	VDD18	PIO[0]	N.C.	PIO[4]	$\overline{\text{RAMS[2]}}$
3	VDD18	VDD18	VSS18	VCC33	PIO[2]	N.C.	$\overline{\text{RAMOE[3]}}$
4	VSS18	VDD18	PIO[9]	N.C.	PIO[5]	PIO[3]	$\overline{\text{RAMS[4]}}$
5	N.C.	N.C.	PIO[11]	N.C.	N.C.	VSS33	$\overline{\text{RAMOE[1]}}$
6	PIO[13]	PIO[10]	VCC33	Reserved	CB[0]	N.C.	VSS33
7	CB[1]	VSS33	N.C.	PIO[15]	VSS33	PIO[12]	PIO[7]
8	CB[6]	CB[4]	D[2]	VCC33	CB[7]	CB[2]	PIO[8]
9	D[3]	N.C.	D[1]	VSS33	D[6]	VCC33	CB[3]
10	D[8]	D[5]	VCC33	VSS33	Reserved	D[10]	D[4]
11	D[12]	VSS33	VCC33	D[13]	D[7]	D[15]	N.C.
12	D[17]	D[18]	D[11]	VSS33	D[14]	D[16]	D[19]
13	D[21]	D[23]	VCC33	VCC33	VSS33	VSS33	A[1]
14	D[25]	N.C.	D[22]	D[27]	N.C.	VSS33	A[3]
15	D[30]	N.C.	D[26]	D[29]	N.C.	N.C.	A[12]
16	VSS18	VSS18	D[28]	VCC33	N.C.	N.C.	A[6]
17	VDD18	VDD18	VSS18	D[31]	N.C.	A[7]	VSS33
18		VSS18	VDD18	VCC33	A[0]	A[4]	A[8]
19			VDD18	VSS18	A[2]	VSS33	A[9]

Table 2. AT697 pinout (suite)

	H	J	K	L	M	N	P
1	$\overline{\text{RAMOE[0]}}$	VSS33	READ	DSUACT	$\overline{\text{BEXC}}$	VCC33	$\overline{\text{SDWE}}$
2	$\overline{\text{RAMOE[2]}}$	$\overline{\text{ROMS[1]}}$	TCK	DSURX	SDCLK	VSS33	PCI_CLK
3	VCC33	$\overline{\text{ROMS[0]}}$	TDI	DSUTX	DSUBRE	SDDQM[1]	VSS33
4	$\overline{\text{RAMOE[4]}}$	$\overline{\text{RWE[0]}}$	TDO	DSUEN	SDDQM[2]	N.C.	$\overline{\text{SDCS[0]}}$
5	$\overline{\text{RWE[1]}}$	$\overline{\text{WRITE}}$	VSS33	TMS	N.C.	SDDQM[3]	$\overline{\text{SDCAS}}$
6	$\overline{\text{RWE[3]}}$	$\overline{\text{RWE[2]}}$	$\overline{\text{IOS}}$	VSS33	VSS33	$\overline{\text{GNT}}$	A/D[24]
7	$\overline{\text{RAMS[0]}}$	N.C.	TRST	SDDQM[0]	VSS33	VCC33	A/D[30]
8	$\overline{\text{RAMS[3]}}$	VCC33	$\overline{\text{OE}}$	$\overline{\text{BRDY}}$	VCC33	A/D[21]	A/D[18]
9	CB[5]	PIO[14]	VSS33	$\overline{\text{SDRAS}}$	A/D[22]	A/D[16]	A/D[17]
10	D[9]	D[0]	N.C.	A/D[14]	VSS33	$\overline{\text{PERR}}$	$\overline{\text{IRDY}}$
11	D[20]	A[5]	A[16]	N.C.	A/D[12]	A/D[9]	A/D[15]

	H	J	K	L	M	N	P
12	D[24]	A[14]	A[26]	VDD_PLL	$\overline{\text{AGNT[3]}}$	A/D[1]	A/D[8]
13	N.C.	VCC33	A[21]	N.C.	N.C.	VSS33	A/D[5]
14	A[10]	VCC33	A[27]	LOCK	SKEW[1]	A/D[0]	$\overline{\text{AGNT[1]}}$
15	N.C.	VSS33	VCC33	A[24]	Reserved	BYPASS	CLK
16	A[11]	VSS33	A[23]	$\overline{\text{RESET}}$	LFT	$\overline{\text{AREQ[2]}}$	VSS33
17	A[19]	A[17]	VSS33	VCC33	$\overline{\text{WDOG}}$	N.C.	VSS33
18	A[13]	A[18]	A[22]	VSS33	VSS_PLL	$\overline{\text{AREQ[3]}}$	N.C.
19	A[15]	A[20]	A[25]	$\overline{\text{ERROR}}$	SKEW[0]	VCC33	$\overline{\text{AREQ[1]}}$

Table 3. AT697 pinout (suite 2)

	R	T	U	V	W
1	$\overline{\text{REQ}}$	VSS18	VDD18		
2	N.C.	$\overline{\text{SDCS[1]}}$	VDD18	VSS18	
3	$\overline{\text{PCI\_RST}}$	A/D[31]	VSS18	VDD18	VDD18
4	N.C.	A/D[29]	VCC33	VSS18	VSS18
5	N.C.	N.C.	A/D[26]	N.C.	A/D[28]
6	N.C.	A/D[27]	IDSEL	VSS33	A/D[25]
7	$\overline{\text{SYSEN}}$	VSS33	VCC33	$\overline{\text{C/BE[3]}}$	A/D[23]
8	VSS33	VSS33	$\overline{\text{FRAME}}$	A/D[20]	A/D[19]
9	$\overline{\text{TRDY}}$	VCC33	N.C.	$\overline{\text{C/BE[2]}}$	VSS33
10	$\overline{\text{PCI\_LOCK}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{STOP}}$	VCC33	VCC33
11	VSS33	VCC33	VSS33	$\overline{\text{C/BE[1]}}$	$\overline{\text{SERR}}$
12	N.C.	A/D[11]	PAR	VSS33	A/D[13]
13	VCC33	A/D[7]	A/D[10]	VSS33	VSS33
14	VCC33	VSS33	$\overline{\text{C/BE[0]}}$	A/D[4]	A/D[6]
15	N.C.	A/D[2]	VCC33	N.C.	A/D[3]
16	N.C.	VCC33	N.C.	VDD18	VSS18
17	VCC33	$\overline{\text{AGNT[0]}}$	VSS18	VDD18	VDD18
18	N.C.	$\overline{\text{AGNT[2]}}$	VDD18	VSS18	
19	$\overline{\text{AREQ[0]}}$	VSS18	VDD18		

Notes: 1. ‘Reserved’ pins shall not be driven to any voltage
2. N.C. refers to unconnected pins

Pin Description

IU and FPU Signals

A[27:0] - Address bus (output)

A[27:0] bus carries the addresses during accesses on the memory. When no access is performed to external memory, the address of the last access is driven.

D[31:0] - Data bus (bi-directional)

D[31:0] bus carries the data during transfers on the memory. The processor only drives the bus during write cycles. During accesses to 8-bit areas, only D[31:24] are used.

CB[7:0] - Check bits (bi-directional)

CB[6:0] bus carries the EDAC checkbits during memory accesses. CB[7][1] takes the value of tcb[7] in the error control register. Processor only drives CB[7:0] during write cycles to areas programmed to be EDAC protected.

Note: 1. CB[7] is implemented to enable programming of flash memories. When only 7 bits are useful for EDAC protection, 8 are needed for programming.

Memory Interface Signals

General management

OE* - Output enable (output)

This active low output is asserted during read cycles on the memory bus

BRDY* - Bus ready (input)

This active low input indicates that the access to a memory mapped I/O area can be terminated on the next rising clock edge.

READ - Read cycle (output)

This active high output is asserted during read cycles on the memory bus.

WRITE* - Write enable (output)

This active low output provides a write strobe during write cycles on the memory bus.

PROM

ROMS*[1:0] - PROM chip-select (output)

These active low outputs provide the chip-select signal for the PROM area. ROMSN[0] is asserted when the lower half of the PROM area is accessed (0 - 0x10000000), while ROMSN[1] is asserted for the upper half.

SRAM

RAMOE*[4:0] - RAM output enable (output)

These active low signals provide an individual output enable for each RAM bank.

RAMS*[4:0] - RAM chip-select (output)

These active low outputs provide the chip-select signals for each RAM bank.

RWEN [3:0] - RAM write enable (output)

These active low outputs provide individual write strobes for each byte. RWEN[0] controls D[31:24], RWEN[1] controls D[23:16], etc.

I/O

IOS* - I/O select (output)

This active low output is the chip-select signal for the memory mapped I/O area.

SDRAM Interface

SDCLK - SDRAM clock (output)

SDRAM clock, can be configured to be identical or inverted in relation to the system clock.

SDCASN - SDRAM column address strobe (output)

This active low signal provides a common CAS for all SDRAM devices.

SDCSN[1:0] - SDRAM chip select (output)

These active low outputs provide the chip select signals for the two SDRAM banks.

SDDQM[3:0] - SDRAM data mask (output)

These active low outputs provide the DQM signals for both SDRAM banks.

SDRAS*- SDRAM row address strobe (output)

This active low signal provides a common RAS for all SDRAM devices.

SDWEN - SDRAM write strobe (output)

This active low signal provides a common write strobe for all SDRAM devices.

System Signals

CLK - Processor clock (input)

This active high input provides the main processor clock.

RESET* - Processor reset (input)

When asserted, this active low input will reset the processor and all on-chip peripherals.

WDOG* - Watchdog time-out (open-drain output)

This active low output is asserted when the watchdog expires.

BEXC* - Bus exception (input)

This active low input is sampled simultaneously with the data during accesses on the memory bus. If asserted, a memory error will be generated.

ERROR* - Processor error (open-drain output)

This active low output is asserted when the processor has entered error state and is halted. This happens when traps are disabled and a synchronous (un-maskable) trap occurs.

PIO[15:0] - Parallel I/O port (bi-directional)

These bi-directional signals can be used as inputs or outputs to control external devices.

BYPASS - PLL bypass (input)

When asserted, this active high input set the PLL in bypass mode. The device is then directly clocked by the external clock. When not asserted, the device is clocked through the PLL.

SKEW[1:0] - Clock tree skew (input)

These input signals configurate the programmable skew on the triplicated clock trees.

LOCK - PLL lock (output)

This active high output is asserted when the PLL output (internal node) is locked at the frequency corresponding to four times the input command.

PLFT - PLL passive low pass filter (input)

This input is used to connect the PLL passive low pass filter.

DSU Signals

DSUACT - DSU active (output)

This active high output is asserted when the processor is in debug mode and controlled by the DSU.

DSUBRE - DSU break enable (input)

A low-to-high transition on this active high input will generate break condition and put the processor in debug mode.

DSUEN - DSU enable (input)

The active high input enables the DSU unit. If de-asserted, the DSU trace buffer will continue to operate but the processor will not enter debug mode.

DSURX - DSU receiver (input)

This active high input provides the data to the DSU communication link receiver

DSUTX - DSU transmitter (output)

This active high input provides the output from the DSU communication link transmitter.

JTAG

TCK - Test Clock (input)

Used to clock serial data into scan latches and control sequence of the test state machine. TCK can be asynchronous with CLK.

TMS - Test Mode select (input)

Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.

TDI - Test data input (input)

Serial input data to the scan latches. Synchronous with TCK

TDO - Test data output (output)

Serial output data from the scan latches. Synchronous with TCK

TRST - Test Reset (input)

Resets the test state machine. Can be asynchronous with TCK. Shall be grounded for end application.

PCI Arbiter

AREQ*[3:0] - PCI bus request (Input)

When asserted, these active low inputs indicate that a PCI agent is requesting the bus.

AGNT*[3:0] - PCI bus grant (Output)

When asserted, these active low outputs indicate that a PCI agent is granted the PCI bus.

PCI interface

PA[31:0] - PCI Address Data (bi-directional)

Address and Data are multiplexed on the same PCI pins.

During the address phase, AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, AD[07::00] contain the least significant byte and AD[31::24] contain the most significant byte.

C/BE[3:0]* - PCI Bus Command and Byte Enables (bi-directional)

During the address phase of a transaction, C/BE[3::0]* define the bus command. During the data phase, C/BE[3::0]* are used as Byte Enables. The Byte Enables are valid for the entire data phase.

PAR - Parity (bi-directional)

The number of "1"s on AD[31::00], C/BE[3::0]*, and PAR equals an even number

FRAME* - Cycle Frame (bi-directional)

It is driven by the current master to indicate the beginning and duration of an access. FRAME* is asserted to indicate a bus transaction is beginning. While FRAME* is asserted, data transfers continue. When FRAME* is deasserted, the transaction is in the final data phase or has completed.

IRDY* - Initiator Ready (bi-directional)

IRDY* indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY* is used in conjunction with TRDY*. During a write, IRDY* indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data.

TRDY* - Target Ready (bi-directional)

TRDY* indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY* is used in conjunction with IRDY*. During a read, TRDY* indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data.

STOP* - Stop (bi-directional)

STOP* indicates the current target is requesting the master to stop the current transaction.

PCI_LOCK* - Lock (bi-directional)

LOCK* indicates an atomic operation to a bridge that may require multiple transactions to complete.

IDSEL - Initialization Device Select (input)

Initialization Device Select is used as a chip select during configuration read and write transactions.

DEVSEL* - Device Select (bi-directional)

When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL* indicates whether any device on the bus has been selected.

REQ* - PCI bus request (output)

REQ* indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ* which must be tri-stated while RST* is asserted.

GNT* - PCI Bus Grant (input)

GNT* indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNT* which must be ignored while RST* is asserted.

PCI_CLK - PCI clock (input)

PCI_CLOCK provides timing for all transactions on PCI. All other PCI signals, except RST*, are sampled on the rising edge of PCI_CLK and all other timing parameters are defined with respect to this edge.

RST* - PCI Reset (input)

Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state.

PERR* - Parity Error (bi-directional)

Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR* pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR* is one clock for each data phase that a data parity error is detected.

SERR* - System Error (bi-directional)

System Error is for reporting address parity errors, data parity errors on the special cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

SYSEN* - PCI Host (input)

This active low input specifies the configuration of the device. At boot-up time, if SYSEN* is sampled at a low level, the device is configured as the host of the PCI bus. If SYSEN* is sampled at a high level, the device is configured as a satellite.

Product Description

Integer Unit

The AT697E integer unit (IU) implements SPARC integer instructions as defined in *SPARC Architecture Manual Version 8.* The IU is designed for highly dependable space and military applications, and includes support for error detection. The RISC architecture makes possible the creation of a processor that can execute instructions at a rate approaching one instruction per processor clock.

Floating Point Unit (FPU)

The FPU is designed to provide execution of single and double-precision floating point instructions. The processor is stopped during the execution of floating point instructions.

Instruction Set

AT697E instruction set describes six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point, and miscellaneous. Please refer to SPARC V8 architecture manual that presents implemented instructions.

Cache Sub-System

Separate instruction and data caches are provided. The instruction cache uses streaming during line-refill to minimize refill latency. The data cache uses writethrough policy and implements a double-word write-buffer. The data cache also performs bus-snooping on the AHB bus.

Memory Interface

The AT697E is designed to allow easy interfacing to internal/external memory resources. The flexible memory interface provides a direct interface for PROM, memory mapped I/O devices, static RAM (SRAM) and synchronous dynamic RAM (SDRAM). The memory areas can be programmed to either 8-, 16- or 32-bit data width.

Address Range	Size	Mapping
0x00000000 - 0x1FFFFFFF	512 MB	PROM
0x20000000 - 0x3FFFFFFF	512 MB	I/O
0x40000000 - 0x7FFFFFFF	1 GB	SRAM/SDRAM

Fault Tolerance

The AT697E processor has been especially designed for space application. To prevent erroneous operations from Single Event Transient (SET) and Single Event Upset (SEU) errors, the AT697E processor implements a set of protection features including:

- Full triple modular redundancy (TMR)
- EDAC protection on Register file
- EDAC protection on external memory interface
- Parity protection on instruction and data caches

TRAPs

The AT697E supports two types of traps:

- Synchronous traps
- Asynchronous traps also called interrupts

Synchronous traps are caused by hardware responding to a particular instruction: they occur during the instruction that caused them. Asynchronous traps occur when an external event interrupts the processor. They are not related to any particular instruction and occur between the execution of instructions.

Timers

General Purpose Timers

Two 24-bit timers are provided on-chip. The timers can work in periodic or one-shot mode. Both timers are clocked by a common 10-bit prescaler.

Watchdog Timer

A 24-bit watchdog is provided on-chip. The watchdog is clocked by the timer prescaler. When the watchdog reaches zero, an output signal (WDOG) is asserted. This signal can be used to generate system reset.

Communication Interfaces

Serial Interfaces – UARTs

Two full duplex asynchronous receiver transmitters (UART) are included. The data format of the UART's is eight data bits with one stop bit. It is possible to choose between no parity, even and odd parity. UART's provide double buffering, i.e. each UART consists of a transmitter holding register, a receiver holding register, a transmitter shift register, and a receiver shift register. Each of these registers are 8-bit wide. For each UART a data register is provided. The baud rate of both the UART's is individually programmable.

Parallel Interface

A 32-bit parallel I/O port is provided. 16 bits are always available and can be individually programmed by software to be an input or an output. The additional 16 bits are only available when the memory bus is configured for 8- or 16-bit operation.

Some of the bits have alternate usage, such as UART inputs/outputs and external interrupts inputs.

PCI interface

The PCI implementation standing on the AT697E is PCI 2.2 compliant. It is a high performance 32-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between processor/memory systems and peripheral controller components.

Test and Diagnostics

The design is highly testable with the support of a Debug System Unit (DSU), an internal and boundary scan through JTAG interface.

Test Access Port (TAP)

A TAP is provided through a JTAG interface.

DSU

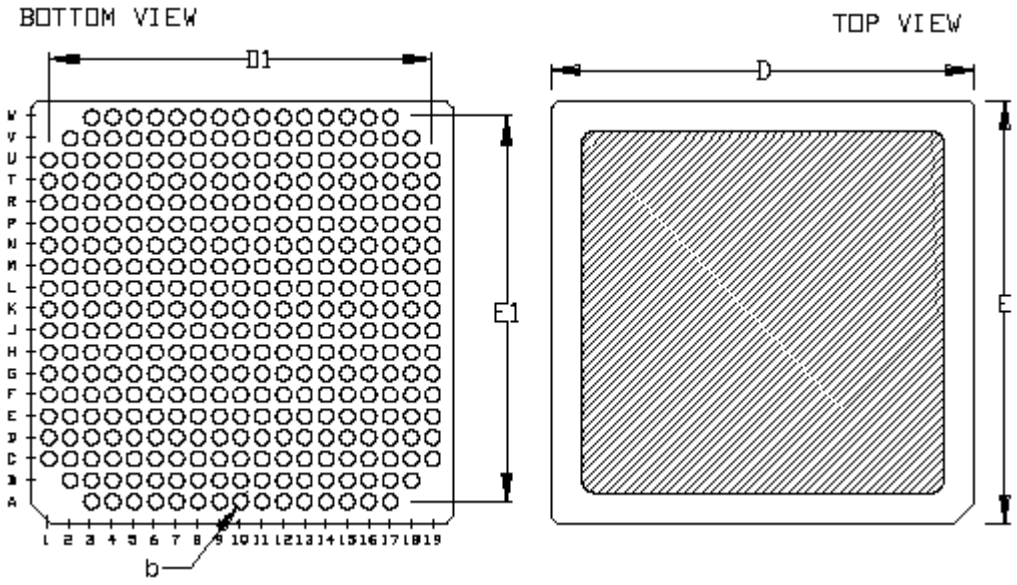
The on-chip debug support unit (DSU) allows non-intrusive debugging on target hardware. The DSU allows to insert instruction and data watchpoints, and access to all on-chip registers from a remote debugger. A trace buffer is provided to trace the executed instruction flow and/or AHB bus traffic. Communication to an outside debugger (e.g. gdb) is done using a dedicated UART (RS232).

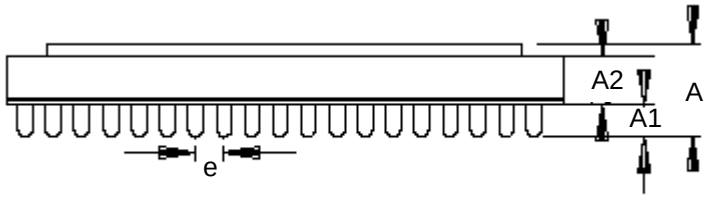
Watchpoint Registers

To aid software debugging, up to four watchpoint registers are provided. Each register can cause a debug-trap on an arbitrary instruction or data address range. If the debug support unit is enabled, the watchpoints can be used to enter debug mode.

Package - MCGA 349

Mechanical Outlines





	mm		inch	
	min	max	min	max
D/E	24,8	25,2	0,976	0,992
D1/E1	22,86		0,9	
A1	1,4	1,85	0,055	0,073
A2	2,4	3,45	0,094	0,136
A	4,3	5,9	0,169	0,232
b	0,79	0,99	0,031	0,04
e	1,27		0,05	

Socket / Adapter

In order to support MCGA 349 package on evaluation board that may require exchange of the chip, ATMEL had a dedicated socket developped by Adapters-Plus.

Socket reference

The reference of the socket for the MCGA349 package is **CL349SA1912F**.

A direct link to information on this socket is available at: **http://www.adapt-plus.com/products/ic_sockets/datasheets/ds_MCGA_lockingskt.htm**

Provider

The **CL349SA1912F** socket is provided by Adapters-Plus :

Adapters-Plus

15 W 8TH STREET STE B.

Tracy, Ca 95376 - USA

Phone: 209-839-0200

Fax: 209-839-0235

www.adapt-plus.com

Ordering Information

Table 1. Possible Order Entries

Part-Number	Supply Voltage (core / IOs)	Temperature Range	Maximum Speed (MHz)	Packaging	Quality Flow
AT697E-2E-E	1.8V / 3.3V	25°C	100	MCGA349	Engineering Samples

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
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