RF9909

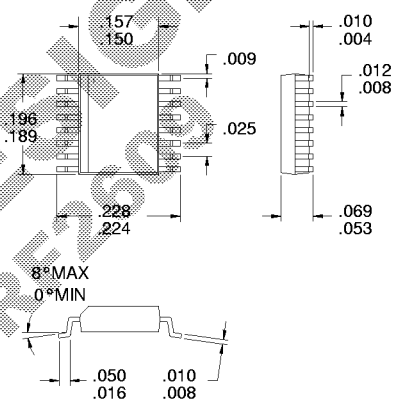
CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Portable Battery Powered Equipment

Product Description

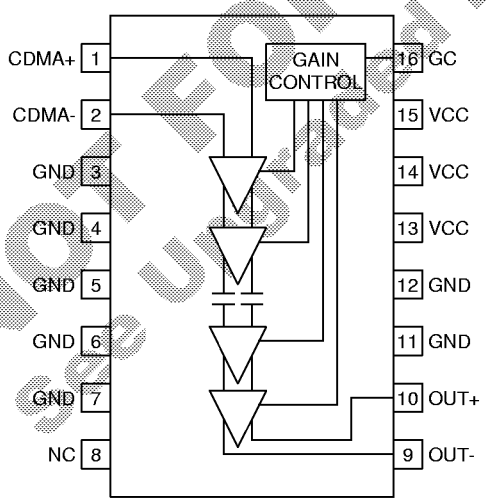
The RF9909 is a complete AGC amplifier designed for the transmit section of dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing 84dB of gain control range. Noise Figure, IP_3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and is packaged in a standard miniature 16-lead plastic SSOP package.



Package Style: SSOP-16

Optimum Technology Matching® Applied

☐ Si BJT ☑ GaAs HBT ☐ GaAs MESFET
☐ Si Bi-CMOS



Functional Block Diagram

Features

- Supports Dual Mode Operation
- -45dB to +39dB Gain Control Range
- Single 3.6V Power Supply
- Monolithic Construction
- DC to 200MHz Operation
- Miniature Surface Mount Package

Ordering Information

RF9909	CDMA/FM Transmit AGC Amplifier
RF9909 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

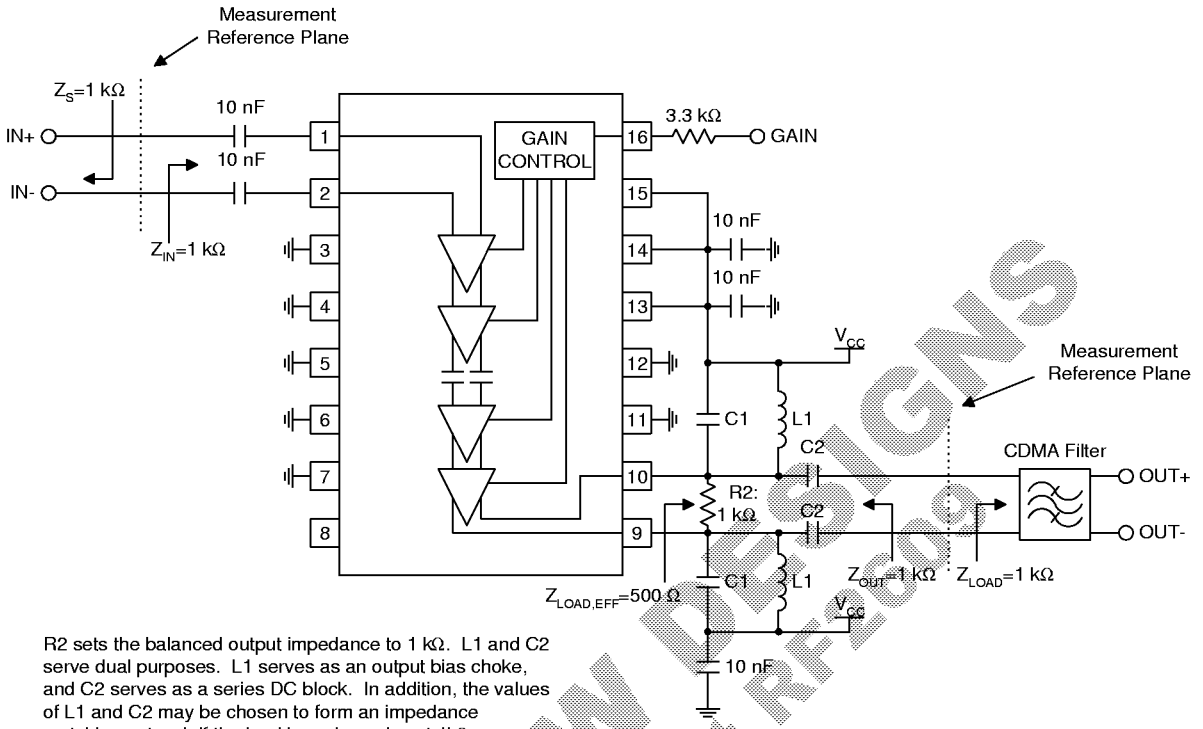
Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 ° C, 130MHz, V_{CC}=3.6 V, Z_S=1 kΩ, Z_L=1 kΩ, 1kΩ External Output Terminating Resistor (Effective Z_L=500Ω) (See Application Example)
Frequency Range		DC to 200		MHz	
Maximum Gain	+39	+42		dB	V_C=2.76V
Minimum Gain		-52	-45	dB	V_C=0.2 V
Gain Slope	30	47	60	dB/V	Measured in 0.5 V increments
Gain Control Voltage Range		0 to 3		V_{DC}	
Gain Control Input Impedance		30		kΩ	
Input IP3	-29	-26		dBm	At +10 gain and referenced to 1 kΩ
Input Impedance		1		kΩ	Differential
Stability (Max VSWR)	10:1				Spurious<-70 dBm
Power Supply					
Voltage		3.6±5%		V	
Current Consumption		23		mA	Maximum gain
Current Consumption		22	28	mA	Minimum gain

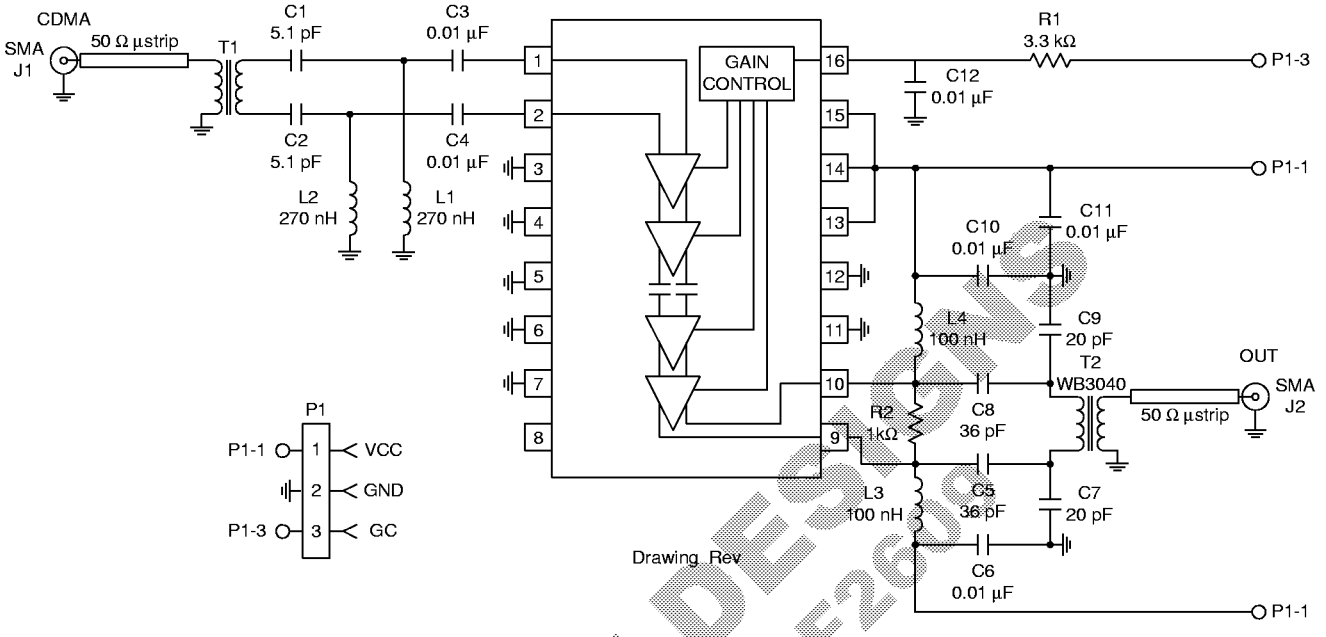
Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level, other than V_{CC}, present. A DC to connection to V_{CC} is acceptable. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 1kΩ, while the single-ended input impedance is 500Ω.	
2	CDMA-	Same as pin 1, except complementary input.	
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	GND	Same as pin 3.	
7	GND	Same as pin 3.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC}.	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	
10	OUT+	Same as pin 9, except complementary output.	
11	GND	Same as pin 3.	
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 13, 14, and 15 may share one bypass capacitor if trace lengths are kept minimal.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are only valid for a 3.3kΩ DC source impedance.	

Application Schematic



R2 sets the balanced output impedance to 1 kΩ. L1 and C2 serve dual purposes. L1 serves as an output bias choke, and C2 serves as a series DC block. In addition, the values of L1 and C2 may be chosen to form an impedance matching network if the load impedance is not 1kΩ. Otherwise, the values of L1 and C1 are chosen to form a parallel-resonant tank circuit at the IF when the IF filter's input impedance is 1 kΩ.

Evaluation Board Schematic



Bill of Materials
RF9909PCBA

Used on: **9909410B.PCB**

Item No.	Qty	Vendor	Vendor Part #	Type	Value	Ref Designator
RF9909	1	RFMD	RF9909	CDMA/FM AGC Amplifier	RF9909	DUT1
40012	1	Digi-Key	P1.00KFTR-ND	Resister, 1206	1K	R2
40018	1	Digi-Key	P3.3KETR-ND	Resistor, 1206	3.3K	R1
42010	2	ATC	100A360JP150X	Capacitor, ATC	36pF	C5, C8
42020	2	ATC	100A5R1CP150X	Capacitor, ATC	5.1Pf	C1, C2
42034	6	Digi-Key	PCC103BTR-ND	Capacitor, 0805	0.01uF	C3, C4, C6, C10, C11, C12
42059	2	ATC	100A200JP150X	Capacitor, ATC	20pF	C7, C9
44001	2	Coilcraft	0805CS-101XKBC	Inductor, 0805	100nH	L3, L4
44020	2	Coilcraft	1008CS-271XKBC	Inductor, 1206	270nH	L1, L2
46001	1	Digi-Key	MPSS100-3C	Connector, Panduit	Connector	P1
46003	2	EFJohnson	142-0701-881	SMA End Connector	SMA	J1, J2
49003	2	Coilcraft	WB3040-SM	Transform	WB3040	T1, T2