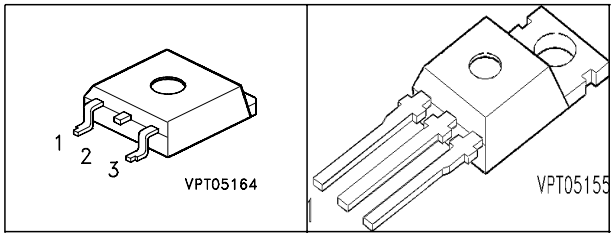
OptiMOS™ Power-Transistor

Features

- N-Channel
- Enhancement mode
- Avalanche rated
- Logic Level
- d*v*/d*t* rated
- 175°C operating temperature

Product Summary

Drain source voltage	V_{DS}	75	V
Drain-source on-state resistance	$R_{DS(on)}$	7.1	mΩ
Continuous drain current	I_D	80	A



Type	Package	Ordering Code
SPP80N08S2L-07	P-TO220-3-1	-
SPB80N08S2L-07	P-TO263-3-2	-

Pin 1	PIN 2/4	PIN 3
G	D	S

Maximum Ratings,at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C, 1) T_C = 100 °C	I_D	 80 80	A
Pulsed drain current T_C = 25 °C	$I_{D\ puls}$	320	
Avalanche energy, single pulse I_D = 80 A , V_{DD} = 25 V, R_{GS} = 25 Ω	E_{AS}	810	mJ
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	35.7	
Reverse diode d*v*/d*t* I_S = 80 A, V_{DS} = 60 V, d*i*/d*t* = 200 A/µs, T_{jmax} = 175 °C	d*v*/d*t*	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C = 25 °C	P_{tot}	357	W
Operating and storage temperature	T_j , T_{stg}	-55...+175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

[1]Current limited by bondwire; with an R_{thJC} = 0.5 K/W the chip is able to carry I_D = 132A

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm^2 cooling area [1)]		-	-	40	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage V_{GS} = 0 V, I_D = 1 mA	$V_{(BR)DSS}$	75	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 250 µA	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}				µA
V_{DS} = 75 V, V_{GS} = 0 V, T_j = 25 °C		-	0.01	1	
V_{DS} = 75 V, V_{GS} = 0 V, T_j = 125 °C		-	1	100	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	1	100	nA
Drain-source on-state resistance V_{GS} = 4.5 V, I_D = 40 A	$R_{DS(on)}$	-	tbd	9	mΩ
Drain-source on-state resistance V_{GS} = 10 V, I_D = 40 A	$R_{DS(on)}$	-	tbd	7.1	

[1]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Transconductance $V_{DS} \geq 2 * I_D * R_{DS(on)max}$, I_D = 80 A	g_{fs}	tbd	tbd	-	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	tbd	tbd	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	tbd	tbd	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	tbd	tbd	
Turn-on delay time V_{DD} = 40 V, V_{GS} = 4.5 V, I_D = 80 A, R_G = 1.1 Ω	$t_{d(on)}$	-	tbd	tbd	ns
Rise time V_{DD} = 40 V, V_{GS} = 4.5 V, I_D = 80 A, R_G = 1.1 Ω	t_r	-	tbd	tbd	
Turn-off delay time V_{DD} = 40 V, V_{GS} = 4.5 V, I_D = 80 A, R_G = 1.1 Ω	$t_{d(off)}$	-	tbd	tbd	
Fall time V_{DD} = 40 V, V_{GS} = 4.5 V, I_D = 80 A, R_G = 1.1 Ω	t_f	-	tbd	tbd	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Gate Charge Characteristics					
Gate to source charge V_{DD} = 60 V, I_D = 80 A	Q_{gs}	-	tbd	tbd	nC
Gate to drain charge V_{DD} = 60 V, I_D = 80 A	Q_{gd}	-	tbd	tbd	
Gate charge total V_{DD} = 60 V, I_D = 80 A, V_{GS} = 0 to 10 V	Q_g	-	tbd	tbd	
Gate plateau voltage V_{DD} = 60 V, I_D = 80 A	$V_{(plateau)}$	-	tbd	-	V

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse Diode					
Inverse diode continuous forward current T_C = 25 °C	I_S	-	-	80	A
Inverse diode direct current, pulsed T_C = 25 °C	I_{SM}	-	-	320	
Inverse diode forward voltage V_{GS} = 0 V, I_F = 80 A	V_{SD}	-	0.9	1.3	V
Reverse recovery time V_R = 40 V, I_F=I_S, di_F/dt = 100 A/µs	t_{rr}	-	tbd	tbd	ns
Reverse recovery charge V_R = 40 V, I_F=I_S, di_F/dt = 100 A/µs	Q_{rr}	-	tbd	tbd	nC
Soft factor t_f / t_s	S	-	tbd	-	

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