



Rev. 1.6

UTRON

UT62L25616
256K X 16 BIT LOW POWER CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	Draft Date
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev. 1.0	1. The symbols CE#,OE#,WE# are revised as $\overline{CE}$, $\overline{OE}$, $\overline{WE}$. 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range. 4. The power supply is revised: 3.3V $\Rightarrow$ 3.6V	Jul 4,2001
Rev. 1.1	1. Revised PIN CONFIGURATION Rev 1.0 : No A17 pin $\rightarrow$ typing error Rev 1.1 : add A17 pin. a、 TFBGA package : ball D3 : NC $\rightarrow$ A17 b、 TSOP- package : pin18 : A16 $\rightarrow$ A17 pin19 : A15 $\rightarrow$ A16 pin20 : A14 $\rightarrow$ A15 pin21 : A13 $\rightarrow$ A14 pin22 : A12 $\rightarrow$ A13 pin23 : NC $\rightarrow$ A12	Oct 18,2001
Rev. 1.2	1. Revised AC ELECTRICAL CHARACTERISTICS t_{OH} : 5ns $\rightarrow$ 10ns (Min.) t_{BLZ} : 0ns $\rightarrow$ 10ns (Min.) 2. Revised FUNCTIONAL BLOCK DIAGRAM	Mar 19,2002
Rev. 1.3	1. Revised DC ELECTRICAL CHARACTERISTICS : Revised V_{IH} as 2.2V 2. Revised 48-pin TFBGA package outline dimension : a、 Rev. 1.2 : ball diameter=0.3mm b、 Rev. 1.3 : ball diameter=0.35mm	Apr 17,2002
Rev. 1.4	1. Add under/overshoot range of V_{IL} & V_{IH}	Nov 13,2002
Rev. 1.5	1. Revised Standby current (LL-Version) : 3uA(typ) $\rightarrow$ 2uA(typ) 2. Revised operating current (Iccmax) : 45/35/25mA $\rightarrow$ 40/30/25mA 3. Revised DC CHARACTERISTICS : a. Operating Power Supply Current (Icc) 55ns (max) : 45 $\rightarrow$ 40mA 70ns (typ) : 25 $\rightarrow$ 20mA, 70ns (max) : 35 $\rightarrow$ 30mA 100ns (Typ) : 20 $\rightarrow$ 16mA b. Standby current(CMOS) : LL-version (typ) : 3 $\rightarrow$ 2uA, 25 $\rightarrow$ 20uA	Dec 03,2002
Rev. 1.6	1. Revised V_{OH} (Typ) : NA $\rightarrow$ 2.7V 2. Add $V_{IH}(\max)=V_{CC}+2.0V$ for pulse width less than 10ns. $V_{IL}(\min)=V_{SS}-2.0V$ for pulse width less than 10ns. 3. Add order information for lead free product	May 06,2003



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FEATURES

- Fast access time : 55/70/100ns
- CMOS Low power operating
Operating current : 40/30/25mA (I_{cc} max.)
Standby current : 20uA (typ.) L-version
2uA (typ.) LL-version
- Single 2.7V~3.6V power supply
- Operating temperature:
Commercial : 0 ~70
Extended : -20 ~80
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Data byte control : $\overline{\text{LB}}$ (I/O1~I/O8)
 $\overline{\text{UB}}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP
48-pin 6mm × 8mm TFBGA

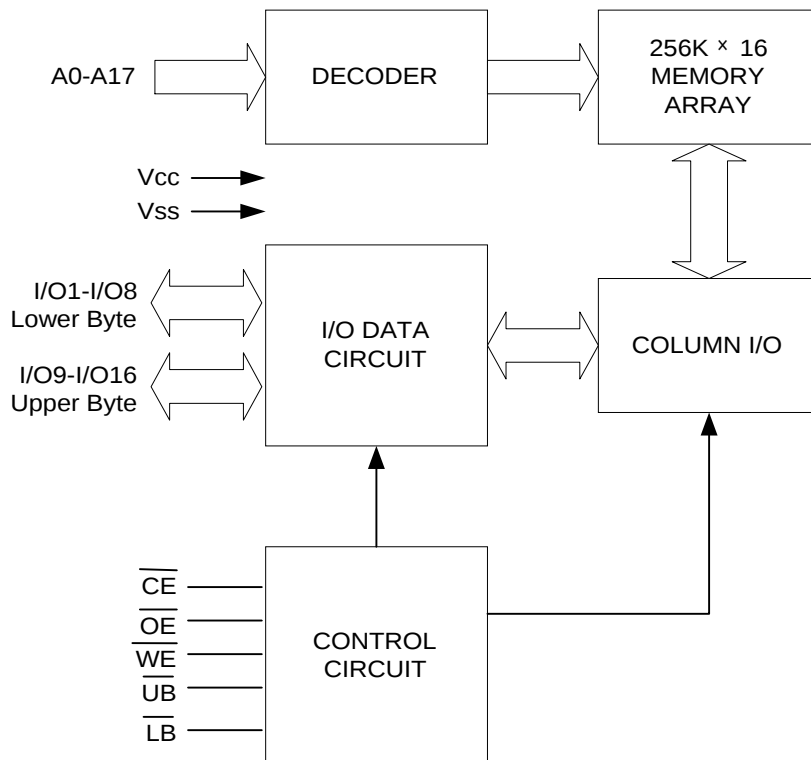
GENERAL DESCRIPTION

The UT62L25616 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

The UT62L25616 operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L25616 is designed for low power system applications. It is particularly suited for use in high-density high-speed system applications.

FUNCTIONAL BLOCK DIAGRAM





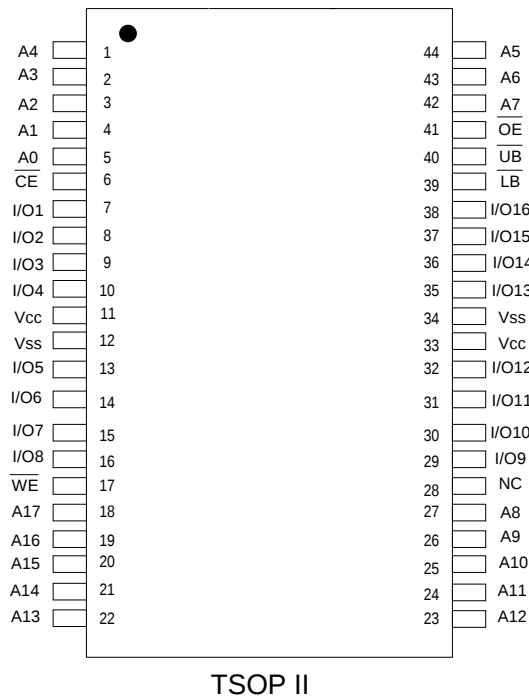
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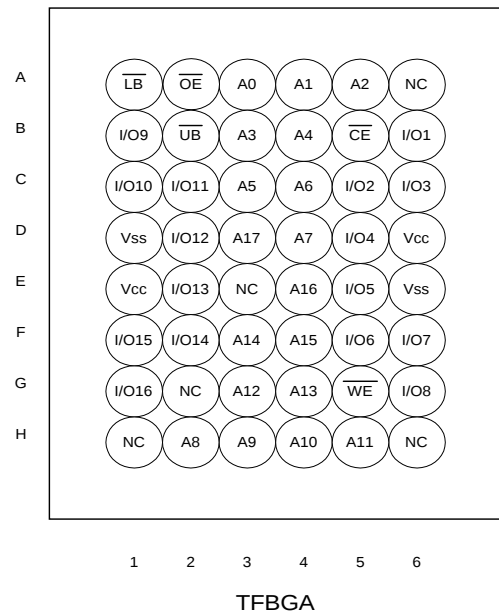
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PIN CONFIGURATION



TSOP II



TFBGA

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Control
$\overline{UB}$	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High - Z	High - Z	I_{SB}, I_{SB1}
	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	L	X	High - Z	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	H	H	X	L	High - Z	High - Z	
Read	L	L	H	L	H	D_{OUT}	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	L	H	H	L	High - Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High - Z	I_{CC}, I_{CC1}, I_{CC2}
	L	X	L	H	L	High - Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH} , L = V_{IL} , X = Don't care.



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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70
	Extended	T_A	-20 to 80
Storage Temperature	T_{STG}	-65 to 150	
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = 0$ to 70 / -20 to 80 (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}		2.7	3.0	3.6	V
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}^{*2}		-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \quad V_{IN} \quad V_{CC}$	-1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \quad V_{IO} \quad V_{CC}$; Output Disable	-1	-	1	μA
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	2.7	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty $I/O=0mA$, $\overline{CE}=V_{IL}$	55	-	30	mA
			70	-	20	mA
			100	-	16	mA
Average Operation Current	I_{CC1}	100%duty, $I_{IO}=0mA$, $\overline{CE} = 0.2V$, other pins at 0.2V or $V_{CC}-0.2V$	$T_{cycle}=1\mu s$	-	4	mA
	I_{CC2}		$T_{cycle}=500ns$	-	8	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}=V_{IH}$, other pins $=V_{IL}$ or V_{IH}	-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}=V_{CC}-0.2V$ other pins at 0.2V or $V_{CC}-0.2V$	-L	-	20	μA
			-LL	-	2	μA

Notes:

1. Overshoot : $V_{CC}+2.0V$ for pulse width less than 10ns.
2. Undershoot : $V_{SS}-2.0V$ for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.



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CAPACITANCE ($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF}$, $I_{OH}/I_{OL} = -1\text{mA} / 2.1\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=2.7\text{V}\sim 3.6\text{V}$, $T_A=0^\circ\text{C}$ to 70°C / -20°C to 80°C (E))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L25616-55		UT62L25616-70		UT62L25616-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	55	-	70	-	100	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{BHZ}	-	25	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{BLZ}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

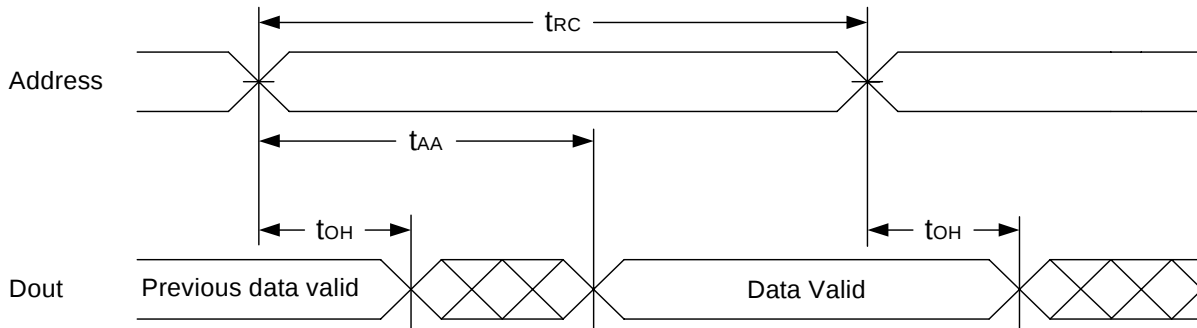
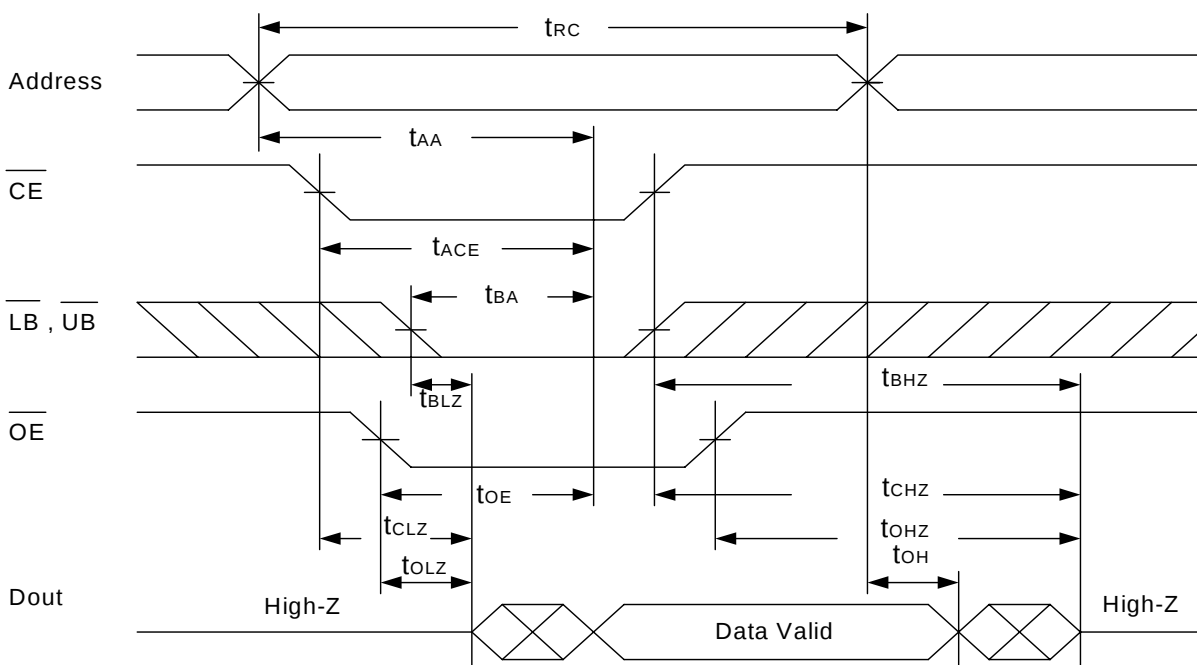
PARAMETER	SYMBOL	UT62L25616-55		UT62L25616-70		UT62L25616-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	45	-	60	-	80	-	ns

*These parameters are guaranteed by device characterization, but not production tested.



TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)

Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ = low, $\overline{CE}$ = low, $\overline{LB}$ or $\overline{UB}$ = low.
3. Address must be valid prior to or coincident with $\overline{CE}$ = low, $\overline{LB}$ or $\overline{UB}$ = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

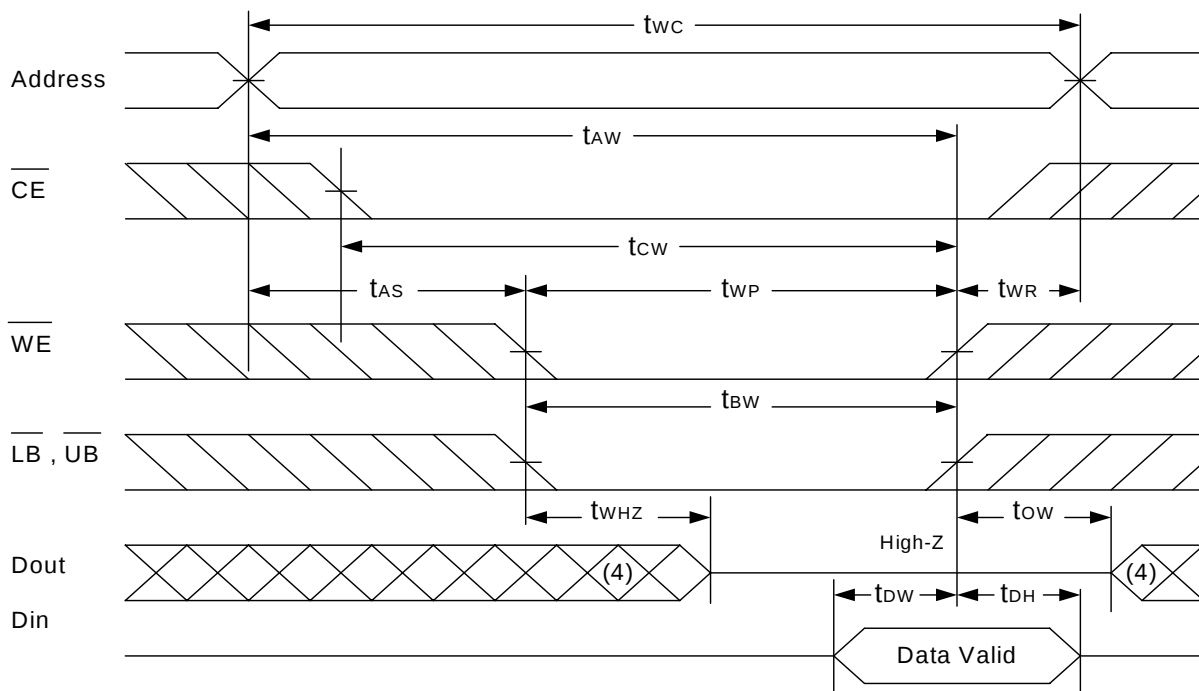


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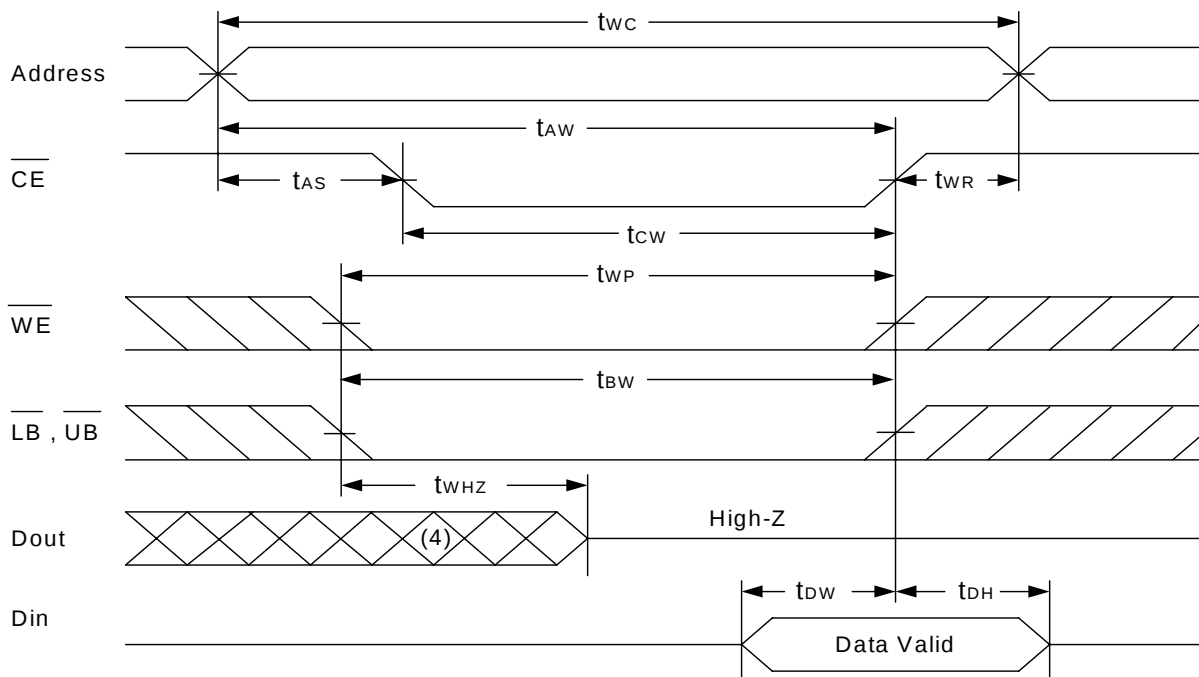
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WRITE CYCLE 1 ($\overline{\text{WE}}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{\text{CE}}$ Controlled) (1,2,5,6)



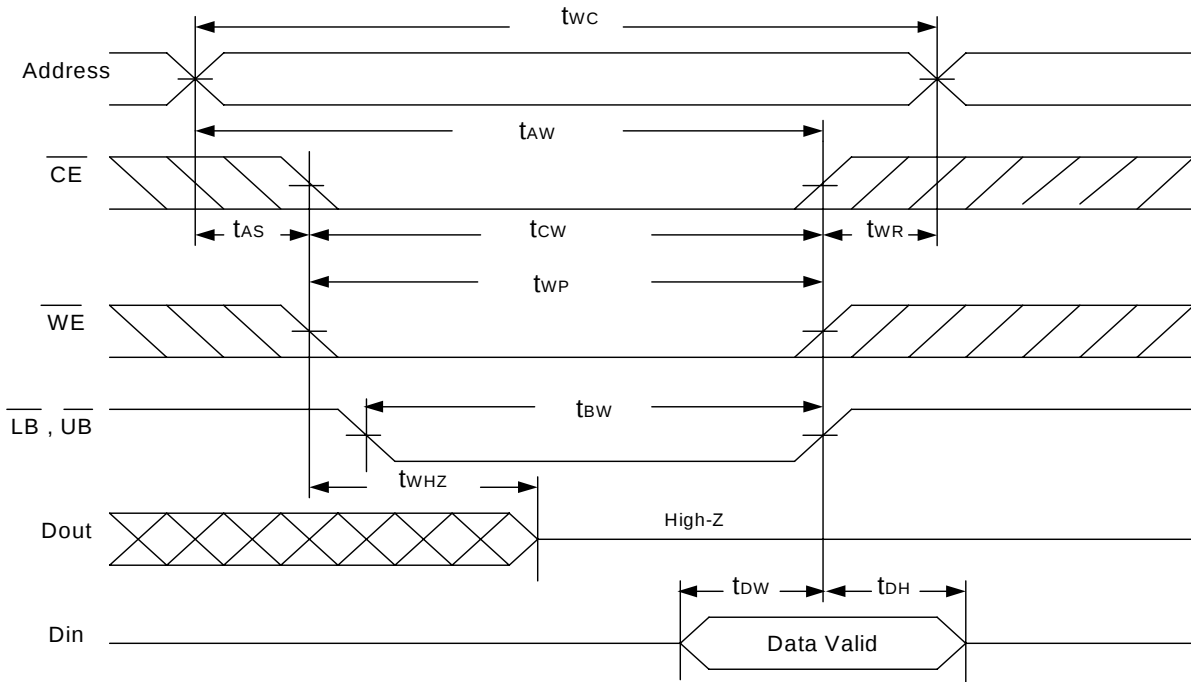


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WRITE CYCLE 3 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled) (1,2,5,6)



Notes :

1. $\overline{\text{WE}}$, $\overline{\text{CE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{\text{CE}}$, low $\overline{\text{WE}}$, $\overline{\text{LB}}$ or $\overline{\text{UB}}$ = low.
3. During a $\overline{\text{WE}}$ controlled write cycle with $\overline{\text{OE}}$ low, t_{WP} must be greater than $t_{\text{WHZ}} + t_{\text{DW}}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{\text{CE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ low transition occurs simultaneously with or after $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

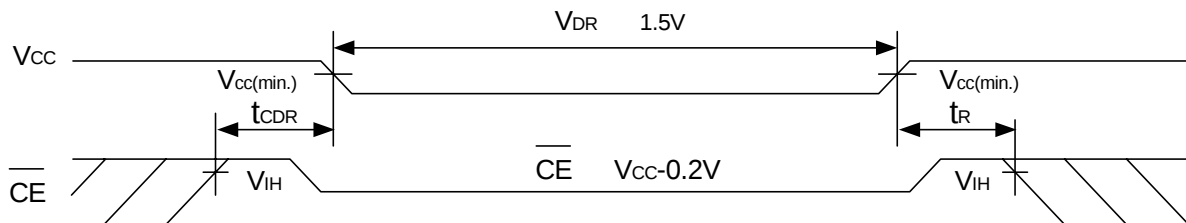
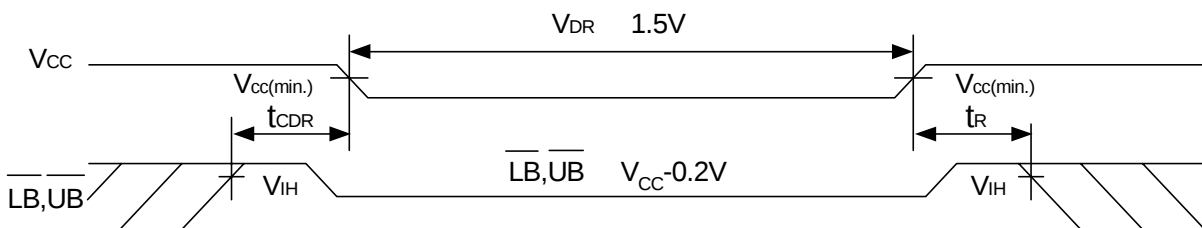


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256K X 16 BIT LOW POWER CMOS SRAM**DATA RETENTION CHARACTERISTICS** ($T_A = 0$ to 70 / -20 to 80 (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	$\overline{CE}$ V _{CC} -0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =1.5V $\overline{CE}$ V _{CC} -0.2V	- L	1	50	μ A
			- LL	0.5	20	μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t _R		5	-	-	ms

DATA RETENTION WAVEFORM**Low V_{CC} Data Retention Waveform (1)** ($\overline{CE}$ controlled)**Low V_{CC} Data Retention Waveform (2)** ($\overline{LB}$, $\overline{UB}$ controlled)



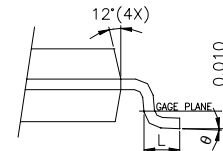
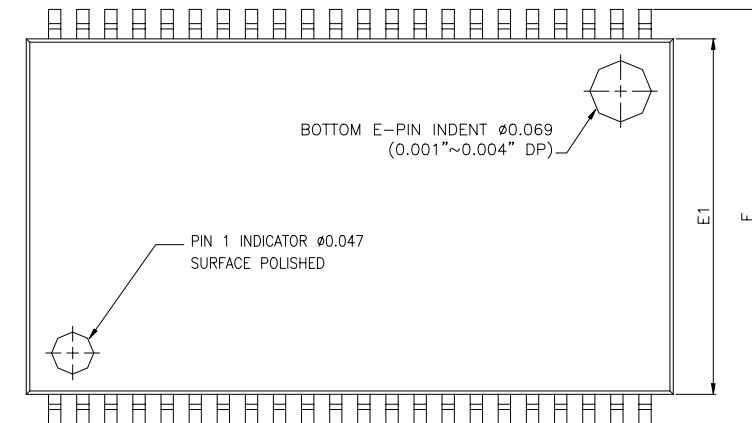
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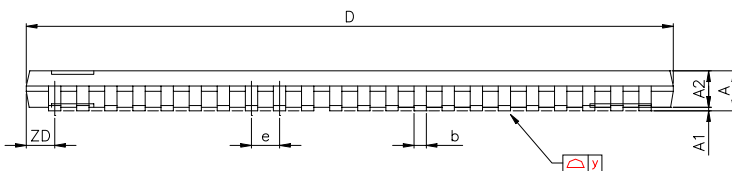
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PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP- Package Outline Dimension



DETAIL B



DETAIL B

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0°	-	5°	0°	-	5°

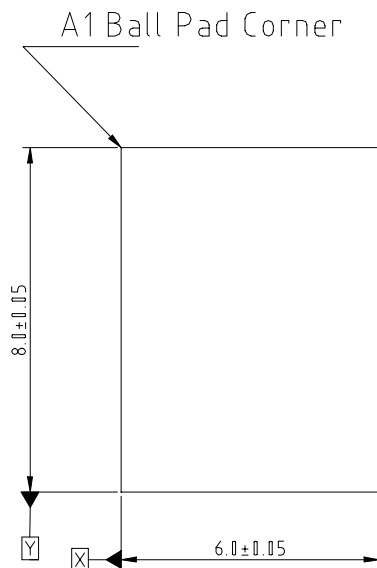


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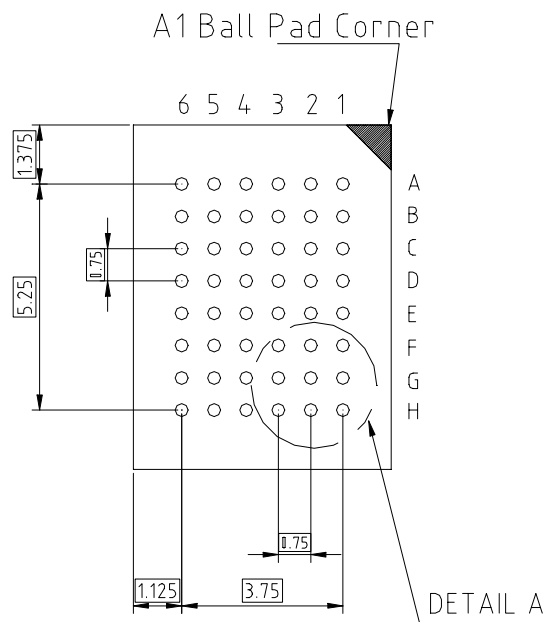
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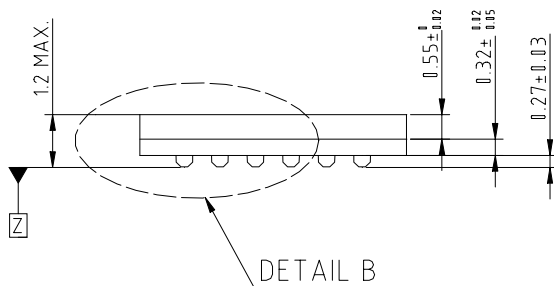
48-pin 6mm × 8mm TFBGA Package Outline Dimension



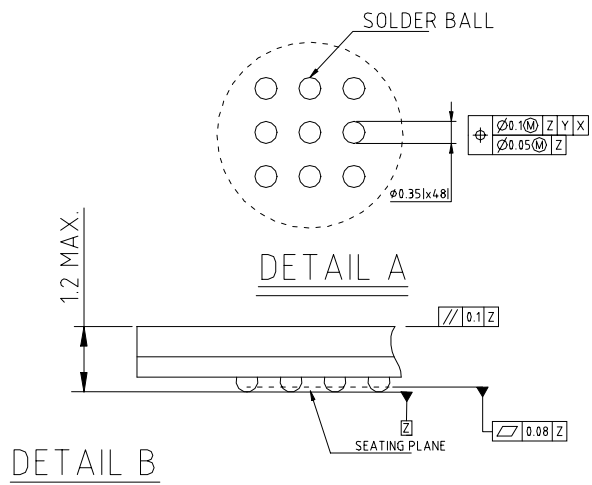
TOP VIEW (DIE VIEW)



BOTTOM VIEW (BALL SIDE)



SIDE VIEW



DETAIL B



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UTRON**UT62L25616****256K X 16 BIT LOW POWER CMOS SRAM****ORDERING INFORMATION****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L25616MC-55L	55	20	44 PIN TSOP-
UT62L25616MC-55LL	55	2	44 PIN TSOP-
UT62L25616MC-70L	70	20	44 PIN TSOP-
UT62L25616MC-70LL	70	2	44 PIN TSOP-
UT62L25616MC-100L	100	20	44 PIN TSOP-
UT62L25616MC-100LL	100	2	44 PIN TSOP-
UT62L25616BS-55L	55	20	48 PIN TFBGA
UT62L25616BS-55LL	55	2	48 PIN TFBGA
UT62L25616BS-70L	70	20	48 PIN TFBGA
UT62L25616BS-70LL	70	2	48 PIN TFBGA
UT62L25616BS-100L	100	20	48 PIN TFBGA
UT62L25616BS-100LL	100	2	48 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L25616MC-55LE	55	20	44 PIN TSOP-
UT62L25616MC-55LLE	55	2	44 PIN TSOP-
UT62L25616MC-70LE	70	20	44 PIN TSOP-
UT62L25616MC-70LLE	70	2	44 PIN TSOP-
UT62L25616MC-100LE	100	20	44 PIN TSOP-
UT62L25616MC-100LLE	100	2	44 PIN TSOP-
UT62L25616BS-55LE	55	20	48 PIN TFBGA
UT62L25616BS-55LLE	55	2	48 PIN TFBGA
UT62L25616BS-70LE	70	20	48 PIN TFBGA
UT62L25616BS-70LLE	70	2	48 PIN TFBGA
UT62L25616BS-100LE	100	20	48 PIN TFBGA
UT62L25616BS-100LLE	100	2	48 PIN TFBGA



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UTRON**UT62L25616****256K X 16 BIT LOW POWER CMOS SRAM****ORDERING INFORMATION (for lead free product)****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) typ.	PACKAGE
UT62L25616MCL-55L	55	20	44 PIN TSOP-
UT62L25616MCL-55LL	55	2	44 PIN TSOP-
UT62L25616MCL-70L	70	20	44 PIN TSOP-
UT62L25616MCL-70LL	70	2	44 PIN TSOP-
UT62L25616MCL-100L	100	20	44 PIN TSOP-
UT62L25616MCL-100LL	100	2	44 PIN TSOP-
UT62L25616BSL-55L	55	20	48 PIN TFBGA
UT62L25616BSL-55LL	55	2	48 PIN TFBGA
UT62L25616BSL-70L	70	20	48 PIN TFBGA
UT62L25616BSL-70LL	70	2	48 PIN TFBGA
UT62L25616BSL-100L	100	20	48 PIN TFBGA
UT62L25616BSL-100LL	100	2	48 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) typ.	PACKAGE
UT62L25616MCL-55LE	55	20	44 PIN TSOP-
UT62L25616MCL-55LLE	55	2	44 PIN TSOP-
UT62L25616MCL-70LE	70	20	44 PIN TSOP-
UT62L25616MCL-70LLE	70	2	44 PIN TSOP-
UT62L25616MCL-100LE	100	20	44 PIN TSOP-
UT62L25616MCL-100LLE	100	2	44 PIN TSOP-
UT62L25616BSL-55LE	55	20	48 PIN TFBGA
UT62L25616BSL-55LLE	55	2	48 PIN TFBGA
UT62L25616BSL-70LE	70	20	48 PIN TFBGA
UT62L25616BSL-70LLE	70	2	48 PIN TFBGA
UT62L25616BSL-100LE	100	20	48 PIN TFBGA
UT62L25616BSL-100LLE	100	2	48 PIN TFBGA



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