GBL GigaBit Logic

10G001

Quad 2 Input NOR Gate

290 PS Gate Delay

10G PicoLogic™ Family

DISTINCTIVE CAPABILITIES

- 290 ps max propagation delay
- Output rise and fall times of 150 ps
- 0°C to +85°C operating temperature range
- 10G PicoLogic compatible inputs and outputs
- VBB reference voltage for improved threshold tracking over temperature and power supply variation
- On-chip VBBS (-1.3V) reference voltage
- Supports a wide range of load resistor and termination voltage combinations
- Wire-OR output capability
- Available in flatpack, leadless chip carrier (LCC) or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

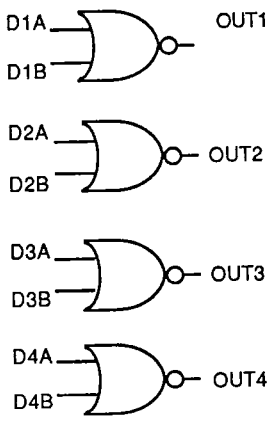
- Logic functions
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed TTL/CMOS to10G/ECL and 10G to TTL/CMOS translation ability

FUNCTIONAL DESCRIPTION

The10G001 is an ultra fast quad 2 input NOR gate featuring a maximum propagation delay of 290 ps for packaged parts. It offers a typical speed four times faster than equivalent ECL NOR gates. The10G001 is ideally suited for use in high performance systems requiring improved throughput, reduced signal skew and increased timing margin. It can also drive and be driven from CMOS and TTL gates, providing the user a high speed TTL/CMOS to10G/ECL translation capability.

For compatibility with other high speed logic familles, the 10G001 features the PicoLogic™ family standard VBB input. This input allows the 10G001's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise inmunity. An on-chip threshold voltage ouput (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G001. The 10G001 has input clamps VICH and VICL. When connected to -1.3V, these internally truncate an overdriven sine wave input signal to a square wave, thus allowing inputs to be driven with faster rise and fall times. When not used, the input clamps should be connected to VICL = VSS and VICH = VDDO for transient protection.

BLOCK DIAGRAM



10G001 ORDERING INFORMATION

PACKAGE TYPE	DELAY (Max @ 25°C)	
	320 ps	390 ps
40 I/O C-Leaded CC	10G001-C	10G001-4C
40 I/O Leadless CC	10G001-L	10G001-4L
	290 ps	360 ps
36 I/O Leadless CC*	10G001-L36	10G001-4L36
36 I/O Flatpack*	10G001-F	10G001-4F
Dice		10G001-4X

* Not recomended for new designs