



CYPRESS

CY7C381
CY7C382

Very High Speed 1K (3K) Gate CMOS FPGA

Features

- **Very high speed**
 - Loadable counter frequencies greater than 100 MHz
 - Chip-to-chip operating frequencies up to 85 MHz
 - Input + logic cell + output delays under 9 ns
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
 - 8 x 12 array of 96 logic cells provides 3,000 total available gates
 - 1,000 typically usable "gate array" gates in 44- and 68-pin PLCC/CPGA packages
- **Low power, high output drive**
 - Standby current typically 2 mA
 - 16-bit counter operating at 100 MHz consumes 50 mA
 - Minimum I_{OL} and I_{OH} of 8 mA
- **Flexible logic cell architecture**
 - Wide fan-in (up to 14 input gates)
 - Multiple outputs in each cell
 - Very low cell propagation delay (3.4 ns)
- **Low-cost, powerful design tools**
 - Designs entered in VHDL, schematics, or both
 - Fast, fully automatic place and route
- Waveform simulation with back annotated net delays
- PC and workstation platforms
- **Robust routing resources**
 - Fully automatic place and route of designs using up to 100 percent of logic resources
 - No hand routing required
- **32 (CY7C381) to 56 (CY7C382) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
 - Clock skew <1 ns
- **Input hysteresis provides high noise immunity**
- **Thorough testability**
 - Built-in scan path permits 100 percent factory testing of logic and I/O cells
 - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- **CMOS process with ViaLink™ programming technology**
 - High-speed metal-to-metal link
 - Non-volatile antifuse technology
- **68-pin PLCC is compatible with EPLD 1800 and LCA 2064 industry-standard pinouts**

Functional Description

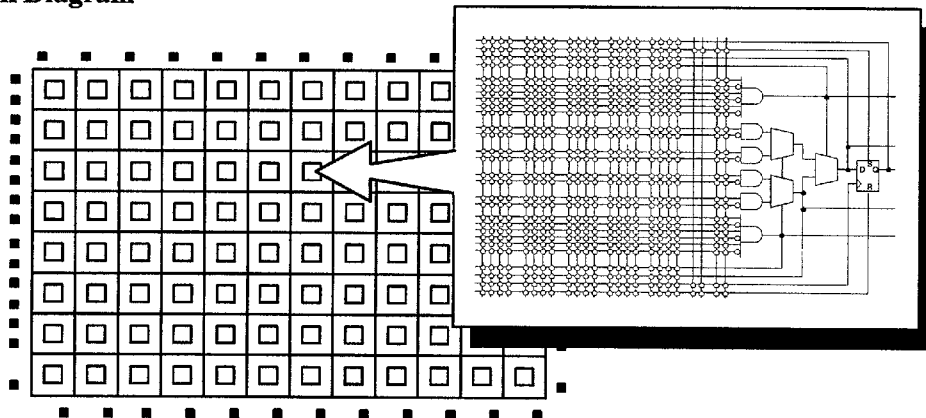
The CY7C381 and CY7C382 are members of the pASIC380 family of very high speed CMOS user-programmable ASIC (pASIC) devices. The 96 logic cell field-programmable gate array (FPGA) offers 1,000 typically usable "gate array" gates. This is equivalent to 3,000 EPLD or LCA gates. The CY7C381 is available in a 44-pin PLCC. The CY7C382 is available in a 68-pin PLCC and CPGA.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 100 MHz with input and output delays under 4 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C381 and CY7C382 using Cypress's *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C381 and CY7C382 feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Logic Block Diagram



■ I/O/HIGH-DRIVE INPUT CLOCK CELLS

44 or 68 PINS, INCLUDING 56 I/O CELLS, 6 INPUT HIGH-DRIVE CELLS, 2 INPUT/CLK (HIGH-DRIVE) CELLS

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Cypress Semiconductor Corporation

• 3901 North First Street

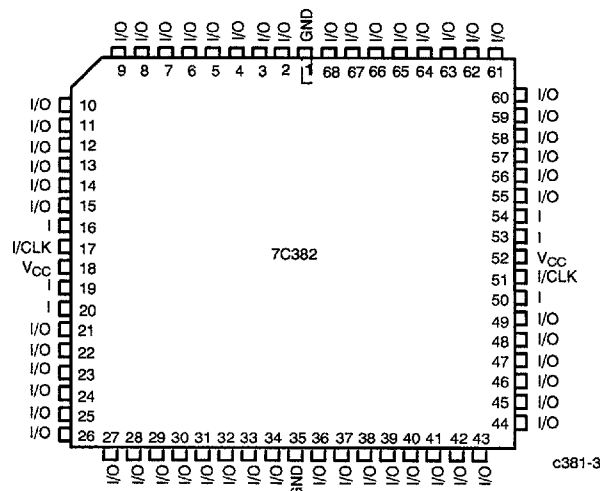
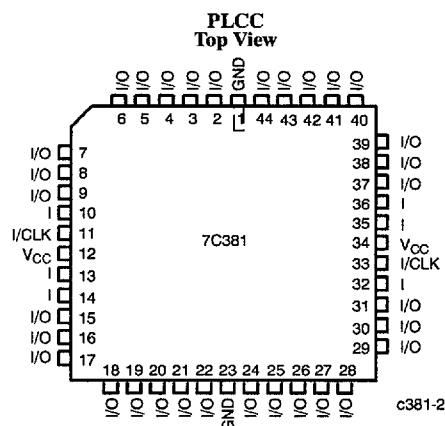
• San Jose

• CA 95134

• 408-943-2600

June 1992 - Revised February 1994

2589662 0014544 T27



Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	-40° to +85°C	5V ± 10%

Speed Grade	Industrial		Commercial	
	Min.	Max.	Min.	Max.
-0	0.4	1.67	0.46	1.55
-1	0.4	1.43	0.46	1.33
-2	0.4	1.35	0.46	1.25
-3			0.46	1.15

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = − 4.0 mA	3.7		V
		I _{OH} = − 8.0 mA	2.4		V
		I _{OH} = − 10.0 μA	V _{CC} − 0.1		V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA		0.4	V
		I _{OL} = 10.0 μA		0.1	V
V _{IH}	Input HIGH Voltage		2.0		V
V _{IL}	Input LOW Voltage			0.8	V
I _I	Input Leakage Current	V _{IN} = V _{CC} or GND	−10	+10	μA
I _{OZ}	Output Leakage Current	V _{IN} = V _{CC} or GND	−10	+10	μA
I _{OS}	Output Short Circuit Current	V _{OUT} = GND	−10	−80	mA
		V _{OUT} = V _{CC}	30	140	mA
I _{CC1}	Standby Supply Current	V _{IN} , V _{I/O} = V _{CC} or GND		10	mA
I _{CC2}	Supply Current ^[1, 2]	f = 1.0 MHz, V _I = V _{CC} or GND		20	mA



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Capacitance

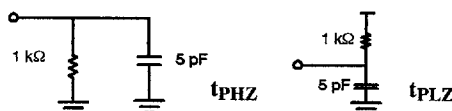
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance ^[3]	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	10	pF
C_{OUT}	Output Capacitance		20	pF

Switching Characteristics Over the Operating Range

Parameter	Description	Propagation Delays ^[4] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t _{PD}	Combinatorial Delay ^[5]	2.4	2.9	3.5	4.0	6.1	ns
t _{SU}	Set-Up Time ^[5]	2.7	2.7	2.7	2.7	2.7	ns
t _H	Hold Time	0	0	0	0	0	ns
t _{CLK}	Clock to Q Delay	2.4	2.9	3.4	3.9	6.0	ns
t _{SET}	Set Delay	3.4	4.0	4.6	5.1	7.4	ns
t _{RESET}	Reset Delay	3.6	4.0	4.5	5.0	6.9	ns
t _{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t _{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t _{SW}	Set Width	2.1	2.1	2.1	2.1	2.1	ns
t _{RW}	Reset Width	1.9	1.9	1.9	1.9	1.9	ns
INPUT CELLS							
t _{IN}	Input Delay (HIGH Drive)	3.7	3.8	4.2	4.6	6.4	ns
t _{INI}	Input, Inverting Delay (HIGH Drive)	3.5	3.6	4.0	4.4	6.2	ns
t _{IO}	Input Delay (Bidirectional Pad)	2.6	3.1	3.6	4.1	6.2	ns
t _{GCK}	Clock Buffer Delay ^[6]	3.6	3.7	3.8	3.9		ns
OUTPUT CELLS		Propagation Delays ^[4] with Output Load Capacitance (pF) of					
		30	50	75	100	150	
t _{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.1	6.8	ns
t _{OUTH}	Output Delay HIGH to LOW	2.7	3.5	4.6	5.7	7.9	ns
t _{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t _{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t _{PHZ}	Output Delay HIGH to Three-State ^[7]	2.9					ns
t _{PLZ}	Output Delay LOW to Three-State ^[7]	3.3					ns

Notes:

- Measured with six 16-bit counters configured internally and all outputs driving. To calculate power for your application, see the "pASIC380 Power vs. Operating Frequency" application note in the Cypress Semiconductor *Applications Handbook*.
- Guaranteed by design but not 100% tested.
- $C_I = 20\text{ pF}$ max. on pin 32 (7C381) or pin 50 (7C382).
- Worst-case propagation delay times over process variation at $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$. Multiply by the appropriate delay factor, K , for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
- These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
- Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
- The following loads are used for t_{PXZ} :





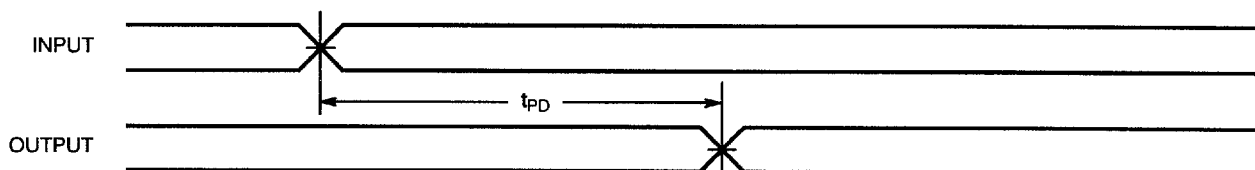
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High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays ^[4] with Fanout of					Unit
			12	24	48	72	96	
t_{IN}	High Drive Input Delay	1	7.9	11.2				ns
		2		8.0	9.7			ns
		3			8.6	10.4	11.8	ns
		4				9.4	10.8	ns
t_{INI}	High Drive Input, Inverting Delay	1	7.5	10.8				ns
		2		7.5	9.3			ns
		3			8.2	10.0	11.8	ns
		4				9.0	10.8	ns

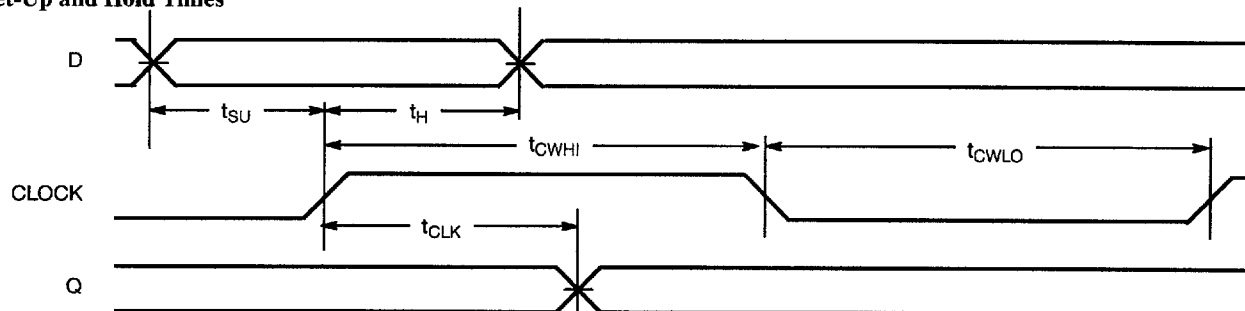
Switching Waveforms

Combinatorial Delay



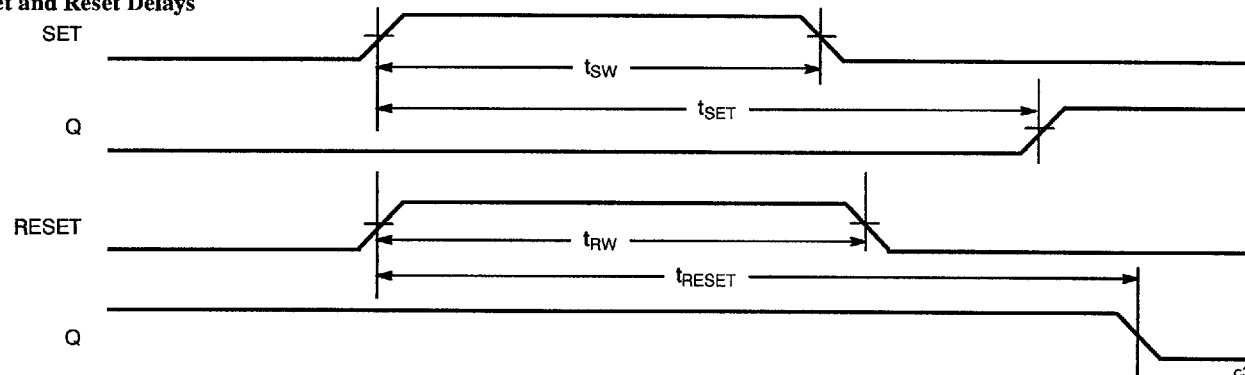
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Set-Up and Hold Times



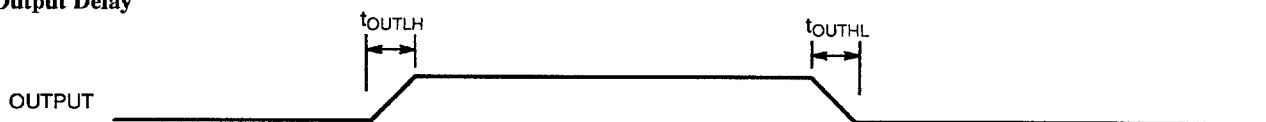
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Set and Reset Delays



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Output Delay



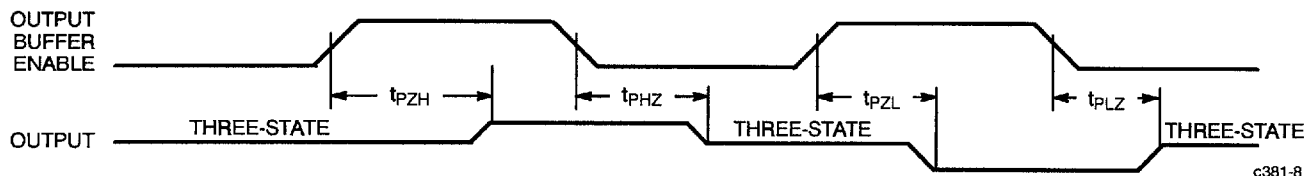
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Switching Waveforms (continued)

Three-State Delay

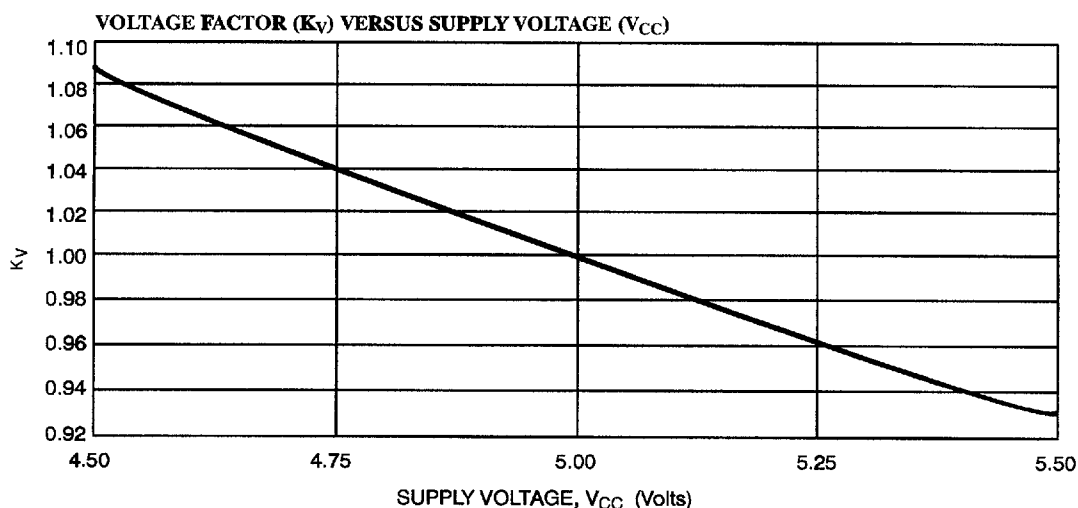


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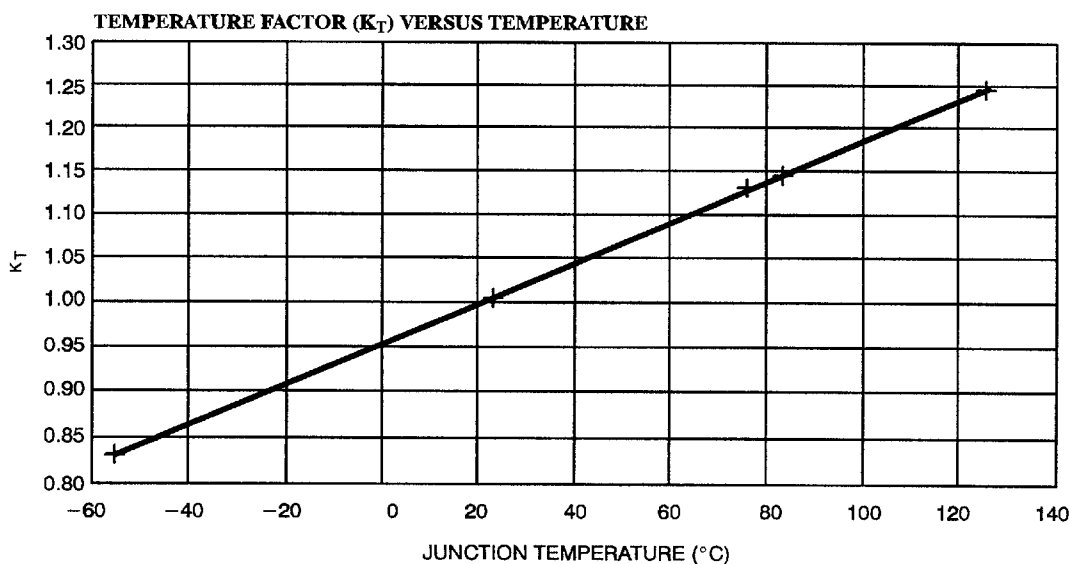
Typical AC Characteristics

Propagation delays depend on routing, fan-out, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K , as specified by the speed grade in the Delay

Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre-place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



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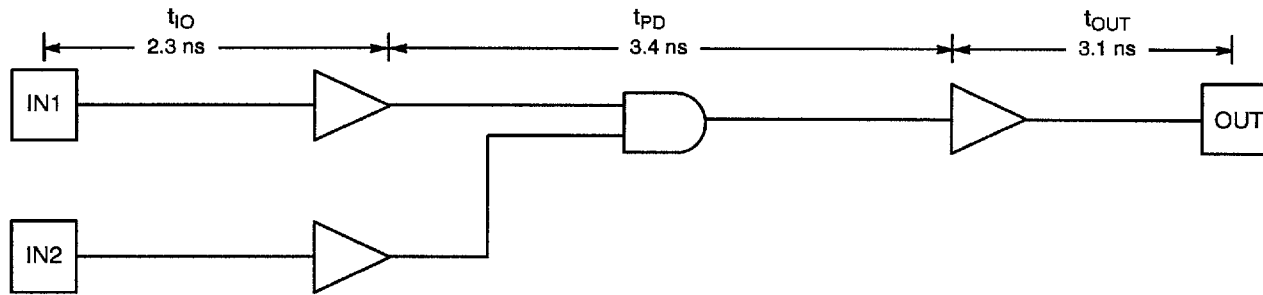


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* $\theta_{JA} = 45^{\circ}\text{C/WATT}$ FOR PLCC

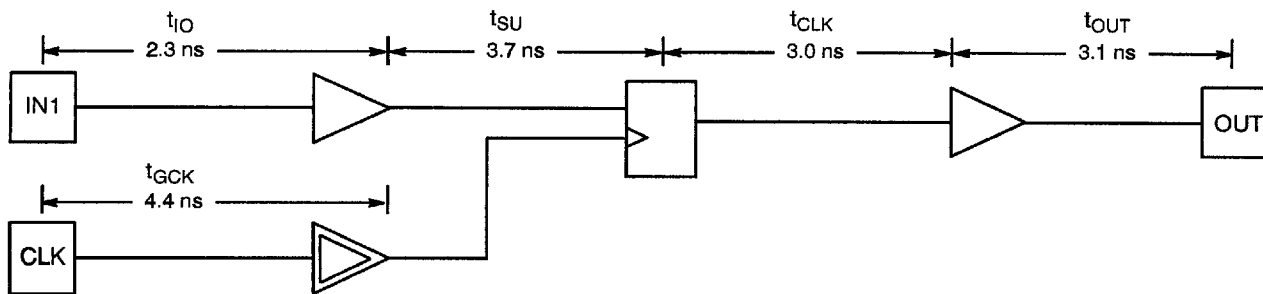


Combinatorial Delay Example (Load = 30 pF)



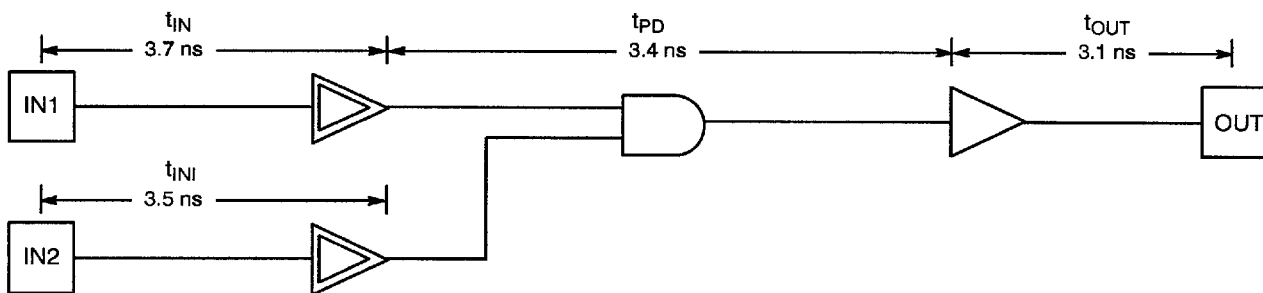
$$\text{INPUT DELAY} + \text{COMBINATORIAL DELAY} + \text{OUTPUT DELAY} = 8.8 \text{ ns}$$

Sequential Delay Example (Load = 30 pF)



$$\text{INPUT DELAY} + \text{REG SET-UP} + \text{CLOCK TO OUTPUT} + \text{OUTPUT DELAY} = 12.1 \text{ ns}$$

High-Drive Delay Example



$$\text{INPUT DELAY} + \text{COMBINATORIAL DELAY} + \text{OUTPUT DELAY} = 10.2 \text{ ns}$$



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Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
3	CY7C381-3JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
2	CY7C381-2JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381-2JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
1	CY7C381-1JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381-1JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
0	CY7C381-0JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C381-0JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
3	CY7C382-3GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382-3JC	J81	68-Lead Plastic Leaded Chip Carrier	
2	CY7C382-2GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382-2JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382-2GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C382-2JI	J81	68-Lead Plastic Leaded Chip Carrier	
1	CY7C382-1GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382-1JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382-1GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C382-1JI	J81	68-Lead Plastic Leaded Chip Carrier	
0	CY7C382-0GC	G68	68-Pin Grid Array (Cavity Down)	Commercial
	CY7C382-0JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C382-0GI	G68	68-Pin Grid Array (Cavity Down)	Industrial
	CY7C382-0JI	J81	68-Lead Plastic Leaded Chip Carrier	

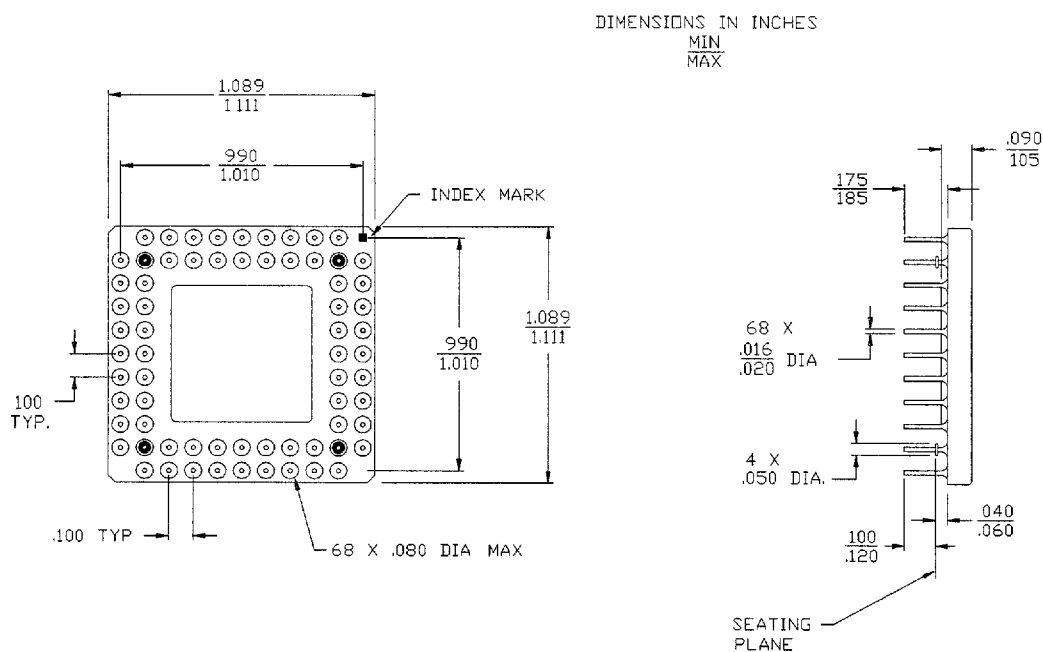
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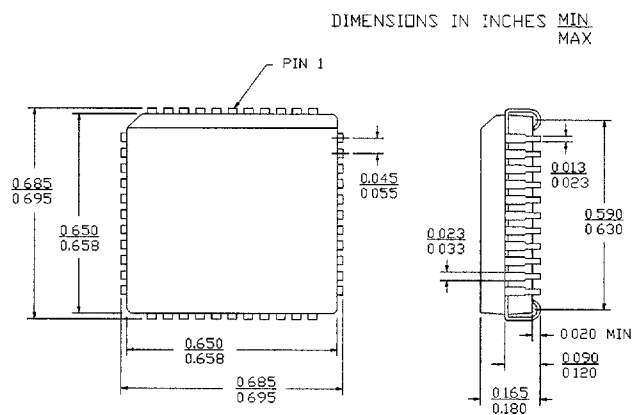
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Package Diagrams

68-Pin Grid Array (Cavity Down) G68



44-Lead Plastic Leaded Chip Carrier J67





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Package Diagrams (continued)

68-Lead Plastic Leaded Chip Carrier J81

