ispMACH™ 4000V/B/C/Z Fa

3.3V/2.5V/1.8V In-System Progr
SuperFAST™ High Den

July 2003

NEW! Industry's Lowest Power CPLDs! ispMACH 4000Z

Features

High Performance

- f_{MAX} = 400MHz maximum operating frequency
- t_{PD} = 2.5ns propagation delay
- Up to four global clock pins with programmable clock polarity control
- Up to 80 PTs per output

Ease of Design

- Enhanced macrocells with individual clock, reset, preset and clock enable controls
- Up to four global OE controls
- Individual local OE control per I/O pin
- Excellent First-Time-Fit™ and refit
- Fast path, SpeedLocking™ Path, and wide-PT path
- Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders

Zero Power (ispMACH 4000Z) and Low Power (ispMACH 4000V/B/C)

- Typical static current 10µA (4032Z)
- Typical static current 1.8mA (4000C)
- 1.8V core low dynamic power

Broad Device Offering

- Multiple temperature range support
  - Commercial: 0 to 90°C junction (T_j)
  - Industrial: -40 to 105°C junction (T_j
  - Automotive: -40 to 130°C junction (

Easy System Integration

- Operation with 3.3V, 2.5V or 1.8V LV
- Operation with 3.3V (4000V), 2.5V (4
  1.8V (4000C/Z) supplies
- 5V tolerant I/O for LVCMOS 3.3, LVT
  interfaces
- Hot-socketing
- Open-drain capability
- Input pull-up, pull-down or bus-keepe
- Programmable output slew rate
- 3.3V PCI compatible
- IEEE 1149.1 boundary scan testable
- 3.3V/2.5V/1.8V In-System Programm
  (ISP™) using IEEE 1532 compliant i
- I/O pins with fast setup path

Table 1. ispMACH 4000V/B/C Family Selection Guide

	ispMACH 4032V/B/C	ispMACH 4064V/B/C	ispMACH 4128V/B/C	ispMACH 4256V/B/C	ispMACH 4384V/B/C	i 4
Macrocells	32	64	128	256	384	
User I/O Options	30/32	30/32/64	64/92/96	64/96/128/160	128/192	
t_{PD} (ns)	2.5	2.5	2.7	3.0	3.5	
t_S (ns)	1.8	1.8	1.8	2.0	2.0	
t_{CO} (ns)	2.2	2.2	2.7	2.7	2.7	
f_{MAX} (MHz)	400	400	333	322	322	
Supply Voltages (V)	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.3/2.5/1.8V	3.
Pins/Package	44 TQFP 48 TQFP	44 TQFP 48 TQFP 100 TQFP	100 TQFP 128 TQFP 144 TQFP[1]	100 TQFP 144 TQFP[1] 176 TQFP 256 fpBGA[2]	176 TQFP 256 fpBGA	1 2

1. 3.3V (4000V) only.
2. 128-I/O and 160-I/O configurations.

Note: ispMACH 4032Z information is preliminary. ispMACH 4064Z/4128Z information is advance

Table 2. ispMACH 4000Z Family Selection Guide

	ispMACH 4032ZC[1]	ispMACH 4064ZC[2]	ispMACH 4128ZC[2]	ispMACH
Macrocells	32	64	128	2
User I/O Options	32	32/64	64/96	64/9
t_{PD} (ns)	3.5	4.0	4.5	5
t_S (ns)	2.2	2.8	2.9	3
t_{CO} (ns)	3.0	3.3	3.9	3
f_{MAX} (MHz)	267	250	220	2
Supply Voltage (V)	1.8	1.8	1.8	1
Standby Icc (µA)	20	25	30	4
Pins/Package	48 TQFP 56 csBGA	48 TQFP 56 csBGA 100 TQFP 132 csBGA	100 TQFP 132csBGA	100 132 176

1. Preliminary information.
2. Advance information.

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The fami of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of b the ispMACH 4000 architecture focuses on significant innovations to combine the highest performan power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of des robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing ity, routing, pin-out retention and density migration.

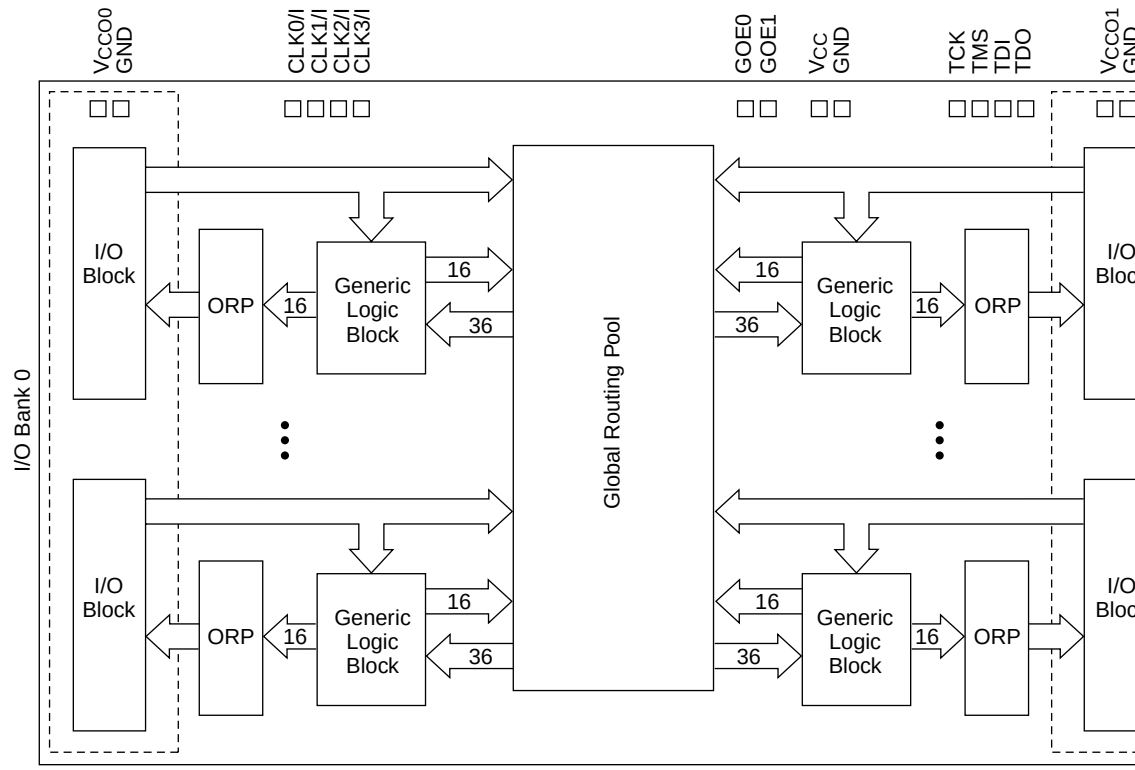
The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple dens binations in Thin Quad Flat Pack (TQFP) and Fine Pitch BGA (fpBGA) packages ranging from 44 to 25 Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 3.3V (4000V), 2. and 1.8V (4000C/Z) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. Additionally, inputs ca driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Th 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latc resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family membe 2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149 scan testing capability also allows product testing on automated test equipment.

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) inte by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (I contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply support a variety of standards independent of the chip or bank power supply. Outputs support the stan patible with the power supply provided to the bank. Support for a variety of standards helps designers designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank nected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

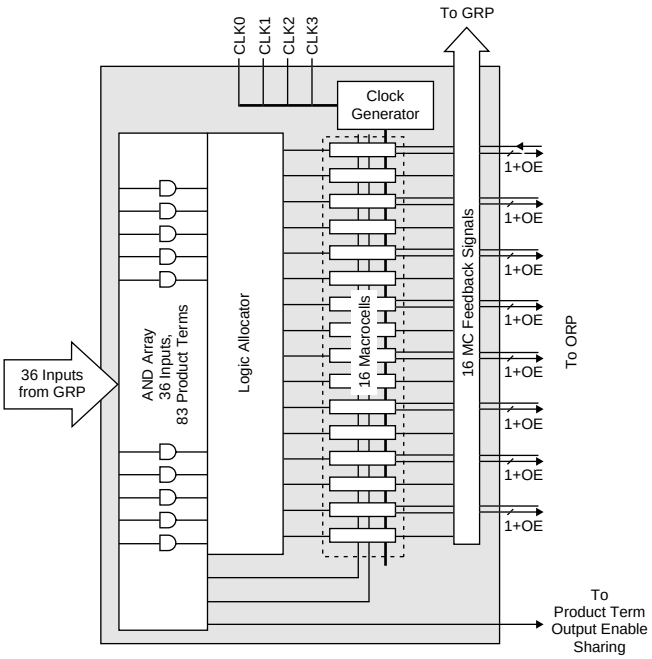
ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Ea 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the connected to the inputs of any other GLB on the device. Even if feedback signals return to the same G must go through the GRP. This mechanism ensures that GLBs communicate with each other with co predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to ated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins pled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

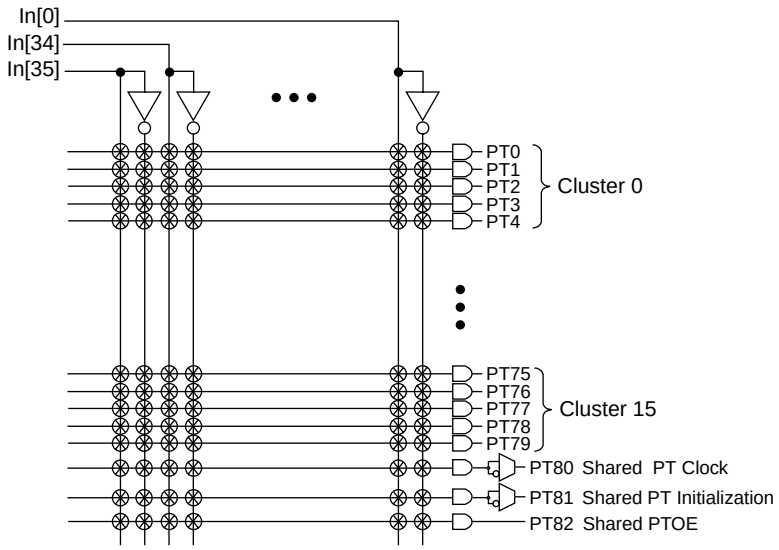


AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from t used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array nected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms fe allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initia Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted b fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster startin There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation Array.

Figure 3. AND Array



Note:
⊗ Indicates programmable fuse.

Enhanced Logic Allocator

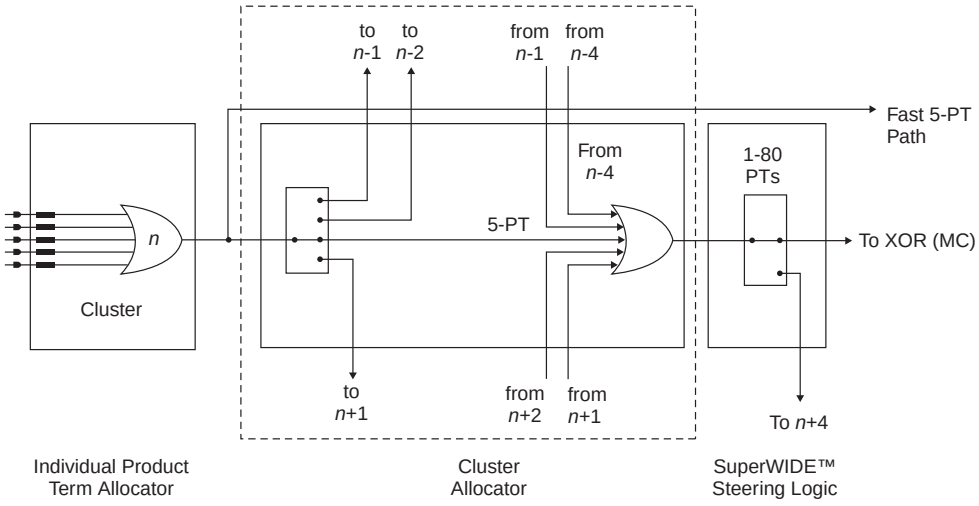
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each p cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) pro The software automatically considers the availability and distribution of product term clusters as it fits t within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 2 Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing v increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications by the design being implemented. Product terms that are used as logic are steered into a 5-input OR ated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cel with the cluster. Table 3 shows the available functions for each of the five product terms in the cluster. T output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and allocator.

Table 3. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation with more product terms. Table 4 shows which clusters can be steered to which macrocells. Used in thi the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster al accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can b

Table 4. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C
M1	C0	C1	C2	C
M2	C1	C2	C3	C
M3	C2	C3	C4	C
M4	C3	C4	C5	C
M5	C4	C5	C6	C
M6	C5	C6	C7	C
M7	C6	C7	C8	C
M8	C7	C8	C9	C
M9	C8	C9	C10	C
M10	C9	C10	C11	C
M11	C10	C11	C12	C
M12	C11	C12	C13	C
M13	C12	C13	C14	C
M14	C13	C14	C15	
M15	C14	C15	—	

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cl tor *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product ter and allowing performance to be increased through a single GLB implementation. Table 5 shows the p chains.

Table 5. Product Term Expansion Capability

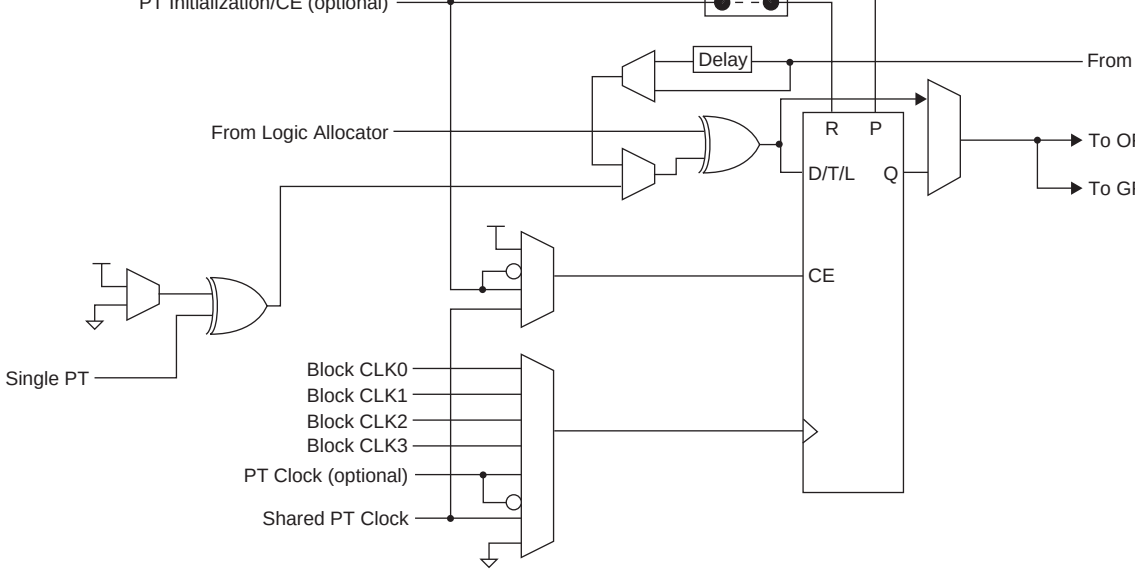
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max Macro
Chain-0	M0 → M4 → M8 → M12 → M0	75
Chain-1	M1 → M5 → M9 → M13 → M1	80
Chain-2	M2 → M6 → M10 → M14 → M2	75
Chain-3	M3 → M7 → M11 → M15 → M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super clu tor is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the ter is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell con grammable XOR gate, a programmable register/latch, along with routing for the logic and contro Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A pro delay in this path allows designers to choose between the fastest possible set-up time and zero hold ti

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, a complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select th eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected f
lowing four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

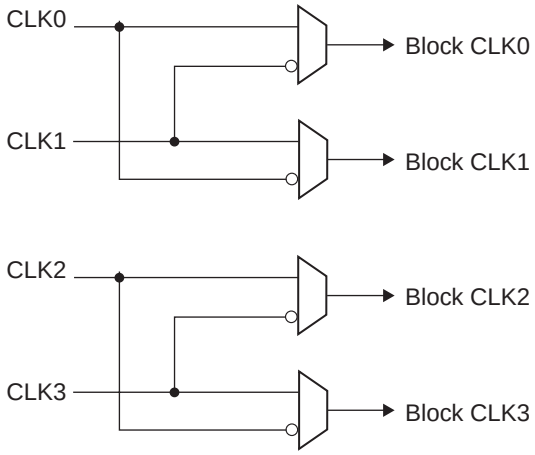
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and rese
There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At th
level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for se
tionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchange
flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops po
known state for predictable system initialization. If a macrocell is configured to SET on a signal from the
initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to R
signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESE
up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive u
delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has up to four clock pins that are also routed to the GRP to be used as in
pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock
can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combina
true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



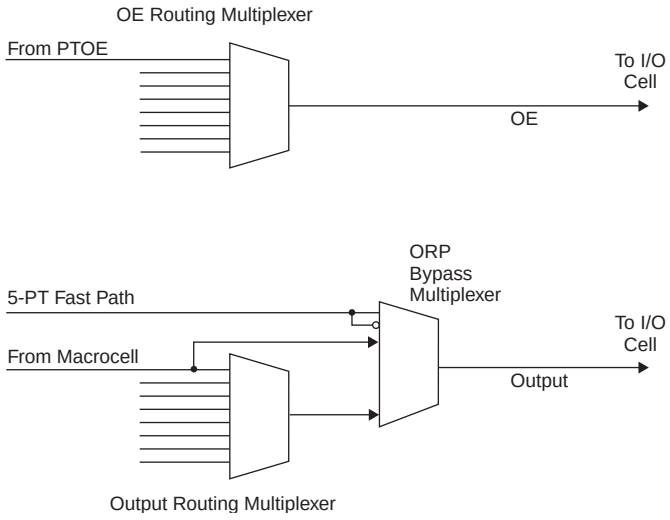
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within a This provides greater flexibility in determining the pinout and allows design changes to occur without a pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additiona put routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to output routing multipliers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and with dependent on the maximum number of I/Os available. Tables 5-9 provide the connection details.

Table 6. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 8. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 9. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8, M9
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

Table 10. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to ORP and be connected directly to the pin with either the regular output or the inverted output. This mul allows the register output to bypass the ORP to achieve faster t_{CO}.

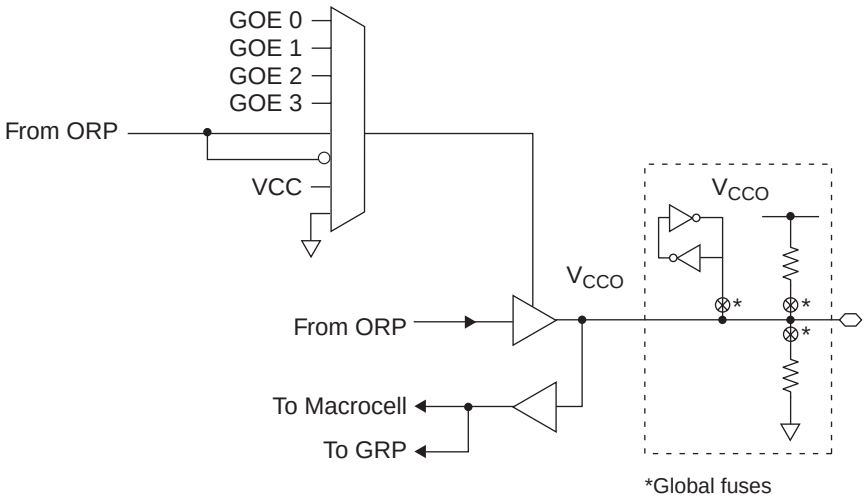
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplex maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. also be configured for open drain operation. Each input can be programmed to support a variety of stan pendent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor c Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The de hardware and software is such that when the device is erased or if the user does not specify, the input configured to be a Pull-up Resistor.

Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each ou individually configured for the higher speed transition (~3V/ns) or for the lower noise transition (~1V/n speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, les keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew used to achieve the highest speed. The slew rate is adjusted independent of power.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 devic 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual pu GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. I 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figur show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032

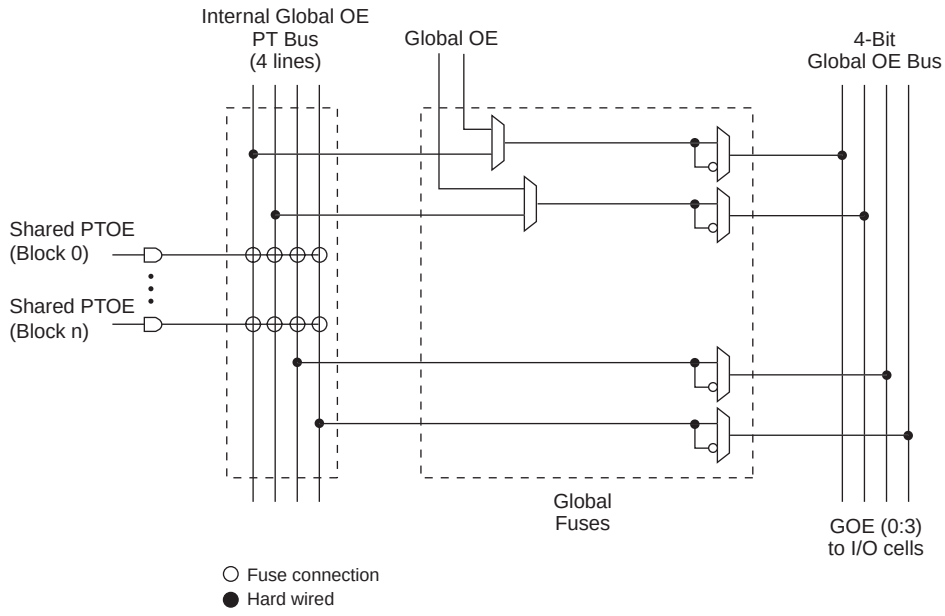
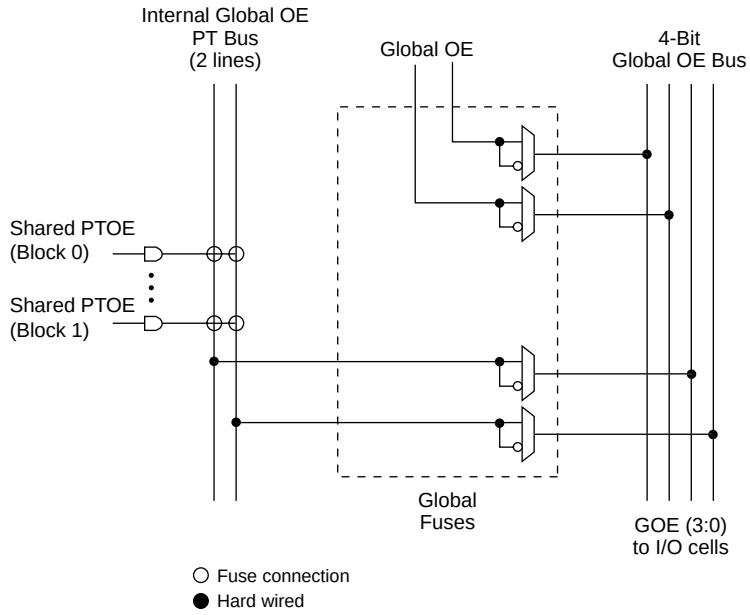


Figure 10. Global OE Generation for ispMACH 4032



Zero Power/Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full C approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously de standby power without needing any “turbo bits” or other power management schemes associated with sense-amplifier approach.

The zero power ispMACH 4000Z is based on the 1.8V ispMACH 4000C family. With innovative ci changes, the ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. functional testing of the circuit board on which the device is mounted through a serial scan path that ca critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded test nodes, or test node data to be captured and shifted out for verification. In addition, these devices c into a board-level serial scan path for more board-level testing. The test access port operates with a interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running a ity tests. As these tests are fast, by nature, the overhead and time that is required for configuration physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of de this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick c takes milliseconds to complete, whereas it takes seconds for the entire device to be programme ispVM™ System programming software can either perform the quick configuration through the PC par can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, tory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices pro tem Programming (ISP™) capability through the Boundary Scan Test Access Port. This capabilit implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a sta defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage ran based Lattice software facilitates in-system programming of ispMACH 4000 devices. The softwar JEDEC file output produced by the design implementation software, along with information about the and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a via the parallel port of a PC. Alternatively, the software can output files in formats understood by co mated test equipment. This equipment can then be used to program ispMACH 4000 devices during the circuit board.

Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized the array configuration patterns. Once programmed, this bit defeats readback of the programmed p device programmer, securing proprietary designs from competitors. Programming and verificatio defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot device requires that the device, during power-up and down, can tolerate active signals on the I/Os and out being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active ispMACH 4000 devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same pa the same pin-out. Furthermore, the architecture ensures a high success rate when performing desig from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization geted for a high density device to a lower density device. However, the exact details of the final resourc will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C/Z (1.8V)	ispMACH 4000B (2.5V)	ispMA (
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V	-0.5
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V	-0.5
Input or I/O Tristate Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V	-0.5
Storage Temperature	-65 to 150°C	-65 to 150°C	-65 t
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C	-55 t

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the devic operation of the device at these or any other conditions above those indicated in the operational sections of this is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6.0V, is permitted for a duratio
5. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max
V_{CC}	Supply Voltage for 1.8V Devices	ispMACH 4000C	1.65	1.95
		ispMACH 4000Z	1.7	1.9
	Supply Voltage for 2.5V Devices		2.3	2.7
	Supply Voltage for 3.3V Devices		3.0	3.6
T_j	Junction Temperature (Commercial)		0	90
	Junction Temperature (Industrial)		-40	105
	Junction Temperature (Automotive)		-40	130

Erase Reprogram Specifications

Parameter	Min.	Max
Erase/Reprogram Cycle	1,000	—

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. ispMACH 4000Z only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max
I_{IL}, I_{IH}[1]	Input Leakage Current	$0 < V_{IN} \le 3.6V$, $T_j = 105°C$	—	—	10
		$0 < V_{IN} \le 3.6V$, $T_j = 130°C$	—	—	15
I_{IH}[2]	Input High Leakage Current	$3.6V < V_{IN} \le 5.5V$, $T_j = 105°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	20
		$3.6V < V_{IN} \le 5.5V$, $T_j = 130°C$ $3.0V \le V_{CCO} \le 3.6V$	—	—	50
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-30	—	-150
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MIN)	30	—	150
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-30	—	—
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} *
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/O should only be placed in banks where $3.0V \le V_{CCO} \le 3.6V$.
3. T_A = 25°C, f = 1.0MHz

Supply Current, ispMACH 4000V/B/C

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.
ispMACH 4032V/B/C					
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	11.8	—
		Vcc = 2.5V	—	11.8	—
		Vcc = 1.8V	—	1.8	—
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.3	—
		Vcc = 2.5V	—	11.3	—
		Vcc = 1.8V	—	1.3	—
ispMACH 4064V/B/C					
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—
		Vcc = 2.5V	—	12	—
		Vcc = 1.8V	—	2	—
ICC^{5}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—
		Vcc = 2.5V	—	11.5	—
		Vcc = 1.8V	—	1.5	—
ispMACH 4128V/B/C					
$ICC^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12	—
		Vcc = 2.5V	—	12	—
		Vcc = 1.8V	—	2	—
ICC^{4}	Standby Power Supply Current	Vcc = 3.3V	—	11.5	—
		Vcc = 2.5V	—	11.5	—
		Vcc = 1.8V	—	1.5	—
ispMACH 4256V/B/C					
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	12.5	—
		Vcc = 2.5V	—	12.5	—
		Vcc = 1.8V	—	2.5	—
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12	—
		Vcc = 2.5V	—	12	—
		Vcc = 1.8V	—	2	—
ispMACH 4384V/B/C					
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	13.5	—
		Vcc = 2.5V	—	13.5	—
		Vcc = 1.8V	—	3.5	—
I_{CC}^{4}	Standby Power Supply Current	Vcc = 3.3V	—	12.5	—
		Vcc = 2.5V	—	12.5	—
		Vcc = 1.8V	—	2.5	—
ispMACH 4512V/B/C					
$I_{CC}^{1,2,3}$	Operating Power Supply Current	Vcc = 3.3V	—	14	—
		Vcc = 2.5V	—	14	—
		Vcc = 1.8V	—	4	—

Supply Current, ispMACH 4000V/B/C (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.
I_{CC}[4]	Standby Power Supply Current	Vcc = 3.3V	—	13	—
		Vcc = 2.5V	—	13	—
		Vcc = 1.8V	—	3	—

1. T_A = 25°C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. T_A = 25°C

Supply Current, ispMACH 4000Z

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	
ispMACH 4032ZC[1]					
ICC[3, 4, 5, 7]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	
		Vcc = 1.9V, T_A = 70°C	—	58	
		Vcc = 1.9V, T_A = 85°C	—	60	
		Vcc = 1.9V, T_A = 125°C	—	70	
ICC[6, 7]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	
		Vcc = 1.9V, T_A = 70°C	—	16	
		Vcc = 1.9V, T_A = 85°C	—	18	
		Vcc = 1.9V, T_A = 125°C	—	22	
ispMACH 4064ZC[2]					
ICC[3, 4, 5, 7]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		
ICC[6, 7]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		
ispMACH 4128ZC[2]					
ICC[3, 4, 5, 7]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		
ICC[6, 7]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		

Supply Current, ispMACH 4000Z (Cont.)

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	
ispMACH 4256ZC[2]					
ICC[3, 4, 5, 7]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		
ICC[6, 7]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—		
		Vcc = 1.9V, T_A = 70°C	—		
		Vcc = 1.9V, T_A = 85°C	—		
		Vcc = 1.9V, T_A = 125°C	—		

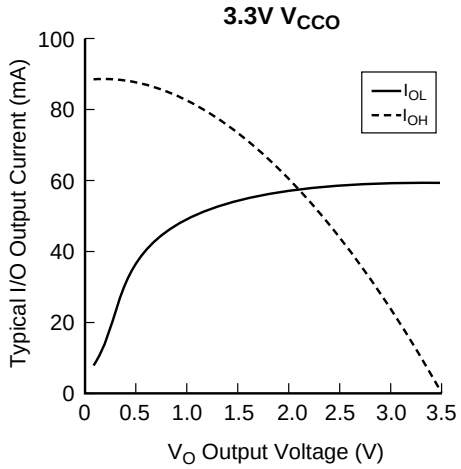
1. Preliminary information.
2. Advance information.
3. T_A = 25°C, frequency = 1.0 MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.
6. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified st
7. Includes V_{CCO} current without output loading.

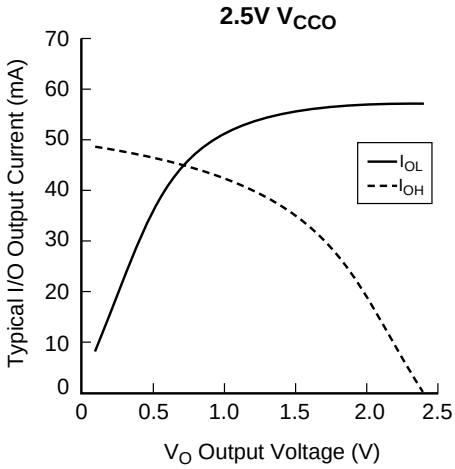
I/O DC Electrical Characteristics

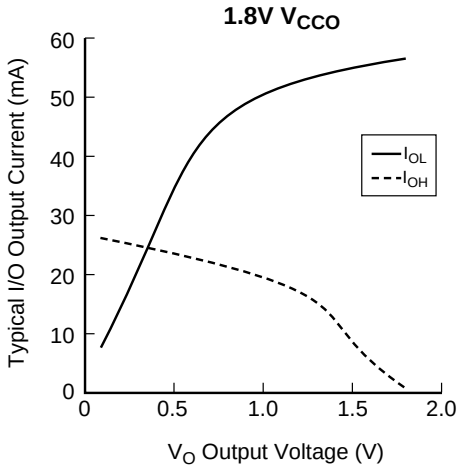
Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I
	Min (V)	Max (V)	Min (V)	Max (V)	Max (V)	Min (V)	(r
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	
					0.20	V_{CCO} - 0.20	
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	
					0.20	V_{CCO} - 0.20	
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	
					0.20	V_{CCO} - 0.20	
LVCMOS 1.8 (4000V/B)	-0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	
					0.20	V_{CCO} - 0.20	
LVCMOS 1.8 (4000C/Z)	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	
					0.20	V_{CCO} - 0.20	
PCI 3.3 (4000V/B)	-0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1
PCI 3.3 (4000C/Z)	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank a the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os betwee connections or between the last GND in a bank and the end of a bank.


3.3V VCCO
Typical I/O Output Current (mA)
100
80
60
40
20
0
0 0.5 1.0 1.5 2.0 2.5 3.0 3.5
VO Output Voltage (V)
IOL
IOH


2.5V VCCO
Typical I/O Output Current (mA)
70
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0 2.5
VO Output Voltage (V)
IOL
IOH


1.8V VCCO
Typical I/O Output Current (mA)
60
50
40
30
20
10
0
0 0.5 1.0 1.5 2.0
VO Output Voltage (V)
IOL
IOH

ispMACH 4000V/B/C External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-25		-27		-3		-35	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	M
t_{PD}	5-PT bypass combinatorial propagation delay	—	2.5	—	2.7	—	3.0	—	
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	3.2	—	3.5	—	3.8	—	
t_S	GLB register setup time before clock	1.8	—	1.8	—	2.0	—	2.0	
t_{ST}	GLB register setup time before clock with T-type register	2.0	—	2.0	—	2.2	—	2.2	
t_{SIR}	GLB register setup time before clock, input register path	0.7	—	1.0	—	1.0	—	1.0	
t_{SIRZ}	GLB register setup time before clock with zero hold	1.7	—	2.0	—	2.0	—	2.0	
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	
t_{HIR}	GLB register hold time after clock, input register path	0.9	—	1.0	—	1.0	—	1.0	
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	
t_{CO}	GLB register clock-to-output delay	—	2.2	—	2.7	—	2.7	—	
t_R	External reset pin to output delay	—	3.5	—	4.0	—	4.4	—	
t_{RW}	External reset pulse duration	1.5	—	1.5	—	1.5	—	1.5	
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	4.0	—	4.5	—	5.0	—	
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	5.0	—	6.5	—	8.0	—	
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	3.0	—	3.5	—	4.0	—	
t_{CW}	Global clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.1	—	1.3	—	1.3	—	1.3	
t_{WIR}	Input register clock width, high or low	1.1	—	1.3	—	1.3	—	1.3	
f_{MAX}[4]	Clock frequency with internal feedback	400	—	333	—	322	—	322	
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	250	—	222	—	212	—	212	

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4000V/B/C External Switching Characteristics (Cont.)

Over Recommended Operating Conditions

Parameter	Description[1, 2, 3]	-5		-75		-10	
		Min.	Max.	Min.	Max.	Min.	M
t_{PD}	5-PT bypass combinatorial propagation delay	—	5.0	—	7.5	—	1
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	5.5	—	8.0	—	1
t_S	GLB register setup time before clock	3.0	—	4.5	—	5.5	
t_{ST}	GLB register setup time before clock with T-type register	3.2	—	4.7	—	5.5	
t_{SIR}	GLB register setup time before clock, input register path	1.2	—	1.7	—	1.7	
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	2.7	—	2.7	
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	
t_{CO}	GLB register clock-to-output delay	—	3.40	—	4.5	—	
t_R	External reset pin to output delay	—	6.30	—	9.0	—	1
t_{RW}	External reset pulse duration	2.0	—	4.0	—	4.0	
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.00	—	9.0	—	1
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.00	—	10.3	—	1
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	5.00	—	7.0	—	
t_{CW}	Global clock width, high or low	2.2	—	3.3	—	4.0	
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.2	—	3.3	—	4.0	
t_{WIR}	Input register clock width, high or low	2.2	—	3.3	—	4.0	
f_{MAX}[4]	Clock frequency with internal feedback	227	—	168	—	125	
f_{MAX} (Ext.)	Clock frequency with external feedback, [1/ (t_S + t_{CO})]	156	—	111	—	86	

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.

ispMACH 4032Z External Switching Characteristics[1]

Over Recommended Operating Conditions

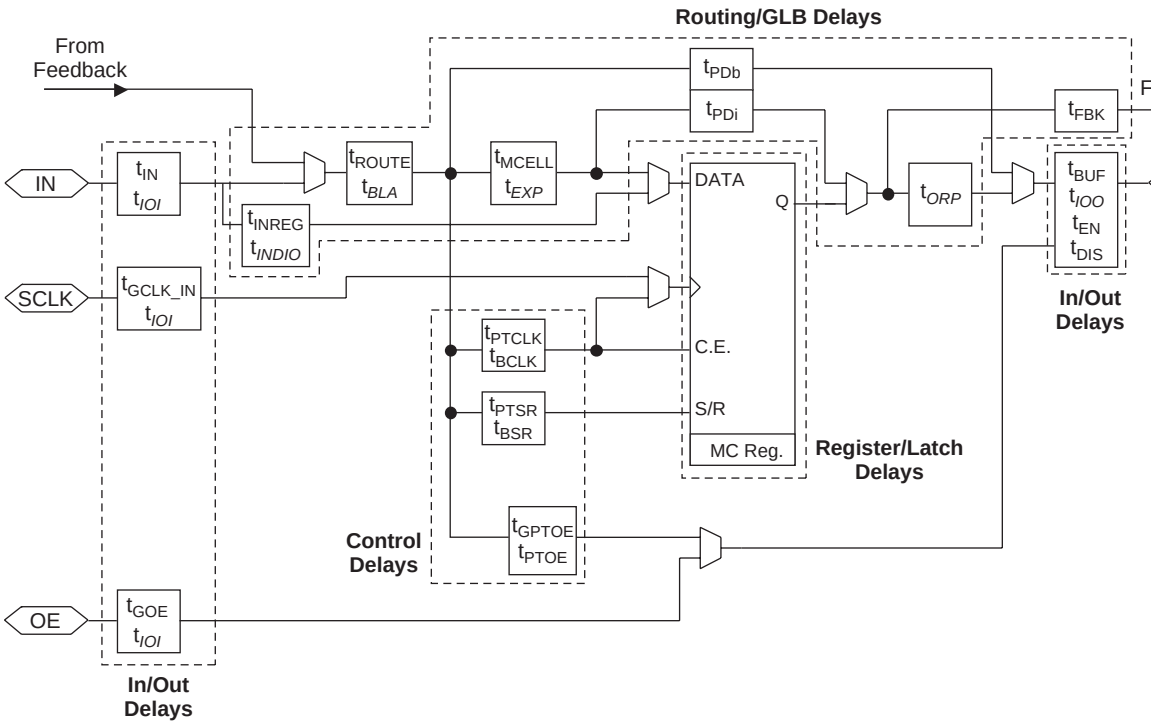
Parameter	Description[2, 3, 4]	-35		-5		-75	
		Min.	Max.	Min.	Max.	Min.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	3.5	—	5.0	—	
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.4	—	5.5	—	
t_S	GLB register setup time before clock	2.2	—	3.0	—	4.5	
t_{ST}	GLB register setup time before clock with T-type register	2.5	—	3.2	—	4.7	
t_{SIR}	GLB register setup time before clock, input register path	1.0	—	1.2	—	1.7	
t_{SIRZ}	GLB register setup time before clock with zeto hold	2.0	—	2.2	—	2.7	
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.0	
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	
t_{CO}	GLB register clock-to-output delay	—	3.0	—	3.4	—	
t_R	External reset pin to output delay	—	5.0	—	6.3	—	
t_{RW}	External reset pulse duration	1.5	—	2.0	—	4.0	
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	8.0	—	
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	6.5	—	8.0	—	
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	5.0	—	
t_{CW}	Global clock width, high or low	1.0	—	2.2	—	3.3	
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	2.2	—	3.3	
t_{WIR}	Input register clock width, high or low	1.0	—	2.2	—	3.3	
f_{MAX}[5]	Clock frequency with internal feedback	267	—	200	—	150	
t_{MAX} (Ext.)	clock frequency with external feedback, [1/(tS + tCO)]	192	—	156	—	111	

1. Preliminary information.
2. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
3. Measured using standard switching GRP loading of 1 and 1 output switching.
4. Pulse widths and clock widths less than minimum will cause unknown behavior.
5. Standard 16-bit counter using GRP feedback.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple model provided in Figure 11 shows the specific delay paths. Once the implementation of a given funct mined either conceptually or from the software report file, the delay path of the function can easily be from the timing model. The Lattice design tools report the timing delays based on the same timing mod ticular design. Note that the internal timing parameters are given for reference only, and are not tested nal timing parameters are tested and guaranteed for every device. For more information on the timing usage, please refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guide*

Figure 11. ispMACH 4000 Timing Model



Note: Italicized items are optional delay

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5	
In/Out Delays									
t_{IN}	Input Buffer Delay	—	0.60	—	0.60	—	0.70	—	0.7
t_{GOE}	Global OE Pin Delay	—	2.04	—	2.54	—	3.04	—	3.5
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.78	—	1.28	—	1.28	—	1.2
t_{BUF}	Delay through Output Buffer	—	0.85	—	0.85	—	0.85	—	0.8
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0.96	—	0.9
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0.96	—	0.9
Routing/GLB Delays									
t_{ROUTE}	Delay through GRP	—	0.61	—	0.81	—	1.01	—	1.0
t_{MCELL}	Macrocell Delay	—	0.45	—	0.55	—	0.55	—	0.6
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.11	—	0.31	—	0.31	—	0.3
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.0
t_{PDb}	5-PT Bypass Propagation Delay	—	0.44	—	0.44	—	0.44	—	0.9
t_{PDi}	Macrocell Propagation Delay	—	0.64	—	0.64	—	0.64	—	0.9
Register/Latch Delays									
t_S	D-Register Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—
t_{ST}	T-Register Setup Time (Global Clock)	1.12	—	1.32	—	1.22	—	1.12	—
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—
t_H	D-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—
t_{HT}	T-Register Hold Time	0.88	—	0.68	—	0.98	—	1.08	—
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.82	—	1.37	—	1.27	—	1.27	—
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	—	1.45	—
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.88	—	0.63	—	0.73	—	0.73	—
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	0.63	—	0.73	—	0.73	—
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.52	—	0.52	—	0.5
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	—	2.25	—
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	—	1.88	—
t_{SL}	Latch Setup Time (Global Clock)	0.92	—	1.12	—	1.02	—	0.92	—
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.42	—	1.32	—	1.32	—	1.32	—
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	—	1.17	—
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0.33	—	0.3

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-2.5		-2.7		-3		-3.5	
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0.25	—	0.2
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	—	0.28	—
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	—	1.67	—
Control Delays									
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	1.12	—	1.1
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0.87	—	0.8
t_{BSR}	Block PT Set/Reset Delay	—	1.83	—	1.83	—	1.83	—	1.8
t_{PTSR}	Macrocell PT Set/Reset Delay	—	1.11	—	1.41	—	1.51	—	1.6
t_{GPTOE}	Global PT OE Delay	—	2.83	—	4.13	—	5.33	—	5.3
t_{PTOE}	Macrocell PT OE Delay	—	1.83	—	2.13	—	2.33	—	2.8

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further d

ispMACH 4000V/B/C Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10	
		Min.	Max.	Min.	Max.	Min.	M
In/Out Delays							
t_{IN}	Input Buffer Delay	—	0.95	—	1.50	—	2
t_{GOE}	Global OE Pin Delay	—	4.04	—	6.04	—	1
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.83	—	2.28	—	3
t_{BUF}	Delay through Output Buffer	—	1.00	—	1.50	—	1
t_{EN}	Output Enable Time	—	0.96	—	0.96	—	0
t_{DIS}	Output Disable Time	—	0.96	—	0.96	—	0
Routing/GLB Delays							
t_{ROUTE}	Delay through GRP	—	1.51	—	2.26	—	3
t_{MCELL}	Macrocell Delay	—	1.05	—	1.45	—	1
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.56	—	0.96	—	1
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0
t_{PDb}	5-PT Bypass Propagation Delay	—	1.54	—	2.24	—	3
t_{PDi}	Macrocell Propagation Delay	—	0.94	—	1.24	—	1
Register/Latch Delays							
t_{S}	D-Register Setup Time (Global Clock)	1.32	—	1.57	—	1.57	
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	
t_{ST}	T-Register Setup Time (Global Clock)	1.52	—	1.77	—	1.77	
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	
t_{H}	D-Register Hold Time	1.68	—	2.93	—	3.93	
t_{HT}	T-Register Hold Time	1.68	—	2.93	—	3.93	
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.52	—	1.57	—	1.57	
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	
t_{HIR}	D-Input Register Hold Time (Global Clock)	0.68	—	1.18	—	1.18	
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.68	—	1.18	—	1.18	
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.52	—	0.67	—	1
t_{CES}	Clock Enable Setup Time	2.25	—	2.25	—	2.25	
t_{CEH}	Clock Enable Hold Time	1.88	—	1.88	—	1.88	
t_{SL}	Latch Setup Time (Global Clock)	1.32	—	1.57	—	1.57	
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	1.32	—	1.32	
t_{HL}	Latch Hold Time	1.17	—	1.17	—	1.17	
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	—	0
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	—	0
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	0.28	—	0.28	
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	1.67	—	1.67	
Control Delays							
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.12	—	0
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	0.87	—	0
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	—	1
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.51	—	3.41	—	3

ispMACH 4000V/B/C Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10	
		Min.	Max.	Min.	Max.	Min.	M
t_{GPTOE}	Global PT OE Delay	—	5.58	—	5.58	—	5
t_{PTOE}	Macrocell PT OE Delay	—	3.58	—	4.28	—	4

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further d

ispMACH 4032Z Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-35		-5		-75	
		Min.	Max.	Min.	Max.	Min.	
In/Out Delays							
t_{IN}	Input Buffer Delay	—	0.75	—	0.95	—	
t_{GOE}	Global OE Pin Delay	—	2.90	—	3.20	—	
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.50	—	1.90	—	
t_{BUF}	Delay through Output Buffer	—	0.65	—	0.90	—	
t_{EN}	Output Enable Time	—	1.60	—	1.80	—	
t_{DIS}	Output Disable Time	—	1.35	—	1.60	—	
Routing/GLB Delays							
t_{ROUTE}	Delay through GRP	—	1.70	—	2.25	—	
t_{MCELL}	Macrocell Delay	—	0.65	—	1.00	—	
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.91	—	0.75	—	
t_{FBK}	Internal Feedback Delay	—	0.35	—	0.50	—	
t_{PDb}	5-PT Bypass Propagation Delay	—	0.40	—	0.90	—	
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.35	—	
Register/Latch Delays							
t_{S}	D-Register Setup Time (Global Clock)	0.60	—	0.70	—	1.57	
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.55	—	1.50	—	1.65	
t_{ST}	T-Register Setup Time (Global Clock)	0.90	—	0.90	—	1.77	
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.75	—	1.50	—	1.32	
t_{H}	D-Register Hold Time	1.60	—	2.30	—	2.93	
t_{HT}	T-Resister Hold Time	1.60	—	2.30	—	2.93	
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.84	—	1.40	—	1.83	
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	1.45	
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.16	—	0.80	—	0.87	
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.88	—	1.00	—	1.18	
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.45	—	0.55	—	
t_{CES}	Clock Enable Setup Time	1.00	—	1.40	—	2.00	
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	0.00	
t_{SL}	Latch Setup Time (Global Clock)	0.65	—	1.02	—	1.57	
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.75	—	1.32	—	1.32	
t_{HL}	Latch Hold Time	1.40	—	1.17	—	1.17	
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.33	—	
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.30	—	0.25	—	
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	1.00	—	0.28	—	
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.67	—	
Control Delays							
t_{BCLK}	GLB PT Clock Delay	—	1.50	—	1.12	—	
t_{PTCLK}	Macrocell PT Clock Delay	—	1.70	—	0.87	—	
t_{BSR}	GLB PT Set/Reset Delay	—	1.10	—	1.83	—	
t_{PTSR}	Macrocell PT Set/Reset Delay	—	0.50	—	1.87	—	
t_{GPTOE}	Global PT OE Delay	—	2.45	—	3.00	—	

ispMACH 4032Z Internal Timing Parameters[1] (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-35		-5		-75	
		Min.	Max.	Min.	Max.	Min.	
t_{PTOE}	Macrocell PT OE Delay	—	2.95	—	3.00	—	

1. Preliminary information.

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data she details.

ispMACH 4000V/B/C Timing Adders[1]

Adder Type	Base Parameter	Description	-25		-27		-3		-35	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	
Optional Delay Adders										
t_{INDIO}	t_{INREG}	Input register delay	—	0.95	—	1.00	—	1.00	—	
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	0.33	—	
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	0.05	—	
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.03	—	0.05	—	0.05	—	
t_{IOI} Input Adjusters										
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	
t_{IOO} Output Adjusters										
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	

Note: Open drain timing is the same as corresponding LVCMOS timing.

1. Refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guidelines* for information regarding use of

ispMACH 4000V/B/C Timing Adders[1]

Adder Type	Base Parameter	Description	-5		-75		-10	
			Min.	Max.	Min.	Max.	Min.	
Optional Delay Adders								
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.33	—	
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.05	—	
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	—	
t_{IOI} Input Adjusters								
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	
t_{IOO} Output Adjusters								
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	

Note: Open drain timing is the same as corresponding LVCMOS timing.

1. Refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guidelines* for information regarding use of

ispMACH 4032Z Timing Adders[1, 2]

Adder Type	Base Parameter	Description	-35		-5		-7	
			Min.	Max.	Min.	Max.	Min.	M
Optional Delay Adders								
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.00	—	1
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.40	—	0.50	—	0
t_{ORP}	—	Output routing pool delay	—	0.40	—	0.05	—	0
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.04	—	0.05	—	0
t_{IOI} Input Adjusters								
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.70	—	0.70	—	0
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.70	—	0.70	—	0
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.40	—	0.40	—	0
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.70	—	0.70	—	0
t_{IOO} Output Adjusters								
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.70	—	0.70	—	0
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.70	—	0.70	—	0
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.40	—	0.40	—	0
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.70	—	0.70	—	0
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1

1. Preliminary information.
2. Refer to Technical Note TN 1004: ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use adders.

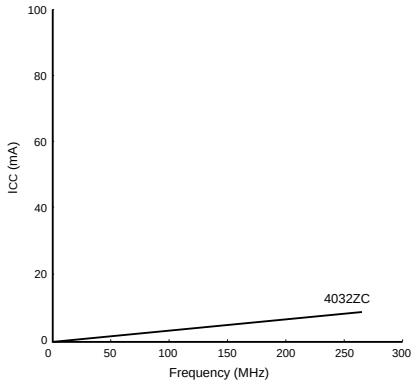
Note: Open drain timing is the same as corresponding LVCMOS timing.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—
t_{BTSU}	TCK [BSCAN test] setup time	8	—
t_{BTH}	TCK [BSCAN test] hold time	10	—
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10
t_{BTCPSU}	BSCAN test Capture register setup time	8	—
t_{BTCPH}	BSCAN test Capture register hold time	10	—
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25

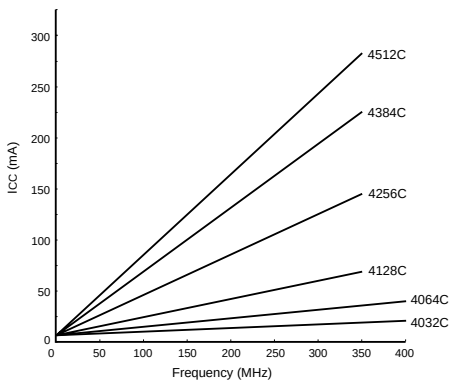
Power Consumption

ispMACH 4000Z
Typical I_{CC} vs. Frequency
(Preliminary Information)



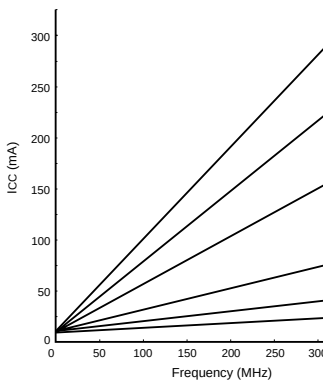
Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.

ispMACH 4000C
Typical I_{CC} vs. Frequency



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25°C.

ispMACH 4000V/B
Typical I_{CC} vs. Frequen



Note: The devices are configured with maxi of 16-bit counters, typical current at 3.3V, 2

Power Estimation Coefficients[1]

Device	A	B
ispMACH 4032V/B	11.3	0.010
ispMACH 4032C	1.3	0.010
ispMACH 4064V/B	11.5	0.010
ispMACH 4064C	1.5	0.010
ispMACH 4128V/B	11.5	0.011
ispMACH 4128C	1.5	0.011
ispMACH 4256V/B	12	0.011
ispMACH 4256C	2	0.011
ispMACH 4384V/B	12.5	0.013
ispMACH 4384C	2.5	0.013
ispMACH 4512V/B	13	0.013
ispMACH 4512C	3	0.013
ispMACH 4032ZC[2]	0.020	0.010
ispMACH 4064ZC[3]		
ispMACH 4128ZC[3]		
ispMACH 4256ZC[3]		

1. For further information about the use of these coefficients, refer to Technical Note TN1005, *Power Estimation in ispMACH 4000V/B/C Devices.*
2. Preliminary information.
3. Advance information.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, c
voltage, and other test conditions are shown in Table 11.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

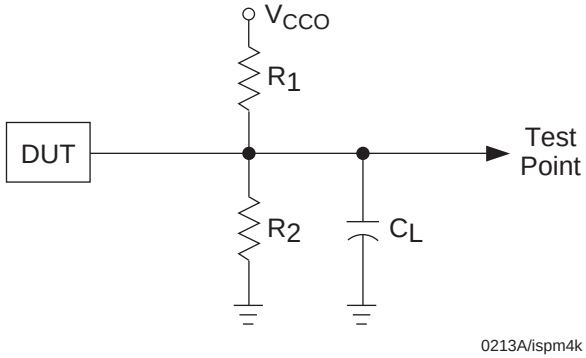


Table 11. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3
				LVCMOS 2.5 = $V_{CCO}/2$	LVCMOS 2
				LVCMOS 1.8 = $V_{CCO}/2$	LVCMOS 1
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is use the state machine	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock th state machine	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift dat	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as pins	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic arr reference (alpha) and z is macrocell reference (numeric). z: 0-15	
	ispMACH 4032	y: A-B
	ispMACH 4064	y: A-D
	ispMACH 4128	y: A-H
	ispMACH 4256	y: A-P
	ispMACH 4384	y: A-P, AX-HX
	ispMACH 4512	y: A-P, AX-PX

1. In some packages, certain I/O are only available for use as inputs. See the signal connections table for details.

ispMACH 4000V/B/C/Z Power Supply and NC Connections[1]

Signal	44 TQFP[4]	48 TQFP[4]	56 csBGA[7]	100 TQFP[4]	128 TQFP[4]	144 TQFP[4]	176 TQFP[4]	256 fpBGA[2, 3, 7]
VCC	11, 33	12, 36	K2, A9	25, 40, 75, 90	32, 51, 96, 115	36, 57, 108, 129	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9,
VCCO0	6	6	F3	13, 33, 95	3, 17, 30, 41, 122	3, 19, 34, 47, 136	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
VCCO1	28	30	E8	45, 63, 83	58, 67, 81, 94, 105	64, 75, 91, 106, 119	78, 92, 110, 128, 144	D11, F13, H10, J10, L13,
GND	12, 34	13, 37	H3, C8	1, 26, 51, 76	1, 33, 65, 97	1, 37, 73, 109	2, 46[5], 65, 90, 134, 153	A1, A16, C6, C11, F3, F14 H8, H9, J8, J9, K7, K10, L P11, T1, T16
GND (Bank 0)	5	5	D3	7, 18, 32, 96	10, 24, 40, 113, 123	10, 18[6], 27, 46, 127, 137	13, 31, 55, 155, 167	
GND (Bank 1)	27	29	G8	46, 57, 68, 82	49, 59, 74, 88, 104	55, 65, 82, 90[6], 99, 118	67, 79, 101, 119, 143	
NC	—	—	**4032Z**: A8, B10, E1, E3, F8, F10, J1, K3	—	—	**4128V**: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 **4256V**: 18, 90	1, 43, 44, 45, 89, 131, 132, 133	**4256V/B/C, 128 I/O:** A4, A A12, A13, A15, B5, B6, B1 C7, D1, D4, D5, D10, D12 E2, E4, E5, E7, E10, E13, E16, F1, F2, F15, F16, G1 G6, G12, G13, G14, J11, L1, L2, L12, L15, L16, M1, M4, M5, M12, M13, M15, N7, N10, N12, N14, P5, P R6, R11, R12, R16, T2, T4 T11, T12, T13, T15 **4256V/B/C, 160 I/O:** A5, A B6, B11, B12, B14, D4, D5 E4, E5, E13, E15, E16, F1 G1, G5, G12, G14, L1, L2 L16, M1, M2, M3, M12, M1 N14, P5, R4, R5, R6, R11 T4, T5, T12, T15 **4384V/B/C:** B5, B12, D5, E15, E16, F2, L12, M1, M2 R5, R12, T4 **4512V/B/C:** None

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are as the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V_{CCO} balls connect to two power planes within the package, one for V_{CCO0} and one for V_{CCO1}.
4. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
5. ispMACH 4384V/B/C pin 46 is tied to GND (Bank 0).
6. ispMACH 4128V only.
7. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and nume ascending horizontally.

ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
1	-	TDI	-	TDI	
2	0	A5	A^5	A10	
3	0	A6	A^6	A12	
4	0	A7	A^7	A14	
5	0	GND (Bank 0)	-	GND (Bank 0)	
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
7	0	A8	A^8	B0	
8	0	A9	A^9	B2	
9	0	A10	A^10	B4	
10	-	TCK	-	TCK	
11	-	VCC	-	VCC	
12	-	GND	-	GND	
13	0	A12	A^12	B8	
14	0	A13	A^13	B10	
15	0	A14	A^14	B12	
16	0	A15	A^15	B14	
17	1	CLK2/I	-	CLK2/I	
18	1	B0	B^0	C0	
19	1	B1	B^1	C2	
20	1	B2	B^2	C4	
21	1	B3	B^3	C6	
22	1	B4	B^4	C8	
23	-	TMS	-	TMS	
24	1	B5	B^5	C10	
25	1	B6	B^6	C12	
26	1	B7	B^7	C14	
27	1	GND (Bank 1)	-	GND (Bank 1)	
28	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
29	1	B8	B^8	D0	
30	1	B9	B^9	D2	
31	1	B10	B^10	D4	
32	-	TDO	-	TDO	
33	-	VCC	-	VCC	
34	-	GND	-	GND	
35	1	B12	B^12	D8	
36	1	B13	B^13	D10	
37	1	B14	B^14	D12	
38	1	B15/GOE1	B^15	D14/GOE1	
39	0	CLK0/I	-	CLK0/I	
40	0	A0/GOE0	A^0	A0/GOE0	
41	0	A1	A^1	A2	

ispMACH 4032V/B/C and 4064V/B/C Logic Signal Connections: 44-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
42	0	A2	A^2	A4	
43	0	A3	A^3	A6	
44	0	A4	A^4	A8	

ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C		ispMACH 40	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
1	-	TDI	-	TDI	-	TDI	
2	0	A5	A^5	A10	A^5	A8	
3	0	A6	A^6	A12	A^6	A10	
4	0	A7	A^7	A14	A^7	A11	
5	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
6	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
7	0	A8	A^8	B0	B^0	B15	
8	0	A9	A^9	B2	B^1	B12	
9	0	A10	A^10	B4	B^2	B10	
10	0	A11	A^11	B6	B^6	B8	
11	-	TCK	-	TCK	-	TCK	
12	-	VCC	-	VCC	-	VCC	
13	-	GND	-	GND	-	GND	
14	0	A12	A^12	B8	B^4	B6	
15	0	A13	A^13	B10	B^5	B4	
16	0	A14	A^14	B12	B^6	B2	
17	0	A15	A^15	B14	B^7	B0	
18	0	CLK1/I	-	CLK1/I	-	CLK1/I	
19	1	CLK2/I	-	CLK2/I	-	CLK2/I	
20	1	B0	B^0	C0	C^0	C0	
21	1	B1	B^1	C2	C^1	C1	
22	1	B2	B^2	C4	C^2	C2	
23	1	B3	B^3	C6	C^3	C4	
24	1	B4	B^4	C8	C^4	C6	
25	-	TMS	-	TMS	-	TMS	
26	1	B5	B^5	C10	C^5	C8	
27	1	B6	B^6	C12	C^6	C10	
28	1	B7	B^7	C14	C^7	C11	
29	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
30	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
31	1	B8	B^8	D0	D^0	D15	
32	1	B9	B^9	D2	D^1	D12	

ispMACH 4032V/B/C/Z and 4064V/B/C/Z Logic Signal Connections: 48-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032V/B/C		ispMACH 4064V/B/C		ispMACH 40	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
33	1	B10	B^10	D4	D^2	D10	
34	1	B11	B^11	D6	D^3	D8	
35	-	TDO	-	TDO	-	TDO	
36	-	VCC	-	VCC	-	VCC	
37	-	GND	-	GND	-	GND	
38	1	B12	B^12	D8	D^4	D6	
39	1	B13	B^13	D10	D^5	D4	
40	1	B14	B^14	D12	D^6	D2	
41	1	B15/GOE1	B^15	D14/GOE1	D^7	D0/GOE1	
42	1	CLK3/I	-	CLK3/I	-	CLK3/I	
43	0	CLK0/I	-	CLK0/I	-	CLK0/I	
44	0	A0/GOE0	A^0	A0/GOE0	A^0	A0/GOE0	
45	0	A1	A^1	A2	A^1	A1	
46	0	A2	A^2	A4	A^2	A2	
47	0	A3	A^3	A6	A^3	A4	
48	0	A4	A^4	A8	A^4	A6	

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBG

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
B1	-	TDI	-	TDI	
C3	0	A5	A^5	A8	
C1	0	A6	A^6	A10	
D1	0	A7	A^7	A11	
D3	0	GND (Bank 0)	-	GND (Bank 0)	
E3	0	NC	-	A15/I	
E1	0	NC	-	I	
F3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
F1	0	A8	A^8	B15	
G3	0	A9	A^9	B12	
G1	0	A10	A^10	B10	
H1	0	A11	A^11	B8	
J1	0	NC	-	I	
K1	-	TCK	-	TCK	
K2	-	VCC	-	VCC	
H3	-	GND	-	GND	
K3	-			I	
K4	0	A12	A^12	B6	
H4	0	A13	A^13	B4	
H5	0	A14	A^14	B2	

ispMACH 4032Z and 4064Z Logic Signal Connections: 56-Ball csBGA

Ball Number	Bank Number	ispMACH 4032Z		ispMACH 4064Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
K5	0	A15	A^15	B0	
H6	0	CLK1/I	-	CLK1/I	
K6	1	CLK2/I	-	CLK2/I	
H7	1	B0	B^0	C0	
K7	1	B1	B^1	C1	
K8	1	B2	B^2	C2	
K9	1	B3	B^3	C4	
K10	1	B4	B^4	C6	
J10	-	TMS	-	TMS	
H8	1	B5	B^5	C8	
H10	1	B6	B^6	C10	
G10	1	B7	B^7	C11	
G8	1	GND (Bank 1)	-	GND (Bank 1)	
F8	1	NC	-	C12/I	
F10	1	NC	-	I	
E8	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
E10	1	B8	B^8	D15	
D8	1	B9	B^9	D12	
D10	1	B10	B^10	D10	
C10	1	B11	B^11	D8	
B10	1	NC	-	I	
A10	-	TDO	-	TDO	
A9	-	VCC	-	VCC	
C8	-	GND	-	GND	
A8	1	NC	-	I	
A7	1	B12	B^12	D6	
C7	1	B13	B^13	D4	
C6	1	B14	B^14	D2	
A6	1	B15/GOE1	B^15	D0/GOE1	
C5	1	CLK3/I	-	CLK3/I	
A5	0	CLK0/I	-	CLK0/I	
C4	0	A0/GOE0	A^0	A0/GOE0	
A4	0	A1	A^1	A1	
A3	0	A2	A^2	A2	
A2	0	A3	A^3	A4	
A1	0	A4	A^4	A6	

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C Logic Signal Connecti 100-Pin TQFP

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 42	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
1	-	GND	-	GND	-	GND	
2	-	TDI	-	TDI	-	TDI	
3	0	A8	A^8	B0	B^0	C12	
4	0	A9	A^9	B2	B^2	C10	
5	0	A10	A^10	B4	B^4	C6	
6	0	A11	A^11	B6	B^6	C2	
7	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
8	0	A12	A^12	B8	B^8	D12	
9	0	A13	A^13	B10	B^10	D10	
10	0	A14	A^14	B12	B^12	D6	
11	0	A15	A^15	B13	B^13	D4	
12*	0	I	-	I	-	I	
13	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
14	0	B15	B^15	C14	C^14	E4	
15	0	B14	B^14	C12	C^12	E6	
16	0	B13	B^13	C10	C^10	E10	
17	0	B12	B^12	C8	C^8	E12	
18	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
19	0	B11	B^11	C6	C^6	F2	
20	0	B10	B^10	C5	C^5	F6	
21	0	B9	B^9	C4	C^4	F10	
22	0	B8	B^8	C2	C^2	F12	
23*	0	I	-	I	-	I	
24	-	TCK	-	TCK	-	TCK	
25	-	VCC	-	VCC	-	VCC	
26	-	GND	-	GND	-	GND	
27*	0	I	-	I	-	I	
28	0	B7	B^7	D13	D^13	G12	
29	0	B6	B^6	D12	D^12	G10	
30	0	B5	B^5	D10	D^10	G6	
31	0	B4	B^4	D8	D^8	G2	
32	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
33	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
34	0	B3	B^3	D6	D^6	H12	
35	0	B2	B^2	D4	D^4	H10	
36	0	B1	B^1	D2	D^2	H6	
37	0	B0	B^0	D0	D^0	H2	
38	0	CLK1/I	-	CLK1/I	-	CLK1/I	
39	1	CLK2/I	-	CLK2/I	-	CLK2/I	
40	-	VCC	-	VCC	-	VCC	
41	1	C0	C^0	E0	E^0	I2	

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C Logic Signal Connecti 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 42	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
42	1	C1	C^1	E2	E^2	I6	
43	1	C2	C^2	E4	E^4	I10	
44	1	C3	C^3	E6	E^6	I12	
45	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
46	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
47	1	C4	C^4	E8	E^8	J2	
48	1	C5	C^5	E10	E^10	J6	
49	1	C6	C^6	E12	E^12	J10	
50	1	C7	C^7	E14	E^14	J12	
51	-	GND	-	GND	-	GND	
52	-	TMS	-	TMS	-	TMS	
53	1	C8	C^8	F0	F^0	K12	
54	1	C9	C^9	F2	F^2	K10	
55	1	C10	C^10	F4	F^4	K6	
56	1	C11	C^11	F6	F^6	K2	
57	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
58	1	C12	C^12	F8	F^8	L12	
59	1	C13	C^13	F10	F^10	L10	
60	1	C14	C^14	F12	F^12	L6	
61	1	C15	C^15	F13	F^13	L4	
62*	1	I	-	I	-	I	
63	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
64	1	D15	D^15	G14	G^14	M4	
65	1	D14	D^14	G12	G^12	M6	
66	1	D13	D^13	G10	G^10	M10	
67	1	D12	D^12	G8	G^8	M12	
68	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
69	1	D11	D^11	G6	G^6	N2	
70	1	D10	D^10	G5	G^5	N6	
71	1	D9	D^9	G4	G^4	N10	
72	1	D8	D^8	G2	G^2	N12	
73*	1	I	-	I	-	I	
74	-	TDO	-	TDO	-	TDO	
75	-	VCC	-	VCC	-	VCC	
76	-	GND	-	GND	-	GND	
77*	1	I	-	I	-	I	
78	1	D7	D^7	H13	H^13	O12	
79	1	D6	D^6	H12	H^12	O10	
80	1	D5	D^5	H10	H^10	O6	
81	1	D4	D^4	H8	H^8	O2	
82	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	

ispMACH 4064V/B/C/Z, 4128V/B/C/Z, 4256V/B/C Logic Signal Connecti 100-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4064V/B/C/Z		ispMACH 4128V/B/C/Z		ispMACH 42	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
83	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
84	1	D3	D^3	H6	H^6	P12	
85	1	D2	D^2	H4	H^4	P10	
86	1	D1	D^1	H2	H^2	P6	
87	1	D0/GOE1	D^0	H0/GOE1	H^0	P2/OE1	
88	1	CLK3/I	-	CLK3/I	-	CLK3/I	
89	0	CLK0/I	-	CLK0/I	-	CLK0/I	
90	-	VCC	-	VCC	-	VCC	
91	0	A0/GOE0	A^0	A0/GOE0	A^0	A2/GOE0	
92	0	A1	A^1	A2	A^2	A6	
93	0	A2	A^2	A4	A^4	A10	
94	0	A3	A^3	A6	A^6	A12	
95	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
96	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
97	0	A4	A^4	A8	A^8	B2	
98	0	A5	A^5	A10	A^10	B6	
99	0	A6	A^6	A12	A^12	B10	
100	0	A7	A^7	A14	A^14	B12	

*This pin is input only.

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
1	0	GND	-
2	0	TDI	-
3	0	VCCO (Bank 0)	-
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^4
8	0	B5	B^5
9	0	B6	B^6
10	0	GND (Bank 0)	-
11	0	B8	B^8
12	0	B9	B^9
13	0	B10	B^10
14	0	B12	B^12
15	0	B13	B^13
16	0	B14	B^14
17	0	VCCO (Bank 0)	-
18	0	C14	C^14

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
19	0	C13	C^13
20	0	C12	C^12
21	0	C10	C^10
22	0	C9	C^9
23	0	C8	C^8
24	0	GND (Bank 0)	-
25	0	C6	C^6
26	0	C5	C^5
27	0	C4	C^4
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	-
31	0	TCK	-
32	0	VCC	-
33	0	GND	-
34	0	D14	D^14
35	0	D13	D^13
36	0	D12	D^12
37	0	D10	D^10
38	0	D9	D^9
39	0	D8	D^8
40	0	GND (Bank 0)	-
41	0	VCCO (Bank 0)	-
42	0	D6	D^6
43	0	D5	D^5
44	0	D4	D^4
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	-
49	1	GND (Bank 1)	-
50	1	CLK2/I	-
51	1	VCC	-
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^4
56	1	E5	E^5
57	1	E6	E^6
58	1	VCCO (Bank 1)	-
59	1	GND (Bank 1)	-
60	1	E8	E^8
61	1	E9	E^9

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
62	1	E10	E^10
63	1	E12	E^12
64	1	E14	E^14
65	1	GND	-
66	1	TMS	-
67	1	VCCO (Bank 1)	-
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^4
72	1	F5	F^5
73	1	F6	F^6
74	1	GND (Bank 1)	-
75	1	F8	F^8
76	1	F9	F^9
77	1	F10	F^10
78	1	F12	F^12
79	1	F13	F^13
80	1	F14	F^14
81	1	VCCO (Bank 1)	-
82	1	G14	G^14
83	1	G13	G^13
84	1	G12	G^12
85	1	G10	G^10
86	1	G9	G^9
87	1	G8	G^8
88	1	GND (Bank 1)	-
89	1	G6	G^6
90	1	G5	G^5
91	1	G4	G^4
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	-
95	1	TDO	-
96	1	VCC	-
97	1	GND	-
98	1	H14	H^14
99	1	H13	H^13
100	1	H12	H^12
101	1	H10	H^10
102	1	H9	H^9
103	1	H8	H^8
104	1	GND (Bank 1)	-

ispMACH 4128V/B/C Logic Signal Connections: 128-Pin TQFP (Cont.

Pin Number	Bank Number	ispMACH 4128V/B/C	
		GLB/MC/Pad	ORP
105	1	VCCO (Bank 1)	-
106	1	H6	H^6
107	1	H5	H^5
108	1	H4	H^4
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	-
113	0	GND (Bank 0)	-
114	0	CLK0/I	-
115	0	VCC	-
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^4
120	0	A5	A^5
121	0	A6	A^6
122	0	VCCO (Bank 0)	-
123	0	GND (Bank 0)	-
124	0	A8	A^8
125	0	A9	A^9
126	0	A10	A^10
127	0	A12	A^12
128	0	A14	A^14

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
1	-	GND	-	GND	
2	-	TDI	-	TDI	
3	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
4	0	B0	B^0	C12	
5	0	B1	B^1	C10	
6	0	B2	B^2	C8	
7	0	B4	B^4	C6	
8	0	B5	B^5	C4	
9	0	B6	B^6	C2	
10	0	GND (Bank 0)	-	GND (Bank 0)	
11	0	B8	B^8	D14	
12	0	B9	B^9	D12	
13	0	B10	B^10	D10	

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
14	0	B12	B^12	D8	
15	0	B13	B^13	D6	
16	0	B14	B^14	D4	
17	-	NC[2]	-	I[2]	
18	0	GND (Bank 0)[1]	-	NC[1]	
19	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
20	0	NC[2]	-	I[2]	
21	0	C14	C^14	E2	
22	0	C13	C^13	E4	
23	0	C12	C^12	E6	
24	0	C10	C^10	E8	
25	0	C9	C^9	E10	
26	0	C8	C^8	E12	
27	0	GND (Bank 0)	-	GND (Bank 0)	
28	0	C6	C^6	F2	
29	0	C5	C^5	F4	
30	0	C4	C^4	F6	
31	0	C2	C^2	F8	
32	0	C1	C^1	F10	
33	0	C0	C^0	F12	
34	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
35	-	TCK	-	TCK	
36	-	VCC	-	VCC	
37	-	GND	-	GND	
38	-	NC[2]	-	I[2]	
39	0	D14	D^14	G12	
40	0	D13	D^13	G10	
41	0	D12	D^12	G8	
42	0	D10	D^10	G6	
43	0	D9	D^9	G4	
44	0	D8	D^8	G2	
45	-	NC[2]	-	I[2]	
46	0	GND (Bank 0)	-	GND (Bank 0)	
47	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
48	0	D6	D^6	H12	
49	0	D5	D^5	H10	
50	0	D4	D^4	H8	
51	0	D2	D^2	H6	
52	0	D1	D^1	H4	
53	0	D0	D^0	H2	
54	0	CLK1/I	-	CLK1/I	
55	1	GND (Bank 1)	-	GND (Bank 1)	
56	1	CLK2/I	-	CLK2/I	

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
57	-	VCC	-	VCC	
58	1	E0	E^0	I2	
59	1	E1	E^1	I4	
60	1	E2	E^2	I6	
61	1	E4	E^4	I8	
62	1	E5	E^5	I10	
63	1	E6	E^6	I12	
64	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
65	1	GND (Bank 1)	-	GND (Bank 1)	
66	1	E8	E^8	J2	
67	1	E9	E^9	J4	
68	1	E10	E^10	J6	
69	1	E12	E^12	J8	
70	1	E13	E^13	J10	
71	1	E14	E^14	J12	
72	-	NC[2]	-	I[2]	
73	-	GND	-	GND	
74	-	TMS	-	TMS	
75	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
76	1	F0	F^0	K12	
77	1	F1	F^1	K10	
78	1	F2	F^2	K8	
79	1	F4	F^4	K6	
80	1	F5	F^5	K4	
81	1	F6	F^6	K2	
82	1	GND (Bank 1)	-	GND (Bank 1)	
83	1	F8	F^8	L14	
84	1	F9	F^9	L12	
85	1	F10	F^10	L10	
86	1	F12	F^12	L8	
87	1	F13	F^13	L6	
88	1	F14	F^14	L4	
89	-	NC[2]	-	I[2]	
90	1	GND (Bank 1)[1]	-	NC[1]	
91	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
92	-	NC[2]	-	I[2]	
93	1	G14	G^14	M2	
94	1	G13	G^13	M4	
95	1	G12	G^12	M6	
96	1	G10	G^10	M8	
97	1	G9	G^9	M10	
98	1	G8	G^8	M12	
99	1	GND (Bank 1)	-	GND (Bank 1)	

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
100	1	G6	G^6	N2	
101	1	G5	G^5	N4	
102	1	G4	G^4	N6	
103	1	G2	G^2	N8	
104	1	G1	G^1	N10	
105	1	G0	G^0	N12	
106	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
107	-	TDO	-	TDO	
108	-	VCC	-	VCC	
109	-	GND	-	GND	
110	-	NC[2]	-	I[2]	
111	1	H14	H^14	O12	
112	1	H13	H^13	O10	
113	1	H12	H^12	O8	
114	1	H10	H^10	O6	
115	1	H9	H^9	O4	
116	1	H8	H^8	O2	
117	-	NC[2]	-	I[2]	
118	1	GND (Bank 1)	-	GND (Bank 1)	
119	1	VCCO (Bank 1)	-	VCCO (Bank 1)	
120	1	H6	H^6	P12	
121	1	H5	H^5	P10	
122	1	H4	H^4	P8	
123	1	H2	H^2	P6	
124	1	H1	H^1	P4	
125	1	H0/GOE1	H^0	P2/GOE1	
126	1	CLK3/I	-	CLK3/I	
127	0	GND (Bank 0)	-	GND (Bank 0)	
128	0	CLK0/I	-	CLK0/1	
129	-	VCC	-	VCC	
130	0	A0/GOE0	A^0	A2/GOE0	
131	0	A1	A^1	A4	
132	0	A2	A^2	A6	
133	0	A4	A^4	A8	
134	0	A5	A^5	A10	
135	0	A6	A^6	A12	
136	0	VCCO (Bank 0)	-	VCCO (Bank 0)	
137	0	GND (Bank 0)	-	GND (Bank 0)	
138	0	A8	A^8	B2	
139	0	A9	A^9	B4	
140	0	A10	A^10	B6	
141	0	A12	A^12	B8	
142	0	A13	A^13	B10	

ispMACH 4128V and 4256V Logic Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	ispMACH 4128V		ispMACH 4256V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	
143	0	A14	A^14	B12	
144	-	NC[2]	-	I[2]	

1. For device migration considerations, these NC pins are GND pins for I/O banks in ispMACH 4128V devices.
2. For device migration considerations, these NC pins are input signal pins in ispMACH 4256V devices.

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C, Logic Signal Connectio 176-Pin TQFP

Pin Number	Bank Number	ispMACH 4256V/B/C		ispMACH 4384V/B/C		ispMACH 45	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
1	-	NC	-	NC	-	NC	
2	-	GND	-	GND	-	GND	
3	-	TDI	-	TDI	-	TDI	
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
5	0	C14	C^7	C14	C^7	C14	
6	0	C12	C^6	C12	C^6	C12	
7	0	C10	C^5	C10	C^5	C10	
8	0	C8	C^4	C8	C^4	C8	
9	0	C6	C^3	C6	C^3	C6	
10	0	C4	C^2	C4	C^2	C4	
11	0	C2	C^1	C2	C^1	C2	
12	0	C0	C^0	C0	C^0	C0	
13	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
14	0	D14	D^7	E14	E^7	G14	
15	0	D12	D^6	E12	E^6	G12	
16	0	D10	D^5	E10	E^5	G10	
17	0	D8	D^4	E8	E^4	G8	
18	0	D6	D^3	E6	E^3	G6	
19	0	D4	D^2	E4	E^2	G4	
20	0	D2	D^1	E2	E^1	G2	
21	0	D0	D^0	E0	E^0	G0	
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
23	0	E0	E^0	H0	H^0	J0	
24	0	E2	E^1	H2	H^1	J2	
25	0	E4	E^2	H4	H^2	J4	
26	0	E6	E^3	H6	H^3	J6	
27	0	E8	E^4	H8	H^4	J8	
28	0	E10	E^5	H10	H^5	J10	
29	0	E12	E^6	H12	H^6	J12	
30	0	E14	E^7	H14	H^7	J14	
31	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
32	0	F0	F^0	J0	J^0	N0	

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C, Logic Signal Connectio 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C		ispMACH 4384V/B/C		ispMACH 45	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
33	0	F2	F^1	J2	J^1	N2	
34	0	F4	F^2	J4	J^2	N4	
35	0	F6	F^3	J6	J^3	N6	
36	0	F8	F^4	J8	J^4	N8	
37	0	F10	F^5	J10	J^5	N10	
38	0	F12	F^6	J12	J^6	N12	
39	0	F14	F^7	J14	J^7	N14	
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
41	-	TCK	-	TCK	-	TCK	
42	-	VCC	-	VCC	-	VCC	
43	-	NC	-	NC	-	NC	
44	-	NC	-	NC	-	NC	
45	-	NC	-	NC	-	NC	
46	-	GND	-	GND (Bank 0)	-	GND	
47	0	G14	G^7	K14	K^7	O14	
48	0	G12	G^6	K12	K^6	O12	
49	0	G10	G^5	K10	K^5	O10	
50	0	G8	G^4	K8	K^4	O8	
51	0	G6	G^3	K6	K^3	O6	
52	0	G4	G^2	K4	K^2	O4	
53	0	G2	G^1	K2	K^1	O2	
54	0	G0	G^0	K0	K^0	O0	
55	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
57	0	H14	H^7	L14	L^7	P14	
58	0	H12	H^6	L12	L^6	P12	
59	0	H10	H^5	L10	L^5	P10	
60	0	H8	H^4	L8	L^4	P8	
61	0	H6	H^3	L6	L^3	P6	
62	0	H4	H^2	L4	L^2	P4	
63	0	H2	H^1	L2	L^1	P2	
64	0	H0	H^0	L0	L^0	P0	
65	-	GND	-	GND	-	GND	
66	0	CLK1/I	-	CLK1/I	-	CLK1/I	
67	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
68	1	CLK2/I	-	CLK2/I	-	CLK2/I	
69	-	VCC	-	VCC	-	VCC	
70	1	I0	I^0	M0	M^0	AX0	
71	1	I2	I^1	M2	M^1	AX2	
72	1	I4	I^2	M4	M^2	AX4	
73	1	I6	I^3	M6	M^3	AX6	

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C, Logic Signal Connectio 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C		ispMACH 4384V/B/C		ispMACH 45	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
74	1	I8	I^4	M8	M^4	AX8	
75	1	I10	I^5	M10	M^5	AX10	
76	1	I12	I^6	M12	M^6	AX12	
77	1	I14	I^7	M14	M^7	AX14	
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
79	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
80	1	J0	J^0	N0	N^0	BX0	
81	1	J2	J^1	N2	N^1	BX2	
82	1	J4	J^2	N4	N^2	BX4	
83	1	J6	J^3	N6	N^3	BX6	
84	1	J8	J^4	N8	N^4	BX8	
85	1	J10	J^5	N10	N^5	BX10	
86	1	J12	J^6	N12	N^6	BX12	
87	1	J14	J^7	N14	N^7	BX14	
88	-	VCC	-	VCC	-	VCC	
89	-	NC	-	NC	-	NC	
90	-	GND	-	GND	-	GND	
91	-	TMS	-	TMS	-	TMS	
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
93	1	K14	K^7	O14	O^7	CX14	
94	1	K12	K^6	O12	O^6	CX12	
95	1	K10	K^5	O10	O^5	CX10	
96	1	K8	K^4	O8	O^4	CX8	
97	1	K6	K^3	O6	O^3	CX6	
98	1	K4	K^2	O4	O^2	CX4	
99	1	K2	K^1	O2	O^1	CX2	
100	1	K0	K^0	O0	O^0	CX0	
101	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
102	1	L14	L^7	AX14	AX^7	GX14	
103	1	L12	L^6	AX12	AX^6	GX12	
104	1	L10	L^5	AX10	AX^5	GX10	
105	1	L8	L^4	AX8	AX^4	GX8	
106	1	L6	L^3	AX6	AX^3	GX6	
107	1	L4	L^2	AX4	AX^2	GX4	
108	1	L2	L^1	AX2	AX^1	GX2	
109	1	L0	L^0	AX0	AX^0	GX0	
110	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
111	1	M0	M^0	DX0	DX^0	JX0	
112	1	M2	M^1	DX2	DX^1	JX2	
113	1	M4	M^2	DX4	DX^2	JX4	
114	1	M6	M^3	DX6	DX^3	JX6	

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C, Logic Signal Connectio 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C		ispMACH 4384V/B/C		ispMACH 45	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
115	1	M8	M^4	DX8	DX^4	JX8	
116	1	M10	M^5	DX10	DX^5	JX10	
117	1	M12	M^6	DX12	DX^6	JX12	
118	1	M14	M^7	DX14	DX^7	JX14	
119	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
120	1	N0	N^0	FX0	FX^0	NX0	
121	1	N2	N^1	FX2	FX^1	NX2	
122	1	N4	N^2	FX4	FX^2	NX4	
123	1	N6	N^3	FX6	FX^3	NX6	
124	1	N8	N^4	FX8	FX^4	NX8	
125	1	N10	N^5	FX10	FX^5	NX10	
126	1	N12	N^6	FX12	FX^6	NX12	
127	1	N14	N^7	FX14	FX^7	NX14	
128	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
129	-	TDO	-	TDO	-	TDO	
130	-	VCC	-	VCC	-	VCC	
131	-	NC	-	NC	-	NC	
132	-	NC	-	NC	-	NC	
133	-	NC	-	NC	-	NC	
134	-	GND	-	GND	-	GND	
135	1	O14	O^7	GX14	GX^7	OX14	
136	1	O12	O^6	GX12	GX^6	OX12	
137	1	O10	O^5	GX10	GX^5	OX10	
138	1	O8	O^4	GX8	GX^4	OX8	
139	1	O6	O^3	GX6	GX^3	OX6	
140	1	O4	O^2	GX4	GX^2	OX4	
141	1	O2	O^1	GX2	GX^1	OX2	
142	1	O0	O^0	GX0	GX^0	OX0	
143	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	
145	1	P14	P^7	HX14	HX^7	PX14	
146	1	P12	P^6	HX12	HX^6	PX12	
147	1	P10	P^5	HX10	HX^5	PX10	
148	1	P8	P^4	HX8	HX^4	PX8	
149	1	P6	P^3	HX6	HX^3	PX6	
150	1	P4	P^2	HX4	HX^2	PX4	
151	1	P2/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE1	
152	1	P0	P^0	HX0	HX^0	PX0	
153	-	GND	-	GND	-	GND	
154	1	CLK3/I	-	CLK3/I	-	CLK3/I	
155	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C, Logic Signal Connectio 176-Pin TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256V/B/C		ispMACH 4384V/B/C		ispMACH 45	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	
156	0	CLK0/I	-	CLK0/I	-	CLK0/I	
157	-	VCC	-	VCC	-	VCC	
158	0	A0	A^0	A0	A^0	A0	
159	0	A2/GOE0	A^1	A2/GOE0	A^1	A2//GOE0	
160	0	A4	A^2	A4	A^2	A4	
161	0	A6	A^3	A6	A^3	A6	
162	0	A8	A^4	A8	A^4	A8	
163	0	A10	A^5	A10	A^5	A10	
164	0	A12	A^6	A12	A^6	A12	
165	0	A14	A^7	A14	A^7	A14	
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	
167	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	
168	0	B0	B^0	B0	B^0	B0	
169	0	B2	B^1	B2	B^1	B2	
170	0	B4	B^2	B4	B^2	B4	
171	0	B6	B^3	B6	B^3	B6	
172	0	B8	B^4	B8	B^4	B8	
173	0	B10	B^5	B10	B^5	B10	
174	0	B12	B^6	B12	B^6	B12	
175	0	B14	B^7	B14	B^7	B14	
176	-	VCC	-	VCC	-	VCC	

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connectio 256-Ball fpBGA

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
-	-	-	-	-	-	VCC	-	VCC
-	-	GND	-	GND	-	GND	-	GND
C3	-	TDI	-	TDI	-	TDI	-	TDI
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
B1	0	C14	C^7	C9	C^9	C14	C^7	C14
F5	0	C12	C^6	C8	C^8	C12	C^6	C12
D3	0	C10	C^5	C7	C^7	C10	C^5	C10
C1	0	C8	C^4	C6	C^6	C8	C^4	C8
C2	0	C6	C^3	C5	C^5	C6	C^3	C6
E3	0	C4	C^2	C4	C^4	C4	C^2	C4
D2	0	C2	C^1	C3	C^3	C2	C^1	C2
F6	0	C0	C^0	C2	C^2	C0	C^0	C0
D1	0	NC	-	C1	C^1	F6	F^3	H0

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection
256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
E2	0	NC	-	C0	C^0	F4	F^2	H4
E4	0	NC	-	NC	-	D6	D^3	F4
G5	0	NC	-	NC	-	D4	D^2	F6
E1	0	NC	-	NC	-	NC	-	F8
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
F2	0	NC	-	NC	-	NC	-	F10
F1	0	NC	-	NC	-	D2	D^1	F12
G1	0	NC	-	NC	-	D0	D^0	F14
G6	0	NC	-	D9	D^9	F2	F^1	H8
G4	0	NC	-	D8	D^8	F0	F^0	H12
H6	0	D14	D^7	D7	D^7	E14	E^7	G14
G3	0	D12	D^6	D6	D^6	E12	E^6	G12
H5	0	D10	D^5	D5	D^5	E10	E^5	G10
G2	0	D8	D^4	D4	D^4	E8	E^4	G8
H1	0	D6	D^3	D3	D^3	E6	E^3	G6
H2	0	D4	D^2	D2	D^2	E4	E^2	G4
H3	0	D2	D^1	D1	D^1	E2	E^1	G2
H4	0	D0	D^0	D0	D^0	E0	E^0	G0
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
J4	0	E0	E^0	E0	E^0	H0	H^0	J0
J3	0	E2	E^1	E1	E^1	H2	H^1	J2
J2	0	E4	E^2	E2	E^2	H4	H^2	J4
J1	0	E6	E^3	E3	E^3	H6	H^3	J6
K1	0	E8	E^4	E4	E^4	H8	H^4	J8
J5	0	E10	E^5	E5	E^5	H10	H^5	J10
K2	0	E12	E^6	E6	E^6	H12	H^6	J12
J6	0	E14	E^7	E7	E^7	H14	H^7	J14
K3	0	NC	-	E8	E^8	G0	G^0	I0
K4	0	NC	-	E9	E^9	G2	G^1	I4
L1	0	NC	-	NC	-	I14	I^7	K0
L2	0	NC	-	NC	-	I12	I^6	K2
M1	0	NC	-	NC	-	NC	-	K4
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
-	0	-	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
M2	0	NC	-	NC	-	NC	-	K6
N1	0	NC	-	NC	-	I10	I^5	K8
M3	0	NC	-	NC	-	I8	I^4	K10
M4	0	NC	-	F0	F^0	G4	G^2	I8
N2	0	NC	-	F1	F^1	G6	G^3	I12

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection
256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
K5	0	F0	F^0	F2	F^2	J0	J^0	N0
P1	0	F2	F^1	F3	F^3	J2	J^1	N2
K6	0	F4	F^2	F4	F^4	J4	J^2	N4
N3	0	F6	F^3	F5	F^5	J6	J^3	N6
L5	0	F8	F^4	F6	F^6	J8	J^4	N8
P2	0	F10	F^5	F7	F^7	J10	J^5	N10
L6	0	F12	F^6	F8	F^8	J12	J^6	N12
R1	0	F14	F^7	F9	F^9	J14	J^7	N14
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
P3	-	TCK	-	TCK	-	TCK	-	TCK
-	-	VCC	-	VCC	-	VCC	-	VCC
-	-	GND	-	GND	-	GND	-	GND
-	0	-	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
T2	0	NC	-	G9	G^9	I6	I^3	K12
M5	0	NC	-	G8	G^8	I4	I^2	K14
N4	0	G14	G^7	G7	G^7	K14	K^7	O14
T3	0	G12	G^6	G6	G^6	K12	K^6	O12
R3	0	G10	G^5	G5	G^5	K10	K^5	O10
M6	0	G8	G^4	G4	G^4	K8	K^4	O8
P4	0	G6	G^3	G3	G^3	K6	K^3	O6
L7	0	G4	G^2	G2	G^2	K4	K^2	O4
N5	0	G2	G^1	G1	G^1	K2	K^1	O2
M7	0	G0	G^0	G0	G^0	K0	K^0	O0
P5	0	NC	-	NC	-	G8	G^4	M0
R4	0	NC	-	NC	-	G10	G^5	M4
T4	0	NC	-	NC	-	NC	-	L0
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
R5	0	NC	-	NC	-	NC	-	L4
T5	0	NC	-	NC	-	I2	I^1	L8
R6	0	NC	-	NC	-	I0	I^0	L12
T6	0	NC	-	H9	H^9	G12	G^6	M8
N7	0	NC	-	H8	H^8	G14	G^7	M12
P7	0	H14	H^7	H7	H^7	L14	L^7	P14
R7	0	H12	H^6	H6	H^6	L12	L^6	P12
L8	0	H10	H^5	H5	H^5	L10	L^5	P10
T7	0	H8	H^4	H4	H^4	L8	L^4	P8
M8	0	H6	H^3	H3	H^3	L6	L^3	P6
N8	0	H4	H^2	H2	H^2	L4	L^2	P4
R8	0	H2	H^1	H1	H^1	L2	L^1	P2
P8	0	H0	H^0	H0	H^0	L0	L^0	P0

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection 256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
-	-	GND	-	GND	-	GND	-	GND
T8	0	CLK1/I	-	CLK1/I	-	CLK1/I	-	CLK1/I
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
N9	1	CLK2/I	-	CLK2/I	-	CLK2/I	-	CLK2/I
-	-	VCC	-	VCC	-	VCC	-	VCC
P9	1	I0	I^0	I0	I^0	M0	M^0	AX0
R9	1	I2	I^1	I1	I^1	M2	M^1	AX2
T9	1	I4	I^2	I2	I^2	M4	M^2	AX4
T10	1	I6	I^3	I3	I^3	M6	M^3	AX6
R10	1	I8	I^4	I4	I^4	M8	M^4	AX8
M9	1	I10	I^5	I5	I^5	M10	M^5	AX10
P10	1	I12	I^6	I6	I^6	M12	M^6	AX12
L9	1	I14	I^7	I7	I^7	M14	M^7	AX14
N10	1	NC	-	I8	I^8	BX14	BX^7	DX0
T11	1	NC	-	I9	I^9	BX12	BX^6	DX4
R11	1	NC	-	NC	-	P0	P^0	EX0
T12	1	NC	-	NC	-	P2	P^1	EX4
N12	1	NC	-	NC	-	NC	-	EX8
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
R12	1	NC	-	NC	-	NC	-	EX12
T13	1	NC	-	J0	J^0	BX10	BX^5	DX8
P12	1	NC	-	J1	J^1	BX8	BX^4	DX12
M10	1	J0	J^0	J2	J^2	N0	N^0	BX0
R13	1	J2	J^1	J3	J^3	N2	N^1	BX2
L10	1	J4	J^2	J4	J^4	N4	N^2	BX4
T14	1	J6	J^3	J5	J^5	N6	N^3	BX6
M11	1	J8	J^4	J6	J^6	N8	N^4	BX8
R14	1	J10	J^5	J7	J^7	N10	N^5	BX10
P13	1	J12	J^6	J8	J^8	N12	N^6	BX12
N13	1	J14	J^7	J9	J^9	N14	N^7	BX14
M12	1	NC	-	NC	-	P4	P^2	FX0
T15	1	NC	-	NC	-	P6	P^3	FX2
-	-	VCC	-	VCC	-	VCC	-	VCC
-	-	GND	-	GND	-	GND	-	GND
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
P14	-	TMS	-	TMS	-	TMS	-	TMS
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
L12	1	NC	-	NC	-	NC	-	FX4
R16	1	NC	-	NC	-	P8	P^4	FX6
N14	1	NC	-	NC	-	P10	P^5	FX8

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection 256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
P15	1	K14	K^7	K9	K^9	O14	O^7	CX14
L11	1	K12	K^6	K8	K^8	O12	O^6	CX12
P16	1	K10	K^5	K7	K^7	O10	O^5	CX10
K11	1	K8	K^4	K6	K^6	O8	O^4	CX8
M14	1	K6	K^3	K5	K^5	O6	O^3	CX6
K12	1	K4	K^2	K4	K^4	O4	O^2	CX4
N15	1	K2	K^1	K3	K^3	O2	O^1	CX2
N16	1	K0	K^0	K2	K^2	O0	O^0	CX0
M15	1	NC	-	K1	K^1	BX6	BX^3	HX0
M13	1	NC	-	K0	K^0	BX4	BX^2	HX4
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
M16	1	NC	-	NC	-	NC	-	FX10
L15	1	NC	-	NC	-	P12	P^6	FX12
L16	1	NC	-	NC	-	P14	P^7	FX14
J11	1	NC	-	L9	L^9	BX2	BX^1	HX8
K15	1	NC	-	L8	L^8	BX0	BX^0	HX12
J12	1	L14	L^7	L7	L^7	AX14	AX^7	GX14
K13	1	L12	L^6	L6	L^6	AX12	AX^6	GX12
K14	1	L10	L^5	L5	L^5	AX10	AX^5	GX10
K16	1	L8	L^4	L4	L^4	AX8	AX^4	GX8
J16	1	L6	L^3	L3	L^3	AX6	AX^3	GX6
J15	1	L4	L^2	L2	L^2	AX4	AX^2	GX4
H16	1	L2	L^1	L1	L^1	AX2	AX^1	GX2
J13	1	L0	L^0	L0	L^0	AX0	AX^0	GX0
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
J14	1	M0	M^0	M0	M^0	DX0	DX^0	JX0
H15	1	M2	M^1	M1	M^1	DX2	DX^1	JX2
H14	1	M4	M^2	M2	M^2	DX4	DX^2	JX4
H13	1	M6	M^3	M3	M^3	DX6	DX^3	JX6
G16	1	M8	M^4	M4	M^4	DX8	DX^4	JX8
H12	1	M10	M^5	M5	M^5	DX10	DX^5	JX10
G15	1	M12	M^6	M6	M^6	DX12	DX^6	JX12
H11	1	M14	M^7	M7	M^7	DX14	DX^7	JX14
F16	1	NC	-	M8	M^8	CX0	CX^0	IX0
G13	1	NC	-	M9	M^9	CX2	CX^1	IX4
G14	1	NC	-	NC	-	EX14	EX^7	KX0
F15	1	NC	-	NC	-	EX12	EX^6	KX2
E16	1	NC	-	NC	-	NC	-	KX4
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection 256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
-	1	-	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
E15	1	NC	-	NC	-	NC	-	KX6
G12	1	NC	-	NC	-	EX10	EX^5	KX8
E13	1	NC	-	NC	-	EX8	EX^4	KX10
D16	1	NC	-	N0	N^0	CX4	CX^2	IX8
E14	1	NC	-	N1	N^1	CX6	CX^3	IX12
G11	1	N0	N^0	N2	N^2	FX0	FX^0	NX0
D15	1	N2	N^1	N3	N^3	FX2	FX^1	NX2
F11	1	N4	N^2	N4	N^4	FX4	FX^2	NX4
C16	1	N6	N^3	N5	N^5	FX6	FX^3	NX6
F12	1	N8	N^4	N6	N^6	FX8	FX^4	NX8
D14	1	N10	N^5	N7	N^7	FX10	FX^5	NX10
C15	1	N12	N^6	N8	N^8	FX12	FX^6	NX12
B16	1	N14	N^7	N9	N^9	FX14	FX^7	NX14
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
C14	-	TDO	-	TDO	-	TDO	-	TDO
-	-	VCC	-	VCC	-	VCC	-	VCC
-	-	GND	-	GND	-	GND	-	GND
-	1	-	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
A15	1	NC	-	NC	-	EX6	EX^3	KX12
B14	1	NC	-	NC	-	EX4	EX^2	KX14
E12	1	O14	O^7	O9	O^9	GX14	GX^7	OX14
A14	1	O12	O^6	O8	O^8	GX12	GX^6	OX12
C13	1	O10	O^5	O7	O^7	GX10	GX^5	OX10
D13	1	O8	O^4	O6	O^6	GX8	GX^4	OX8
E11	1	O6	O^3	O5	O^5	GX6	GX^3	OX6
B13	1	O4	O^2	O4	O^4	GX4	GX^2	OX4
F10	1	O2	O^1	O3	O^3	GX2	GX^1	OX2
C12	1	O0	O^0	O2	O^2	GX0	GX^0	OX0
E10	1	NC	-	O1	O^1	CX8	CX^4	MX0
A13	1	NC	-	O0	O^0	CX10	CX^5	MX4
D12	1	NC	-	NC	-	NC	-	LX0
-	1	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank 1)	-	GND (Bank
-	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Bank 1)	-	VCCO (Ban
B12	1	NC	-	NC	-	NC	-	LX4
A12	1	NC	-	NC	-	EX2	EX^1	LX8
B11	1	NC	-	NC	-	EX0	EX^0	LX12
A11	1	NC	-	P9	P^9	CX12	CX^6	MX8
D10	1	NC	-	P8	P^8	CX14	CX^7	MX12
C10	1	P14	P^7	P7	P^7	HX14	HX^7	PX14
B10	1	P12	P^6	P6	P6	HX12	HX^6	PX12

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connection 256-Ball fpBGA (Cont.)

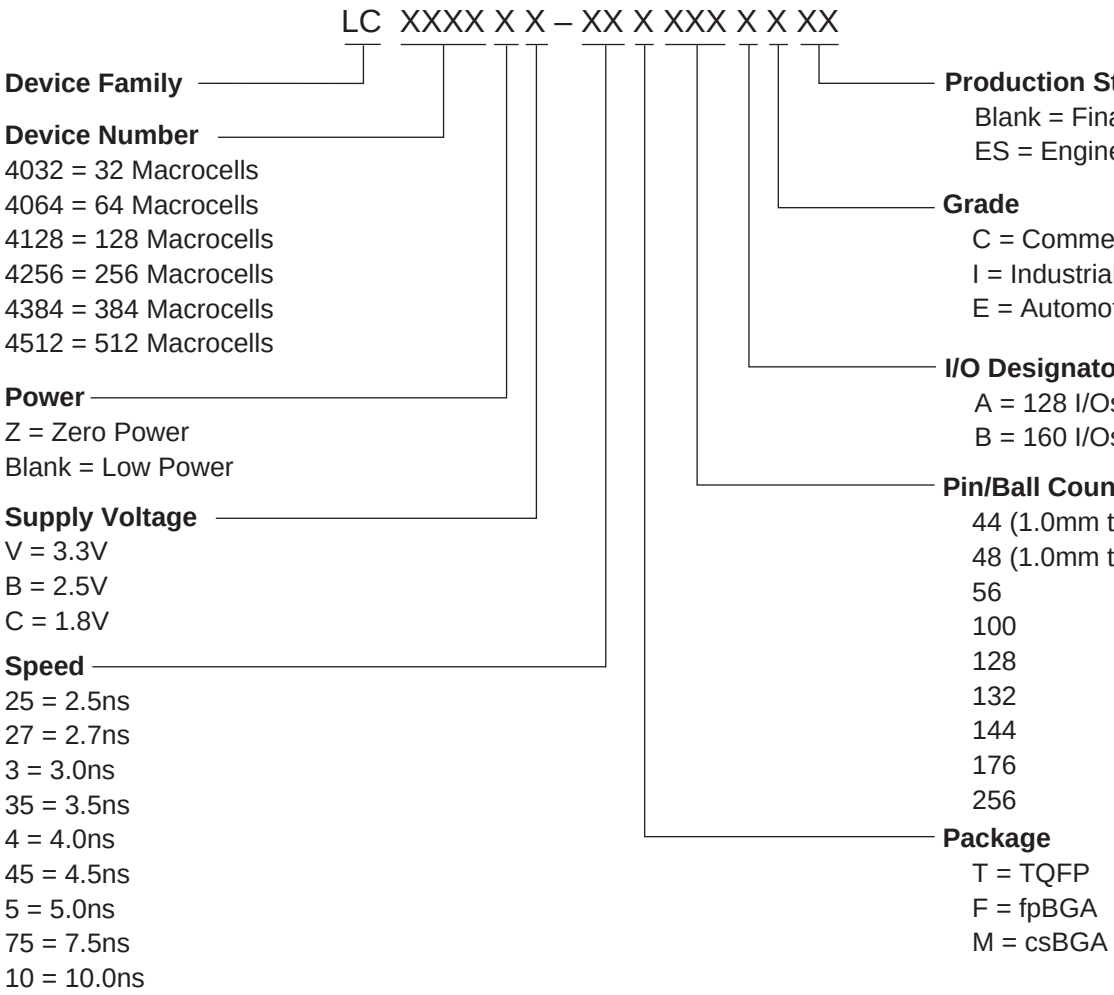
Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
A10	1	P10	P^5	P5	P^5	HX10	HX^5	PX10
A9	1	P8	P^4	P4	P^4	HX8	HX^4	PX8
F9	1	P6	P^3	P3	P^3	HX6	HX^3	PX6
B9	1	P4	P^2	P2	P^2	HX4	HX^2	PX4
E9	1	P2/GOE1	P^1	P1/GOE1	P^1	HX2/GOE1	HX^1	PX2/GOE
C9	1	P0	P^0	P0	P^0	HX0	HX^0	PX0
-	-	GND	-	GND		GND	-	GND
D9	1	CLK3/I	-	CLK3/I	-	CLK3/I	-	CLK3/I
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
B8	0	CLK0/I	-	CLK0/I	-	CLK0/I	-	CLK0/I
-	-	VCC	-	VCC	-	VCC	-	VCC
D8	0	A0	A^0	A0	A^0	A0	A^0	A0
C8	0	A2/GOE0	A^1	A1/GOE0	A^1	A2/GOE0	A^1	A2/GOE
A8	0	A4	A^2	A2	A^2	A4	A^2	A4
A7	0	A6	A^3	A3	A^3	A6	A^3	A6
B7	0	A8	A^4	A4	A^4	A8	A^4	A8
E8	0	A10	A^5	A5	A^5	A10	A^5	A10
D7	0	A12	A^6	A6	A^6	A12	A^6	A12
F8	0	A14	A^7	A7	A^7	A14	A^7	A14
C7	0	NC	-	A8	A^8	F14	F^7	D0
A6	0	NC	-	A9	A^9	F12	F^6	D4
B6	0	NC	-	NC	-	D14	D^7	E0
A5	0	NC	-	NC	-	D12	D^6	E4
B5	0	NC	-	NC	-	NC	-	E8
-	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Bank 0)	-	VCCO (Ban
-	0	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank 0)	-	GND (Bank
D5	0	NC	-	NC	-	NC	-	E12
A4	0	NC	-	B0	B^0	F10	F^5	D8
E7	0	NC	-	B1	B^1	F8	F^4	D12
A3	0	B0	B^0	B2	B^2	B0	B^0	B0
F7	0	B2	B^1	B3	B^3	B2	B^1	B2
B4	0	B4	B^2	B4	B^4	B4	B^2	B4
C5	0	B6	B^3	B5	B^5	B6	B^3	B6
A2	0	B8	B^4	B6	B^6	B8	B^4	B8
E6	0	B10	B^5	B7	B^7	B10	B^5	B10
B3	0	B12	B^6	B8	B^8	B12	B^6	B12
C4	0	B14	B^7	B9	B^9	B14	B^7	B14
D4	0	NC	-	NC	-	D10	D^5	F0
E5	0	NC	-	NC	-	D8	D^4	F2
-	-	VCC	-	VCC	-	VCC	-	VCC
-	-	-	-	-	-	GND	-	GND

ispMACH 4256V/B/C, 4384V/B/C, 4512V/B/C Logic Signal Connectior 256-Ball fpBGA (Cont.)

Ball Number	I/O Bank	ispMACH 4256V/B/C 128-I/O		ispMACH 4256V/B/C 160-I/O		ispMACH 4384V/B/C		ispMACH
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/Pad	ORP	GLB/MC/P
-	0	-	-	-	-	GND (Bank 0)	-	GND (Bank

Note: VCC, VCCO and GND are tied together to their respective common signal on the package substrate. See Power Supply a nections table for VCC/ VCCO/GND pin definitions.

Part Number Description



Ordering Information

Note: ispMACH 4000 devices are all dual marked except the slowest commercial speed grade ispM devices. For example, the commercial speed grade LC4128C-5T100C is also marked with the industria The commercial grade is always one speed grade faster than the associated dual mark industrial grad est commercial speed grade ispMACH 4000Z devices are marked as commercial grade only.

ispMACH 4000C (1.8V) Commercial Devices[1]

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O
LC4032C	LC4032C-25T48C	32	1.8	2.5	TQFP	48	32
	LC4032C-5T48C	32	1.8	5	TQFP	48	32
	LC4032C-75T48C	32	1.8	7.5	TQFP	48	32
	LC4032C-25T44C	32	1.8	2.5	TQFP	44	30
	LC4032C-5T44C	32	1.8	5	TQFP	44	30
	LC4032C-75T44C	32	1.8	7.5	TQFP	44	30

ispMACH 4000C (1.8V) Commercial Devices[1] (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4064C	LC4064C-25T100C	64	1.8	2.5	TQFP	100	64
	LC4064C-5T100C	64	1.8	5	TQFP	100	64
	LC4064C-75T100C	64	1.8	7.5	TQFP	100	64
	LC4064C-25T48C	64	1.8	2.5	TQFP	48	32
	LC4064C-5T48C	64	1.8	5	TQFP	48	32
	LC4064C-75T48C	64	1.8	7.5	TQFP	48	32
	LC4064C-25T44C	64	1.8	2.5	TQFP	44	30
	LC4064C-5T44C	64	1.8	5	TQFP	44	30
	LC4064C-75T44C	64	1.8	7.5	TQFP	44	30
LC4128C	LC4128C-27T128C	128	1.8	2.7	TQFP	128	92
	LC4128C-5T128C	128	1.8	5	TQFP	128	92
	LC4128C-75T128C	128	1.8	7.5	TQFP	128	92
	LC4128C-27T100C	128	1.8	2.7	TQFP	100	64
	LC4128C-5T100C	128	1.8	5	TQFP	100	64
	LC4128C-75T100C	128	1.8	7.5	TQFP	100	64
LC4256C	LC4256C-3F256AC	256	1.8	3	fpBGA	256	128
	LC4256C-5F256AC	256	1.8	5	fpBGA	256	128
	LC4256C-75F256AC	256	1.8	7.5	fpBGA	256	128
	LC4256C-3F256BC	256	1.8	3	fpBGA	256	160
	LC4256C-5F256BC	256	1.8	5	fpBGA	256	160
	LC4256C-75F256BC	256	1.8	7.5	fpBGA	256	160
	LC4256C-3T176C	256	1.8	3	TQFP	176	128
	LC4256C-5T176C	256	1.8	5	TQFP	176	128
	LC4256C-75T176C	256	1.8	7.5	TQFP	176	128
	LC4256C-3T100C	256	1.8	3	TQFP	100	64
	LC4256C-5T100C	256	1.8	5	TQFP	100	64
	LC4256C-75T100C	256	1.8	7.5	TQFP	100	64
LC4384C	LC4384C-35F256C	384	1.8	3.5	fpBGA	256	192
	LC4384C-5F256C	384	1.8	5	fpBGA	256	192
	LC4384C-75F256C	384	1.8	7.5	fpBGA	256	192
	LC4384C-35T176C	384	1.8	3.5	TQFP	176	128
	LC4384C-5T176C	384	1.8	5	TQFP	176	128
	LC4384C-75T176C	384	1.8	7.5	TQFP	176	128
LC4512C	LC4512C-35F256C	512	1.8	3.5	fpBGA	256	208
	LC4512C-5F256C	512	1.8	5	fpBGA	256	208
	LC4512C-75F256C	512	1.8	7.5	fpBGA	256	208
	LC4512C-35T176C	512	1.8	3.5	TQFP	176	128
	LC4512C-5T176C	512	1.8	5	TQFP	176	128
	LC4512C-75T176C	512	1.8	7.5	TQFP	176	128

ispMACH 4000B (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4032B	LC4032B-25T48C	32	2.5	2.5	TQFP	48	32
	LC4032B-5T48C	32	2.5	5	TQFP	48	32
	LC4032B-75T48C	32	2.5	7.5	TQFP	48	32
	LC4032B-25T44C	32	2.5	2.5	TQFP	44	30
	LC4032B-5T44C	32	2.5	5	TQFP	44	30
	LC4032B-75T44C	32	2.5	7.5	TQFP	44	30
LC4064B	LC4064B-25T100C	64	2.5	2.5	TQFP	100	64
	LC4064B-5T100C	64	2.5	5	TQFP	100	64
	LC4064B-75T100C	64	2.5	7.5	TQFP	100	64
	LC4064B-25T48C	64	2.5	2.5	TQFP	48	32
	LC4064B-5T48C	64	2.5	5	TQFP	48	32
	LC4064B-75T48C	64	2.5	7.5	TQFP	48	32
	LC4064B-25T44C	64	2.5	2.5	TQFP	44	30
	LC4064B-5T44C	64	2.5	5	TQFP	44	30
	LC4064B-75T44C	64	2.5	7.5	TQFP	44	30
LC4128B	LC4128B-27T128C	128	2.5	2.7	TQFP	128	92
	LC4128B-5T128C	128	2.5	5	TQFP	128	92
	LC4128B-75T128C	128	2.5	7.5	TQFP	128	92
	LC4128B-27T100C	128	2.5	2.7	TQFP	100	64
	LC4128B-5T100C	128	2.5	5	TQFP	100	64
	LC4128B-75T100C	128	2.5	7.5	TQFP	100	64
LC4256B	LC4256B-3F256AC	256	2.5	3	fpBGA	256	128
	LC4256B-5F256AC	256	2.5	5	fpBGA	256	128
	LC4256B-75F256AC	256	2.5	7.5	fpBGA	256	128
	LC4256B-3F256BC	256	2.5	3	fpBGA	256	160
	LC4256B-5F256BC	256	2.5	5	fpBGA	256	160
	LC4256B-75F256BC	256	2.5	7.5	fpBGA	256	160
	LC4256B-3T176C	256	2.5	3	TQFP	176	128
	LC4256B-5T176C	256	2.5	5	TQFP	176	128
	LC4256B-75T176C	256	2.5	7.5	TQFP	176	128
	LC4256B-3T100C	256	2.5	3	TQFP	100	64
	LC4256B-5T100C	256	2.5	5	TQFP	100	64
	LC4256B-75T100C	256	2.5	7.5	TQFP	100	64
LC4384B	LC4384B-35F256C	384	2.5	3.5	fpBGA	256	192
	LC4384B-5F256C	384	2.5	5	fpBGA	256	192
	LC4384B-75F256C	384	2.5	7.5	fpBGA	256	192
	LC4384B-35T176C	384	2.5	3.5	TQFP	176	128
	LC4384B-5T176C	384	2.5	5	TQFP	176	128
	LC4384B-75T176C	384	2.5	7.5	TQFP	176	128

ispMACH 4000B (2.5V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4512B	LC4512B-35F256C	512	2.5	3.5	fpBGA	256	208
	LC4512B-5F256C	512	2.5	5	fpBGA	256	208
	LC4512B-75F256C	512	2.5	7.5	fpBGA	256	208
	LC4512B-35T176C	512	2.5	3.5	TQFP	176	128
	LC4512B-5T176C	512	2.5	5	TQFP	176	128
	LC4512B-75T176C	512	2.5	7.5	TQFP	176	128

ispMACH 4000V (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4032V	LC4032V-25T48C	32	3.3	2.5	TQFP	48	32
	LC4032V-5T48C	32	3.3	5	TQFP	48	32
	LC4032V-75T48C	32	3.3	7.5	TQFP	48	32
	LC4032V-25T44C	32	3.3	2.5	TQFP	44	30
	LC4032V-5T44C	32	3.3	5	TQFP	44	30
	LC4032V-75T44C	32	3.3	7.5	TQFP	44	30
LC4064V	LC4064V-25T100C	64	3.3	2.5	TQFP	100	64
	LC4064V-5T100C	64	3.3	5	TQFP	100	64
	LC4064V-75T100C	64	3.3	7.5	TQFP	100	64
	LC4064V-25T48C	64	3.3	2.5	TQFP	48	32
	LC4064V-5T48C	64	3.3	5	TQFP	48	32
	LC4064V-75T48C	64	3.3	7.5	TQFP	48	32
	LC4064V-25T44C	64	3.3	2.5	TQFP	44	30
	LC4064V-5T44C	64	3.3	5	TQFP	44	30
	LC4064V-75T44C	64	3.3	7.5	TQFP	44	30
LC4128V	LC4128V-27T144C	128	3.3	2.7	TQFP	144	96
	LC4128V-5T144C	128	3.3	5	TQFP	144	96
	LC4128V-75T144C	128	3.3	7.5	TQFP	144	96
	LC4128V-27T128C	128	3.3	2.7	TQFP	128	92
	LC4128V-5T128C	128	3.3	5	TQFP	128	92
	LC4128V-75T128C	128	3.3	7.5	TQFP	128	92
	LC4128V-27T100C	128	3.3	2.7	TQFP	100	64
	LC4128V-5T100C	128	3.3	5	TQFP	100	64
	LC4128V-75T100C	128	3.3	7.5	TQFP	100	64

ispMACH 4000V (3.3V) Commercial Devices (Cont.)

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O
LC4256V	LC4256V-3F256AC	256	3.3	3	fpBGA	256	128
	LC4256V-5F256AC	256	3.3	5	fpBGA	256	128
	LC4256V-75F256AC	256	3.3	7.5	fpBGA	256	128
	LC4256V-3F256BC	256	3.3	3	fpBGA	256	160
	LC4256V-5F256BC	256	3.3	5	fpBGA	256	160
	LC4256V-75F256BC	256	3.3	7.5	fpBGA	256	160
	LC4256V-3T176C	256	3.3	3	TQFP	176	128
	LC4256V-5T176C	256	3.3	5	TQFP	176	128
	LC4256V-75T176C	256	3.3	7.5	TQFP	176	128
	LC4256V-3T144C	256	3.3	3	TQFP	144	96
	LC4256V-5T144C	256	3.3	5	TQFP	144	96
	LC4256V-75T144C	256	3.3	7.5	TQFP	144	96
	LC4256V-3T100C	256	3.3	3	TQFP	100	64
	LC4256V-5T100C	256	3.3	5	TQFP	100	64
	LC4256V-75T100C	256	3.3	7.5	TQFP	100	64
LC4384V	LC4384V-35F256C	384	3.3	3.5	fpBGA	256	192
	LC4384V-5F256C	384	3.3	5	fpBGA	256	192
	LC4384V-75F256C	384	3.3	7.5	fpBGA	256	192
	LC4384V-35T176C	384	3.3	3.5	TQFP	176	128
	LC4384V-5T176C	384	3.3	5	TQFP	176	128
	LC4384V-75T176C	384	3.3	7.5	TQFP	176	128
LC4512V	LC4512V-35F256C	512	3.3	3.5	fpBGA	256	208
	LC4512V-5F256C	512	3.3	5	fpBGA	256	208
	LC4512V-75F256C	512	3.3	7.5	fpBGA	256	208
	LC4512V-35T176C	512	3.3	3.5	TQFP	176	128
	LC4512V-5T176C	512	3.3	5	TQFP	176	128
	LC4512V-75T176C	512	3.3	7.5	TQFP	176	128

ispMACH 4000ZC (Zero Power, 1.8V) Commercial Devices[1]

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O
LC4032ZC	LC4032ZC-35T48C	32	1.8	3.5	TQFP	48	32
	LC4032ZC-5T48C	32	1.8	5	TQFP	48	32
	LC4032ZC-75T48C	32	1.8	7.5	TQFP	48	32

1. Preliminary information.

ispMACH 4000C (1.8V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O
LC4032C	LC4032C-5T48I	32	1.8	5	TQFP	48	32
	LC4032C-75T48I	32	1.8	7.5	TQFP	48	32
	LC4032C-10T48I	32	1.8	10	TQFP	48	32
	LC4032C-5T44I	32	1.8	5	TQFP	44	30
	LC4032C-75T44I	32	1.8	7.5	TQFP	44	30
	LC4032C-10T44I	32	1.8	10	TQFP	44	30

ispMACH 4000C (1.8V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4064C	LC4064C-5T100I	64	1.8	5	TQFP	100	64
	LC4064C-75T100I	64	1.8	7.5	TQFP	100	64
	LC4064C-10T100I	64	1.8	10	TQFP	100	64
	LC4064C-5T48I	64	1.8	5	TQFP	48	32
	LC4064C-75T48I	64	1.8	7.5	TQFP	48	32
	LC4064C-10T48I	64	1.8	10	TQFP	48	32
	LC4064C-5T44I	64	1.8	5	TQFP	44	30
	LC4064C-75T44I	64	1.8	7.5	TQFP	44	30
	LC4064C-10T44I	64	1.8	10	TQFP	44	30
LC4128C	LC4128C-5T128I	128	1.8	5	TQFP	128	92
	LC4128C-75T128I	128	1.8	7.5	TQFP	128	92
	LC4128C-10T128I	128	1.8	10	TQFP	128	92
	LC4128C-5T100I	128	1.8	5	TQFP	100	64
	LC4128C-75T100I	128	1.8	7.5	TQFP	100	64
	LC4128C-10T100I	128	1.8	10	TQFP	100	64
LC4256C	LC4256C-5F256AI	256	1.8	5	fpBGA	256	128
	LC4256C-75F256AI	256	1.8	7.5	fpBGA	256	128
	LC4256C-10F256AI	256	1.8	10	fpBGA	256	128
	LC4256C-5F256BI	256	1.8	5	fpBGA	256	160
	LC4256C-75F256BI	256	1.8	7.5	fpBGA	256	160
	LC4256C-10F256BI	256	1.8	10	fpBGA	256	160
	LC4256C-5T176I	256	1.8	5	TQFP	176	128
	LC4256C-75T176I	256	1.8	7.5	TQFP	176	128
	LC4256C-10T176I	256	1.8	10	TQFP	176	128
	LC4256C-5T100I	256	1.8	5	TQFP	100	64
	LC4256C-75T100I	256	1.8	7.5	TQFP	100	64
	LC4256C-10T100I	256	1.8	10	TQFP	100	64
LC4384C	LC4384C-5F256I	384	1.8	5	fpBGA	256	192
	LC4384C-75F256I	384	1.8	7.5	fpBGA	256	192
	LC4384C-10F256I	384	1.8	10	fpBGA	256	192
	LC4384C-5T176I	384	1.8	5	TQFP	176	128
	LC4384C-75T176I	384	1.8	7.5	TQFP	176	128
	LC4384C-10T176I	384	1.8	10	TQFP	176	128
LC4512C	LC4512C-5F256I	512	1.8	5	fpBGA	256	208
	LC4512C-75F256I	512	1.8	7.5	fpBGA	256	208
	LC4512C-10F256I	512	1.8	10	fpBGA	256	208
	LC4512C-5T176I	512	1.8	5	TQFP	176	128
	LC4512C-75T176I	512	1.8	7.5	TQFP	176	128
	LC4512C-10T176I	512	1.8	10	TQFP	176	128

ispMACH 4000B (2.5V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O
LC4032B	LC4032B-5T48I	32	2.5	5	TQFP	48	32
	LC4032B-75T48I	32	2.5	7.5	TQFP	48	32
	LC4032B-10T48I	32	2.5	10	TQFP	48	32
	LC4032B-5T44I	32	2.5	5	TQFP	44	30
	LC4032B-75T44I	32	2.5	7.5	TQFP	44	30
	LC4032B-10T44I	32	2.5	10	TQFP	44	30
LC4064B	LC4064B-5T100I	64	2.5	5	TQFP	100	64
	LC4064B-75T100I	64	2.5	7.5	TQFP	100	64
	LC4064B-10T100I	64	2.5	10	TQFP	100	64
	LC4064B-5T48I	64	2.5	5	TQFP	48	32
	LC4064B-75T48I	64	2.5	7.5	TQFP	48	32
	LC4064B-10T48I	64	2.5	10	TQFP	48	32
	LC4064B-5T44I	64	2.5	5	TQFP	44	30
	LC4064B-75T44I	64	2.5	7.5	TQFP	44	30
	LC4064B-10T44I	64	2.5	10	TQFP	44	30
LC4128B	LC4128B-5T128I	128	2.5	5	TQFP	128	92
	LC4128B-75T128I	128	2.5	7.5	TQFP	128	92
	LC4128B-10T128I	128	2.5	10	TQFP	128	92
	LC4128B-5T100I	128	2.5	5	TQFP	100	64
	LC4128B-75T100I	128	2.5	7.5	TQFP	100	64
	LC4128B-10T100I	128	2.5	10	TQFP	100	64
LC4256B	LC4256B-5F256AI	256	2.5	5	fpBGA	256	128
	LC4256B-75F256AI	256	2.5	7.5	fpBGA	256	128
	LC4256B-10F256AI	256	2.5	10	fpBGA	256	128
	LC4256B-5F256BI	256	2.5	5	fpBGA	256	160
	LC4256B-75F256BI	256	2.5	7.5	fpBGA	256	160
	LC4256B-10F256BI	256	2.5	10	fpBGA	256	160
	LC4256B-5T176I	256	2.5	5	TQFP	176	128
	LC4256B-75T176I	256	2.5	7.5	TQFP	176	128
	LC4256B-10T176I	256	2.5	10	TQFP	176	128
	LC4256B-5T100I	256	2.5	5	TQFP	100	64
	LC4256B-75T100I	256	2.5	7.5	TQFP	100	64
	LC4256B-10T100I	256	2.5	10	TQFP	100	64
LC4384B	LC4384B-5F256I	384	2.5	5	fpBGA	256	192
	LC4384B-75F256I	384	2.5	7.5	fpBGA	256	192
	LC4384B-10F256I	384	2.5	10	fpBGA	256	192
	LC4384B-5T176I	384	2.5	5	TQFP	176	128
	LC4384B-75T176I	384	2.5	7.5	TQFP	176	128
	LC4384B-10T176I	384	2.5	10	TQFP	176	128

ispMACH 4000B (2.5V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4512B	LC4512B-5F256I	512	2.5	5	fpBGA	256	208
	LC4512B-75F256I	512	2.5	7.5	fpBGA	256	208
	LC4512B-10F256I	512	2.5	10	fpBGA	256	208
	LC4512B-5T176I	512	2.5	5	TQFP	176	128
	LC4512B-75T176I	512	2.5	7.5	TQFP	176	128
	LC4512B-10T176I	512	2.5	10	TQFP	176	128

ispMACH 4000V (3.3V) Industrial Devices

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4032V	LC4032V-5T48I	32	3.3	5	TQFP	48	32
	LC4032V-75T48I	32	3.3	7.5	TQFP	48	32
	LC4032V-10T48I	32	3.3	10	TQFP	48	32
	LC4032V-5T44I	32	3.3	5	TQFP	44	30
	LC4032V-75T44I	32	3.3	7.5	TQFP	44	30
	LC4032V-10T44I	32	3.3	10	TQFP	44	30
LC4064V	LC4064V-5T100I	64	3.3	5	TQFP	100	64
	LC4064V-75T100I	64	3.3	7.5	TQFP	100	64
	LC4064V-10T100I	64	3.3	10	TQFP	100	64
	LC4064V-5T48I	64	3.3	5	TQFP	48	32
	LC4064V-75T48I	64	3.3	7.5	TQFP	48	32
	LC4064V-10T48I	64	3.3	10	TQFP	48	32
	LC4064V-5T44I	64	3.3	5	TQFP	44	30
	LC4064V-75T44I	64	3.3	7.5	TQFP	44	30
	LC4064V-10T44I	64	3.3	10	TQFP	44	30
LC4128V	LC4128V-5T144I	128	3.3	5	TQFP	144	96
	LC4128V-75T144I	128	3.3	7.5	TQFP	144	96
	LC4128V-10T144I	128	3.3	10	TQFP	144	96
	LC4128V-5T128I	128	3.3	5	TQFP	128	92
	LC4128V-75T128I	128	3.3	7.5	TQFP	128	92
	LC4128V-10T128I	128	3.3	10	TQFP	128	92
	LC4128V-5T100I	128	3.3	5	TQFP	100	64
	LC4128V-75T100I	128	3.3	7.5	TQFP	100	64
	LC4128V-10T100I	128	3.3	10	TQFP	100	64

ispMACH 4000V (3.3V) Industrial Devices (Cont.)

Family	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4256V	LC4256V-5F256AI	256	3.3	5	fpBGA	256	128
	LC4256V-75F256AI	256	3.3	7.5	fpBGA	256	128
	LC4256V-10F256AI	256	3.3	10	fpBGA	256	128
	LC4256V-5F256BI	256	3.3	5	fpBGA	256	160
	LC4256V-75F256BI	256	3.3	7.5	fpBGA	256	160
	LC4256V-10F256BI	256	3.3	10	fpBGA	256	160
	LC4256V-5T176I	256	3.3	5	TQFP	176	128
	LC4256V-75T176I	256	3.3	7.5	TQFP	176	128
	LC4256V-10T176I	256	3.3	10	TQFP	176	128
	LC4256V-5T144I	256	3.3	5	TQFP	144	96
	LC4256V-75T144I	256	3.3	7.5	TQFP	144	96
	LC4256V-10T144I	256	3.3	10	TQFP	144	96
	LC4256V-5T100I	256	3.3	5	TQFP	100	64
	LC4256V-75T100I	256	3.3	7.5	TQFP	100	64
	LC4256V-10T100I	256	3.3	10	TQFP	100	64
LC4384V	LC4384V-5F256I	384	3.3	5	fpBGA	256	192
	LC4384V-75F256I	384	3.3	7.5	fpBGA	256	192
	LC4384V-10F256I	384	3.3	10	fpBGA	256	192
	LC4384V-5T176I	384	3.3	5	TQFP	176	128
	LC4384V-75T176I	384	3.3	7.5	TQFP	176	128
	LC4384V-10T176I	384	3.3	10	TQFP	176	128
LC4512V	LC4512V-5F256I	512	3.3	5	fpBGA	256	208
	LC4512V-75F256I	512	3.3	7.5	fpBGA	256	208
	LC4512V-10F256I	512	3.3	10	fpBGA	256	208
	LC4512V-5T176I	512	3.3	5	TQFP	176	128
	LC4512V-75T176I	512	3.3	7.5	TQFP	176	128
	LC4512V-10T176I	512	3.3	10	TQFP	176	128

ispMACH 4000V (3.3V) Automotive Devices

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/C
LC4032V	LC4032V-75T48E	32	3.3	7.5	TQFP	48	32
	LC4032V-75T44E	32	3.3	7.5	TQFP	44	30
LC4064V	LC4064V-75T100E	64	3.3	7.5	TQFP	100	64
	LC4064V-75T48E	64	3.3	7.5	TQFP	48	32
	LC4064V-75T44E	64	3.3	7.5	TQFP	44	30
LC4128V	LC4128V-75T144E	128	3.3	7.5	TQFP	144	96
	LC4128V-75T128E	128	3.3	7.5	TQFP	128	92
	LC4128V-75T100E	128	3.3	7.5	TQFP	100	64
LC4256V	LC4256V-75T176E	256	3.3	7.5	TQFP	176	128
	LC4256V-75T144E	256	3.3	7.5	TQFP	144	96
	LC4256V-75T100E	256	3.3	7.5	TQFP	100	64

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with th 4000V/B/C/Z family:

- *ispMACH 4000 Timing Model Design and Usage Guidelines* (TN1004)
- *ispMACH 4000V/B/C Power Consumption* (TN1005)
- *Low Power Design Guide* (TN1042)