MC2674

Advance Information

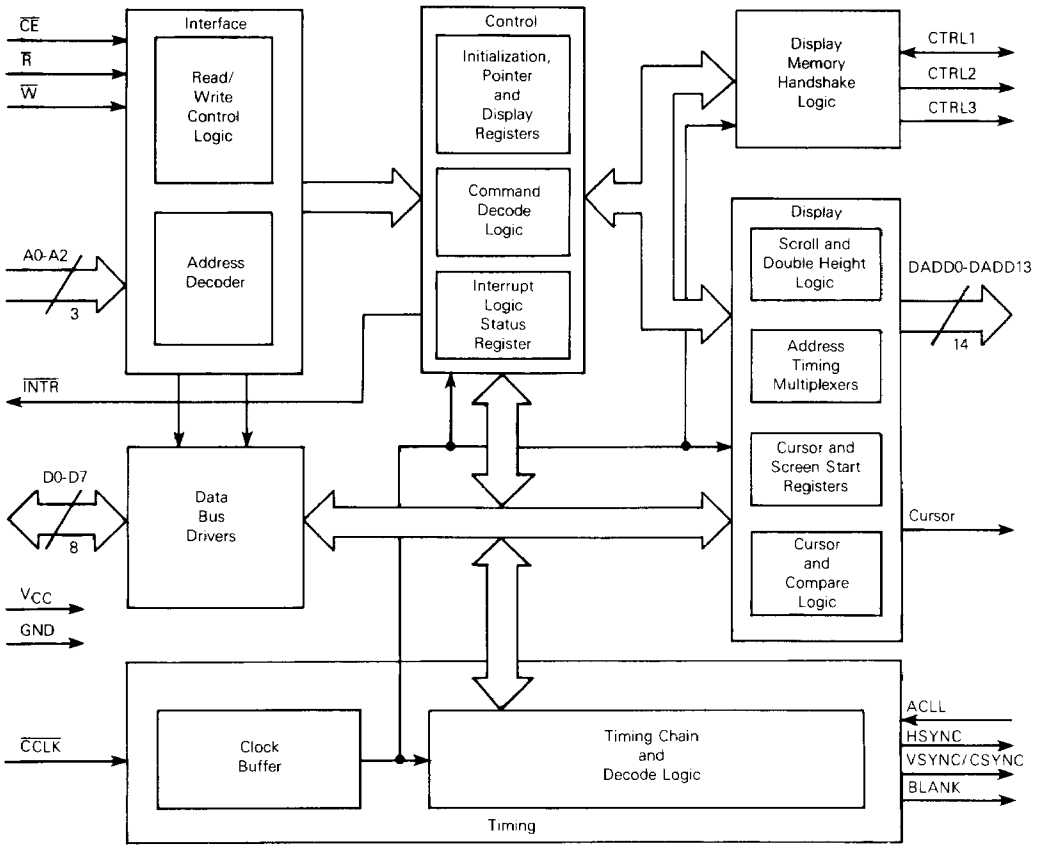
Advanced Video Display Controller (AVDC)

The MC2674 advanced video display controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster-scan techniques. The AVDC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the AVDC.

A minimum CRT terminal system configuration consists of an AVDC, a keyboard controller, an asynchronous communications interface adapter, character ROM, and an attributes controller. Other necessary parts of the system are a single-chip microcomputer such as the MC6809, display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. System complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data buses.

- 4 MHz Character Rate
- 1 to 256 Characters Per Row
- 1 to 16 Raster Lines Per Character Row
- Bit Mapped Graphics Mode
- Programmable Horizontal and Vertical Sync Generators
- Interlaced or Non-Interlaced Operation
- Up to 64K RAM Address for Multiple-Page Operation
- Readable, Writeable, and Incrementable Cursor
- Programmable Cursor Size and Blink
- AC Line Lock
- Automatic Wraparound of RAM
- Automatic Split Screen
- Automatic Bidirectional Soft Scrolling
- Programmable Scan Line Increment
- Row Table Addressing Mode
- Double Height Tops and Bottoms
- Double Width Control Output
- Selectable Buffer Interface Modes
- Dynamic RAM Refresh
- Completely TTL Compatible
- Single +5-Volt Power Supply
- Power-On Reset Circuit
- Applications Include: CRT Terminals, Word Processing Systems, Small Business Computers, and Home Computers

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance Plastic Package	θ_{JA}	50	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{PORT}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} < P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part, K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A

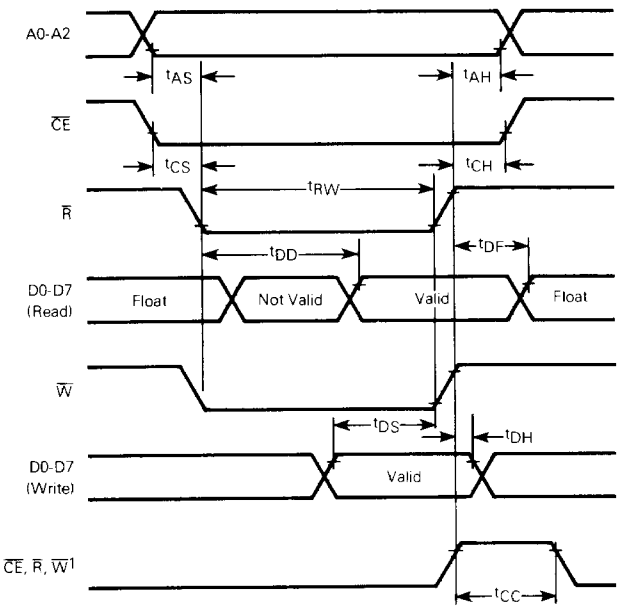
DC ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to 70°C, $V_{CC} = 5.0$ V ± 5%)

Parameter	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	−0.3	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Output Low Voltage ($I_{OL} = 2.4$ mA)	V_{OL}	–	0.4	V
Output High Voltage (Except $\overline{INTR}$ Output) ($I_{OH} = -200\ \mu A$)	V_{OH}	2.4	–	V
Input Leakage Current ($V_{in} = 0$ to V_{CC})	I_{in}	−10	10	μA
Hi-Z (Off-State) Leakage Current ($V_{CC} = 5.25$ V, $V_{in} = 0.4$ to 2.4 V)	I_{TSI}	−10	10	μA
$\overline{INTR}$ Open-Drain Output Leakage Current ($V_O = 0$ to V_{CC})	I_{OD}	–	10	μA
Internal Power Dissipation (Measured at $T_A = 0°C$)	P_{INT}	–	800	mW

AC ELECTRICAL CHARACTERISTICS — BUS TIMING (T_A = 0°C to 70°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	2.7 MHz Min	2.7 MHz Max	4.0 MHz Min	4.0 MHz Max	Unit
A0-A2 Setup Time to $\overline{W}$, $\overline{R}$ Low	t_{AS}	30	–	30	–	ns
A0-A2 Hold Time from $\overline{W}$, $\overline{R}$ High	t_{AH}	0	–	0	–	ns
$\overline{CE}$ Setup Time to $\overline{W}$, $\overline{R}$ Low	t_{CS}	0	–	0	–	ns
$\overline{CE}$ Hold Time from $\overline{W}$, $\overline{R}$ High	t_{CH}	0	–	0	–	ns
$\overline{W}$, $\overline{R}$ Pulse Width	t_{RW}	250	–	200	–	ns
Data Valid after $\overline{R}$ Low	t_{DD}	–	200	–	200	ns
Data Bus Floating after $\overline{R}$ High	t_{DF}	–	100	–	100	ns
Data Setup Time to $\overline{W}$ High	t_{DS}	150	–	150	–	ns
Data Hold Time from $\overline{W}$ High	t_{DH}	10	–	5	–	ns
High Time from $\overline{CE}$ to $\overline{CE}$ Consecutive Commands Other Accesses	t_{CC}	 t_{CCP} 300	 – –	 t_{CCP} 300	 – –	 ns ns

BUS TIMING DIAGRAM



NOTES:
1. Any two must be high for t_{CC}.
2. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

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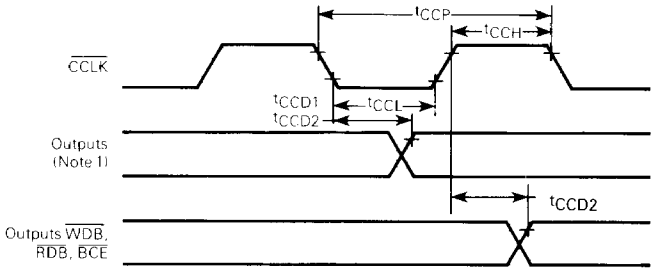
AC ELECTRICAL CHARACTERISTICS — CHARACTER CLOCK ($\overline{CCLK}$) TIMING ($T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 5\%$)

Parameter	Symbol	2.7 MHz		4.0 MHz		Unit
		Min	Max	Min	Max	
$\overline{CCLK}$ Period	t_{CCP}	370	10000	250	10000	ns
$\overline{CCLK}$ High Time	t_{CCH}	125	–	100	–	ns
$\overline{CCLK}$ Low Time	t_{CCL}	125	–	100	–	ns
Output Delay Time from $\overline{CCLK}$ Edge						
DADD0-13, MBC	t_{CCD1}	40	175	40	150	ns
BLANK, HSYNC, VSYNC/CSYNC, CURSOR, $\overline{BEXT}$, $\overline{BREQ}$, $\overline{BACK}$, $\overline{BCE}$, $\overline{WDB}$, $\overline{RDB}$*	t_{CCD2}	40	225	40	200	ns

* $\overline{BCE}$, $\overline{WDB}$, and $\overline{RDB}$ delays track each other within 10 nanoseconds. Also, these output delays will tend to follow direction (minimum/maximum) of DADD0-DADD13 delays.

CCLK TIMING DIAGRAM



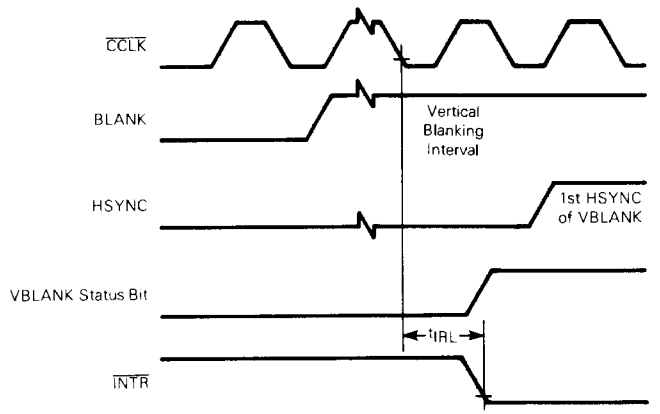
NOTES:
1. DADD0-DADD13, BLANK, HSYNC, CSYNC VSYNC, CURSOR, $\overline{BEXT}$, $\overline{BREQ}$, $\overline{BCE}$, MBC, BACK.
2. $\overline{BCE}$ changes state on both $\overline{CCLK}$ edges.
3. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

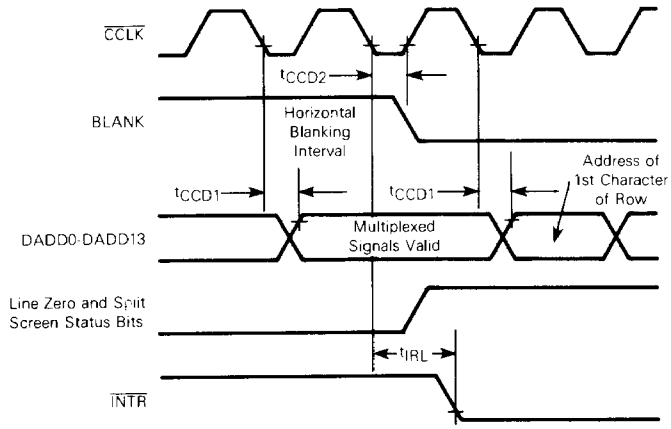
AC ELECTRICAL CHARACTERISTICS – OTHER TIMING ($T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 5\%$)

Parameter	Symbol	2.7 MHz		4.0 MHz		Unit
		Min	Max	Min	Max	
READY RDFLG low from $\overline{W}$ High*	t_{RDL}	—	$t_{CCP} - 30$	—	$t_{CCP} - 30$	ns
$\overline{BACK}$ High from $\overline{PBREQ}$ Low	t_{BAK}	—	225	—	200	ns
$\overline{BEXT}$ High from $\overline{PBREQ}$ High	t_{BXT}	—	225	—	200	ns
$\overline{INTR}$ Low from $\overline{CCLK}$ Low	t_{IRL}	—	225	—	200	ns
$\overline{INTR}$ High from $\overline{W}$, $\overline{R}$ High*	t_{IRH}	—	600	—	600	ns
ACLL from HSYNC	t_{AC}	$3 \times t_{CCP}$	—	$3 \times t_{CCP}$	—	ns

*Timing is illustrated and specified referenced to $\overline{W}$ and $\overline{R}$ inputs. Device may also be operated with $\overline{CE}$ as the "strobing" input. In this case, all timing specifications apply referenced to falling and rising edges of $\overline{CE}$.

OTHER TIMING DIAGRAMS (Sheet 2 of 2)





NOTE: All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

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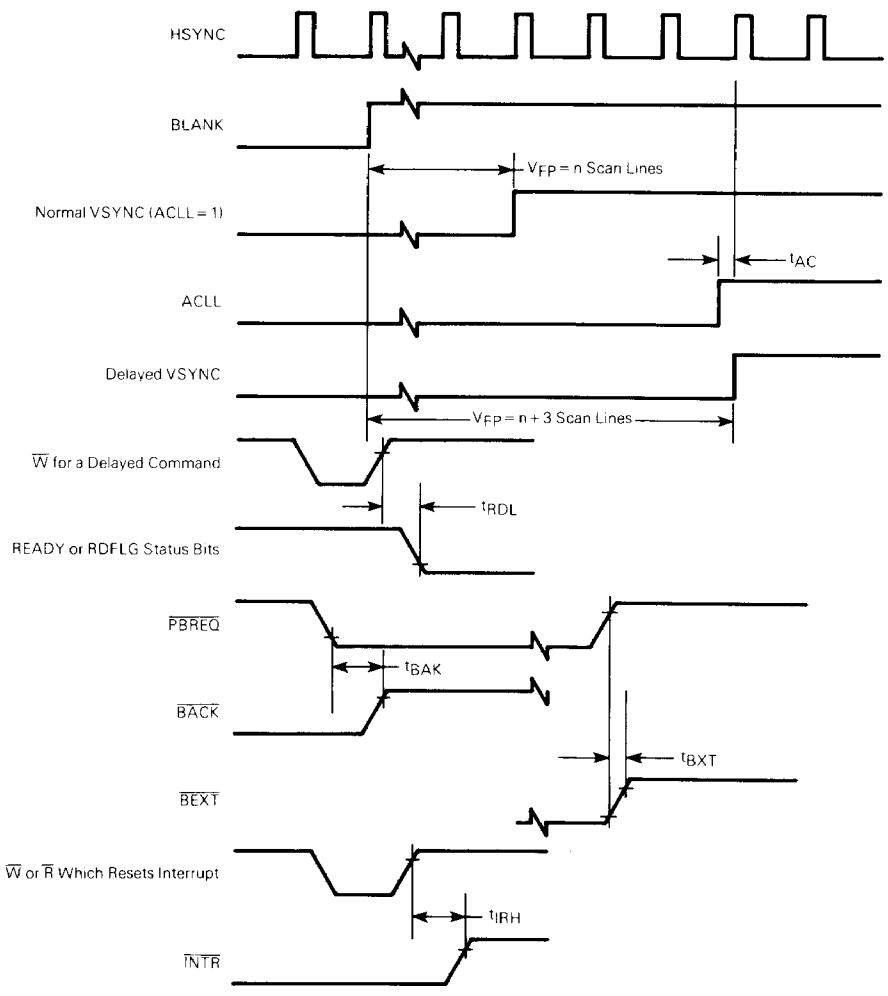
OTHER TIMING DIAGRAMS (Sheet 2 of 2)

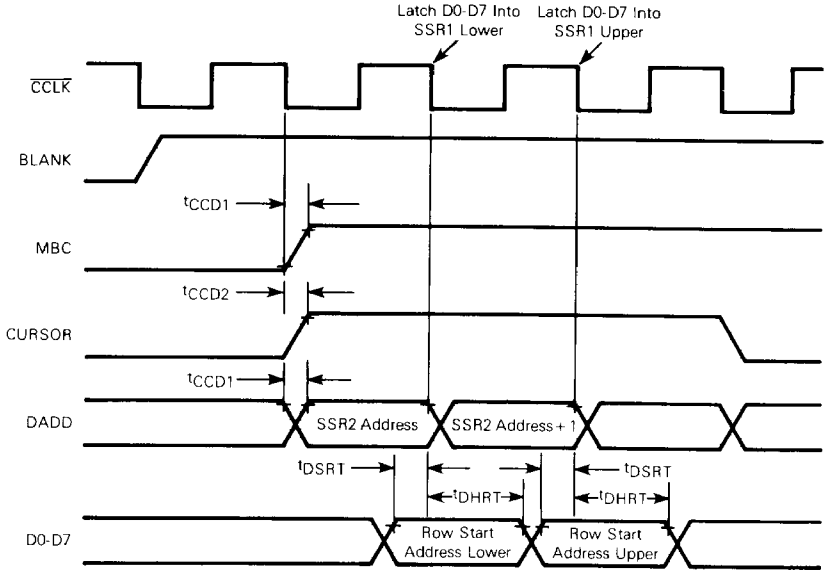


NOTE: All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

AC ELECTRICAL CHARACTERISTICS — ROW TABLE INPUT TIMING (T_A = 0°C to 70°C, V_{CC} = 5 V ± 5%)

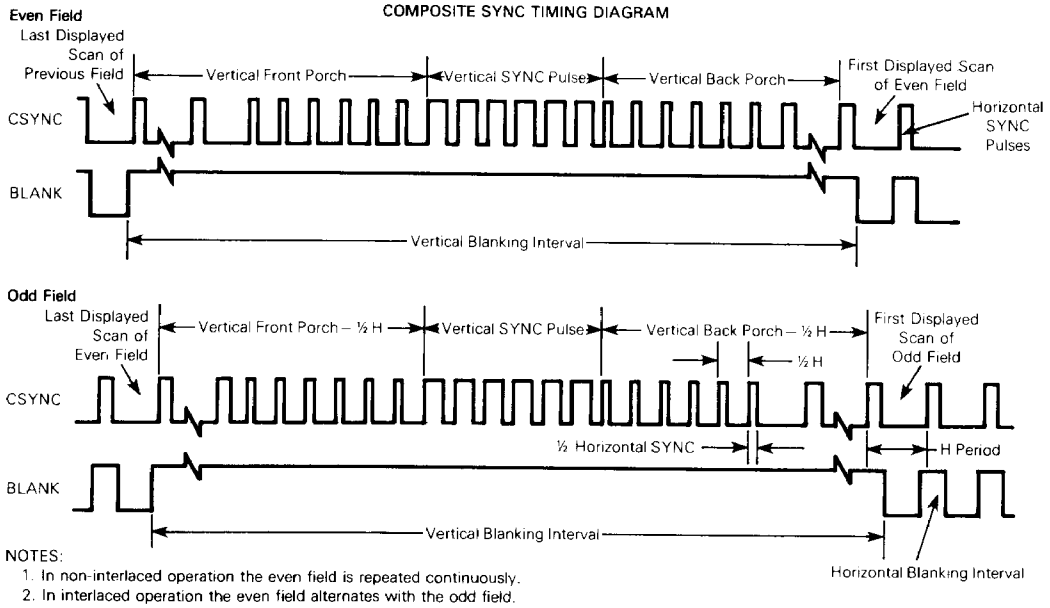
Parameter	Symbol	2.7 MHz		4.0 MHz		Unit
		Min	Max	Min	Max	
Data Setup Time to $\overline{CCLK}$ Low	t_{DSRT}	100	–	60	–	ns
Data Hold Time from $\overline{CCLK}$ Low	t_{DHRT}	60	–	60	–	ns

ROW TABLE FETCH I/O TIMING DIAGRAM



NOTE: All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

COMPOSITE SYNC TIMING DIAGRAM



NOTES:
1. In non-interlaced operation the even field is repeated continuously.
2. In interlaced operation the even field alternates with the odd field.

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SIGNAL DESCRIPTION

The input and output signals for the AVDC are described in the following paragraphs.

ADDRESS LINES (A0-A2)

These input lines are used to select AVDC internal register for read/write operations and for commands.

DATA BUS (D0-D7)

The 8-bit bidirectional three-state data bus controls all data, command, and status transfers between the CPU and the AVDC. Bit 0 is the least significant bit and bit 7 is the most significant bit. The direction of the transfer is controlled by the read ($\overline{R}$) and write ($\overline{W}$) inputs when chip enable ($\overline{CE}$) input is low. When the $\overline{CE}$ input is high, the data bus is in the three-state condition.

READ STROBE ($\overline{R}$)

This pin is an active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by the address lines to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{R}$.

WRITE STROBE ($\overline{W}$)

This is an active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by the address lines. The transfer occurs on the trailing (rising) edge of $\overline{W}$.

CHIP ENABLE ($\overline{CE}$)

This is an active low input. When low, data transfers between the CPU and the AVDC are enabled on the data bus as controlled by the write strobe, read strobe, and address lines. When $\overline{CE}$ is high, effectively, the AVDC is isolated from the data bus and D0-D7 are placed in the three-state condition.

CHARACTER CLOCK ($\overline{CCLK}$)

This input is the timing signal derived from the video dot clock which is used to synchronize the AVDC's timing functions.

HORIZONTAL SYNC (HSYNC)

This active high output provides video horizontal sync pulses. The timing parameters are programmable.

VERTICAL SYNC/COMPOSITE SYNC (VSYNC/CSYNC)

A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.

BLANK (BLANK)

This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on display addresses DADD0 and DADD3 through DADD13 are valid on the trailing edge of BLANK.

CURSOR GATE (CURSOR)

This output becomes active for a specified number of scan lines when the address continued in the cursor register matches the address output on DADD0 through DADD13 for displayable character addresses. The first and last lines of the cursor and a blink option are programmable. When the row table addressing mode is enabled, this output is active for a portion of the blanking interval prior to the first scan line of a character row, while the AVDC is fetching the starting address for that row.

INTERRUPT REQUEST ($\overline{INTR}$)

This is an open-drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after a power-on reset or a master reset command.

AC LINE LOCK (ACLL)

If this input is low after the programmed vertical front porch interval, the vertical front porch will be lengthened by increments of horizontal scan line times until this input goes high.

HANDSHAKE CONTROL 1 (CTRL1)

In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory.

HANDSHAKE CONTROL 2 (CTRL2)

In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the AVDC has relinquished control of the display memory (DADD0-DADD13 are in the three-state condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.

HANDSHAKE CONTROL 3 (CTRL3)

In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes, provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control (MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer.

DISPLAY ADDRESS (DADD0-DADD13)

These outputs are used by the AVDC to address up to 16K of display memory directly, or to 64K of memory by demultiplexing DADD14 and DADD15. These outputs are floated at various times depending on the buffer mode. Various control

signals are multiplexed on DADD0 through DADD13 and are valid at the trailing edge of BLANK. The following paragraphs describes the control signals.

LINE GRAPHICS (DADD0/LG) – This is the output which denotes bit-mapped graphics mode.

DISPLAY ADDRESS 14 (DADD1/DADD14) – This is the multiplexed address bit used to extend addressing to 64K.

DISPLAY ADDRESS 15 (DADD2/DADD15) – This is the multiplexed address bit used to extend addressing to 64K.

LAST ROW (DADD3/LR) – This is the output which indicates the last active character row of each field.

LINE ADDRESS (DADD4-DADD7/LA0-LA3) – These outputs provide the number of the current scan line count for each character row.

FIRST LINE (DADD8/FL) – This output is asserted during the blanking interval just prior to the first scan line of each character row.

DOUBLE WIDTH (DADD9/DW) – This output denotes a double width character row.

UNDERLINE (DADD10/UL) – This output is asserted during the blanking interval just prior to the scan line which matches the programmed underline position (line 0 through 15).

BLINK FREQUENCY (DADD11/BLINK) – Blink frequency provides an output divided down from the vertical sync rate.

ODD FIELD (DADD12/ODD) – This active high signal is asserted before each scan line of the odd field when interlace is specified. Replaces DADD4/LA0 as the least significant line address for interlaced sync and video applications.

LAST LINE (DADD13/LL) – This output is asserted during the blanking interval just prior to the last scan line of each character row.

V_{CC} AND GND

Power is supplied to the AVDC using these two pins. V_{CC} is the +5 volts ±5% power input and GND is the ground connection.

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the AVDC contains the following major blocks: data bus buffer, interface logic, operation control, timing, display control, and buffer control. The major blocks are described in the following paragraphs.

DATA BUS BUFFER

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the AVDC.

INTERFACE LOGIC

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data buffer. The functions performed by the CPU read and write operations are shown in Table 1.

OPERATION CONTROL

The operation control section decodes configuration and operation commands from the CPU and generates appropriate signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

TIMING

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

DISPLAY CONTROL

The display control section generates linear addressing of up to 16K bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning and address comparisons required for generation of timing signals, double-height tops and bottoms, smooth scrolling, and the split-screen interrupts.

BUFFER CONTROL

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described in **SYSTEM CONFIGURATIONS.**

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TABLE 1 – AVDC ADDRESSING

A2	A1	A0	Read ($\overline{R}=0$)	Write ($\overline{W}=0$)
0	0	0	Interrupt Register	Initialization Registers*
0	0	1	Status Register	Command Register
0	1	0	Screen Start 1 Lower Register	Screen Start 1 Lower Register
0	1	1	Screen Start 1 Upper Register	Screen Start 1 Upper Register
1	0	0	Cursor Address Lower Register	Cursor Address Lower Register
1	0	1	Cursor Address Upper Register	Cursor Address Upper Register
1	1	0	Screen Start 2 Lower Register	Screen Start 2 Lower Register
1	1	1	Screen Start 2 Upper Register	Screen Start 2 Upper Register

* There are 15 initialization registers which are accessed sequentially via a single address. The AVDC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR14) is accessed. The pointer then continues to point to IR14 for additional accesses. Upon a power-on or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal that uses an MC2674, character ROM, a keyboard interface, and an attribute controller. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This bufferis typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row.

The AVDC supports four common system configurations of display-buffer memory, designated the independent, transparent, shared, and row-buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row-buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

The user programs IR0 bits 0 and 1 select the mode best suited for the system environment. The CTRL1, CTRL2, and CTRL3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

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INDEPENDENT MODE

The CPU-to-RAM interface configuration for this mode is illustrated in Figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly — the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The AVDC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

The CPU manages the data transfers by supplying commands to the AVDC. The commands used are:

1. Read/write at pointer address,
2. Read/write at cursor address (with optional increment of address), and
3. Write from cursor address to pointer address.

The operational sequence for a write operation is:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes address into cursor or pointer registers.
4. CPU issues "write at cursor with/without increment" or "write at pointer" command.
5. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. AVDC sets RDFLG status to indicate that the write is completed.

Similarly, a read operation proceeds as follows:

1. Steps 1. and 3. as above.
2. CPU issues "read at cursor with/without increment" or "read at pointer" command.
3. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and AVDC sets RDFLG status to indicate that the read is completed.
4. CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the "write from cursor to pointer" command:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.
4. CPU issues "write from cursor to pointer" command.
5. AVDC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. AVDC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously asserted delayed command has been completed.

Two timing sequences are possible for the "read/write at cursor/pointer" commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in Figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately five character clocks (see Figure 4).

Timing for the "write from cursor to pointer" operation is shown in Figure 5. The memory is filled at a rate of one location per two character times. The command will execute only during blanking intervals and may require many horizontal or vertical blanking intervals to complete. Additional delayed commands can be asserted immediately after this command has completed.

Immediately commands can be asserted at any time regardless of the state of the ready state/interrupt.

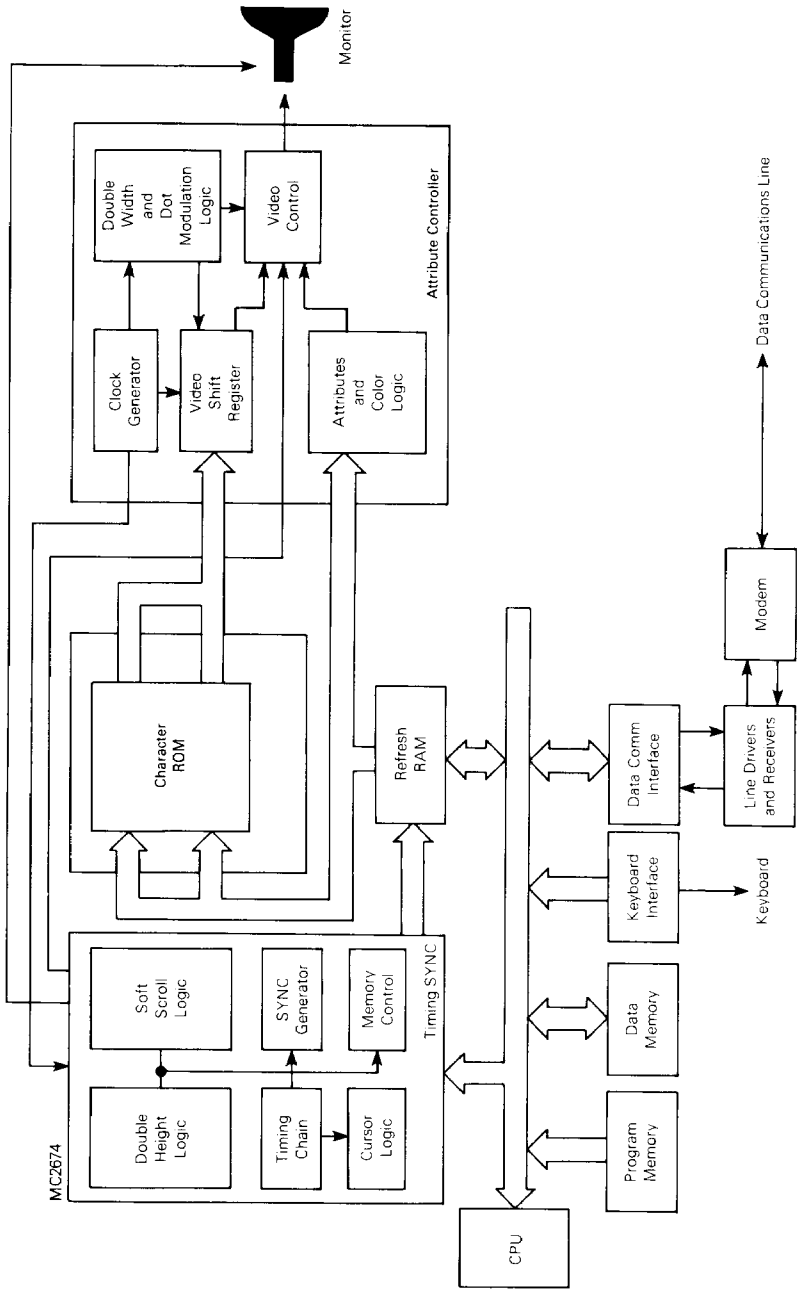

FIGURE 1 – CRT TERMINAL BLOCK DIAGRAM

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FIGURE 2 — INDEPENDENT BUFFER MODE CONFIGURATION

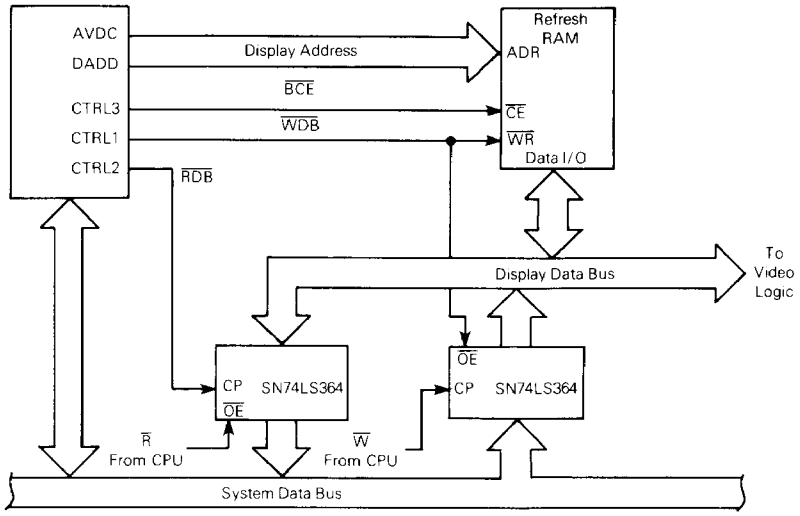
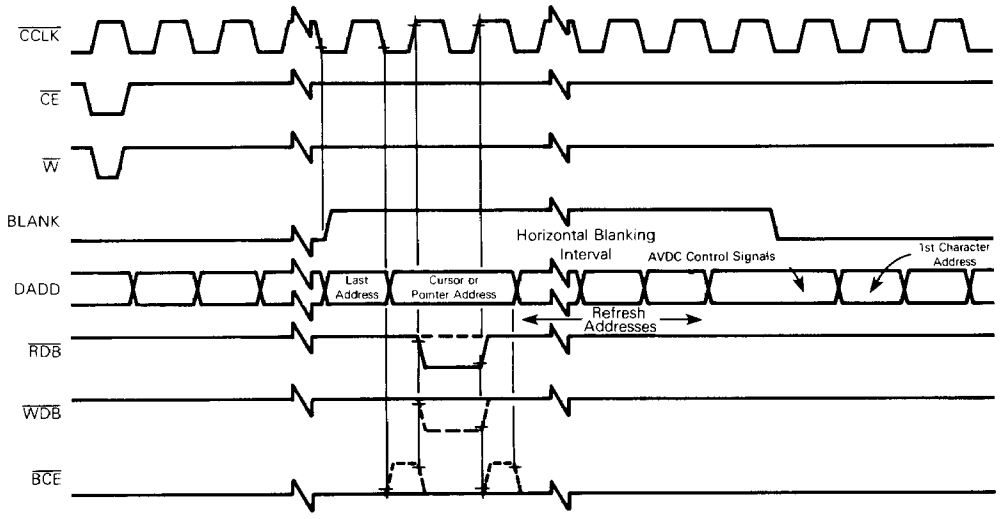
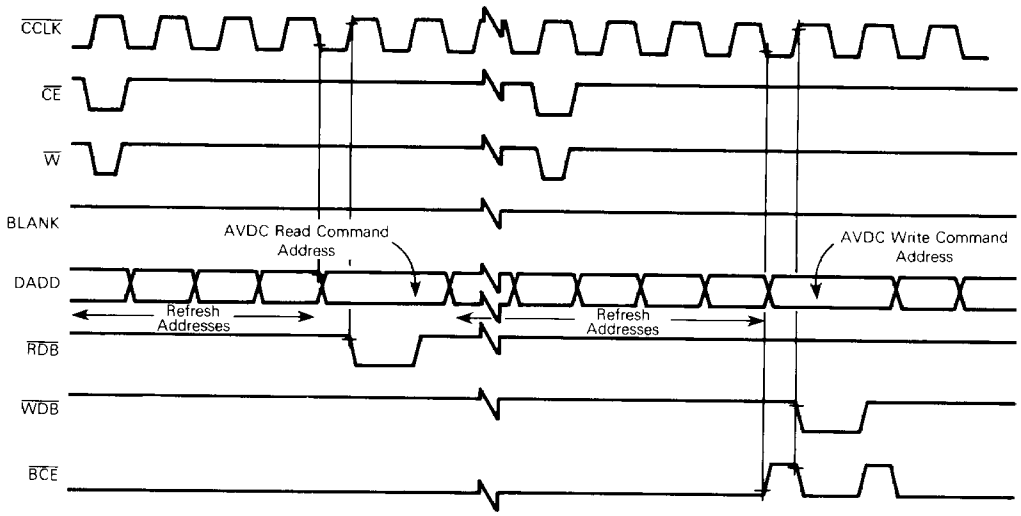


FIGURE 3 — READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command Received During Active Display Window)



NOTES:
1. Write waveforms shown in dotted lines.
2. If command execution occurs just prior to the first scan line of a character row and row table addressing mode is enabled, execution of the command is delayed by two character clocks from the timing illustrated.
3. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

FIGURE 4 – READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command Received While Display Is Blanked)



NOTE: All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

3

SHARED AND TRANSPARENT BUFFER MODES

In these modes, the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three-state drivers (see Figure 6). The processor bus request ($\overline{PBREQ}$) control signal informs the AVDC that the CPU is requesting access to the display buffer. In response to this request, the AVDC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data buses for CPU access. $\overline{BACK}$, which can be used as a "hold" input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the AVDC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the AVDC will blank the display and grant immediate access to the CPU. Timing for these modes is illustrated in Figures 7, 8, and 9.

ROW BUFFER MODE

Figures 10 and 11 show the timing and a typical hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the AVDC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The AVDC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The control signal $\overline{BREQ}$ informs the CPU that character addresses and the MBC signal will start at the next falling edge of BLANK. The CPU must release the address and data buses before this time to prevent bus contention. After the row of character data is transferred to the CPU, $\overline{BREQ}$ returns high to grant memory control back to the CPU.

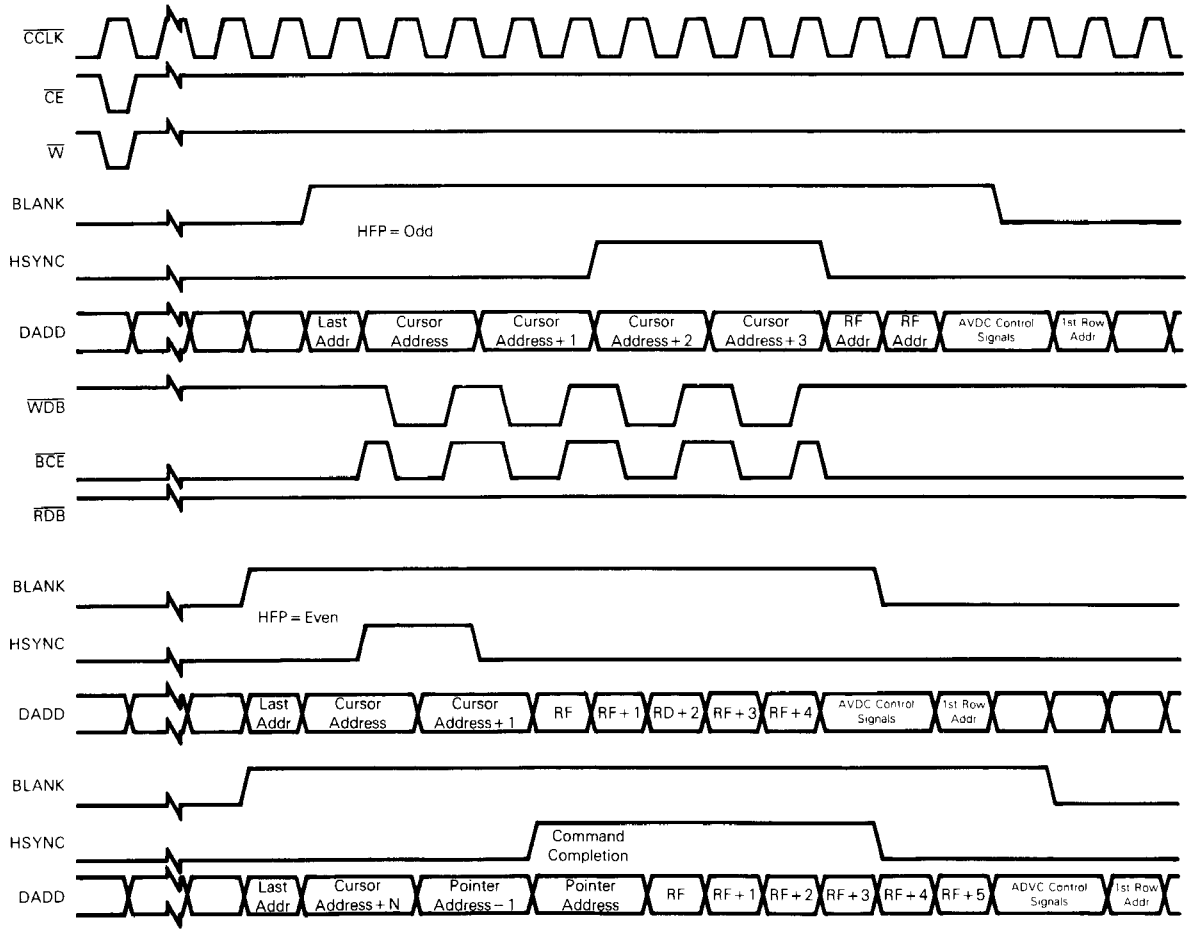
ROW TABLE ADDRESS MODE

In this mode, each character row in the screen image memory has a unique starting address. This provides greater flexibility with respect to screen operations, such as editing, than the sequential addressing mode. The row table, Figure 12, is a list of starting addresses for each character row and may reside anywhere in the AVDC's addressable memory space. Each entry in the table consists of two bytes: the first byte contains the eight least significant bits of the row starting address and the second byte contains, in its six least significant bits, the six most significant bits of the row starting address. The function of the two most significant bits of the second byte is selected by programming IR0[7]. They may be used either as row attribute bits to control double width and double height for that character row, or as an additional two address bits to extend the usable display memory to 64K.

The first address of the row table operation is designated in screen start register 2 (SSR2). If row table addressing is enabled via IR2[7], the AVDC fetches the next row's starting address from the table during the blanking interval prior to the first scan line of each character row, while simultaneously incrementing the contents of SSR2 by two so as to point to the next table entry. The fetching of the row starting address from the row table is indicated by the assertion of the CURSOR output during BLANK. The address read from the table by the AVDC is loaded into screen start register 1 (SSR1) for use internally. Since the contents of SSR2 changes as the table entries are fetched, it must be reinitialized to point to the first table entry during each vertical retrace interval.

Row table addressing is intended primarily for use in conjunction with the row buffer mode of operation and requires no additional circuitry in that case. It may also be used with

FIGURE 5 — WRITE FROM CURSOR TO POINTER COMMAND TIMING



NOTE:
If command execution occurs just prior to the first scan line of a character row and row table addressing mode is enabled, execution of the command is delayed by two character clocks from the timing illustrated.

FIGURE 6 — AVDC SHARED OR TRANSPARENT BUFFER MODES

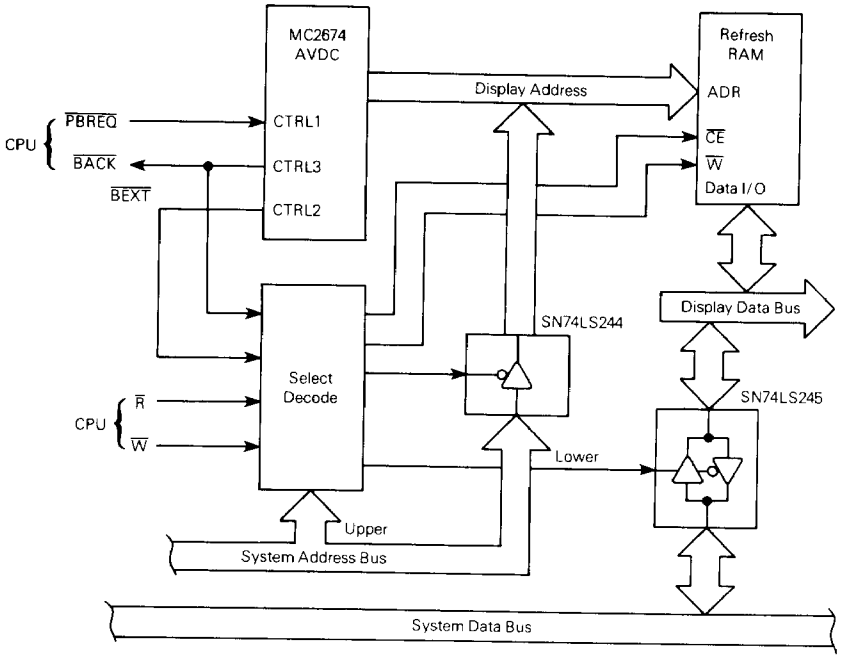
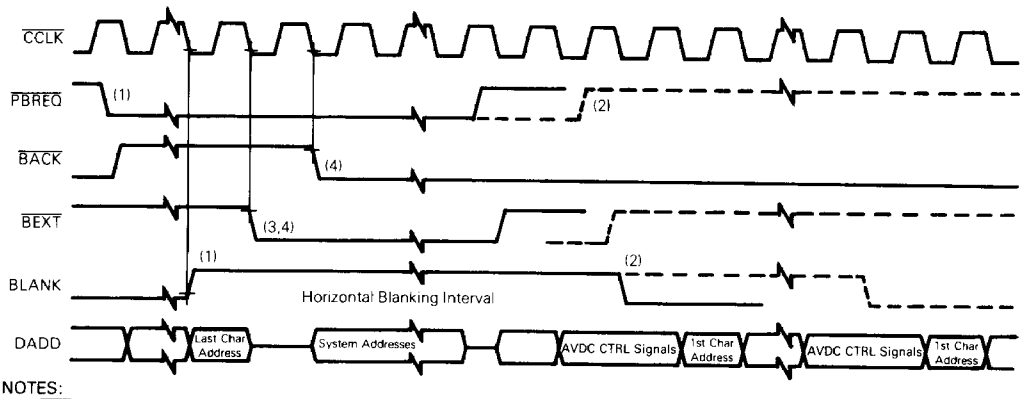


FIGURE 7 — TRANSPARENT BUFFER MODE TIMING



NOTES:
1. PBREQ must be asserted prior to the rising edge of BLANK in order for sequence to begin during that blanking period.
2. If PBREQ is negated after the next to last CCLK of the horizontal blanking interval, the next scan line will also be blanked.
3. Accesses during vertical blank or "display off" are granted only at the beginning of the horizontal front porch.
4. If row table addressing is enabled, CPU access is delayed by two character clocks prior to the first scan line of each character row.
5. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

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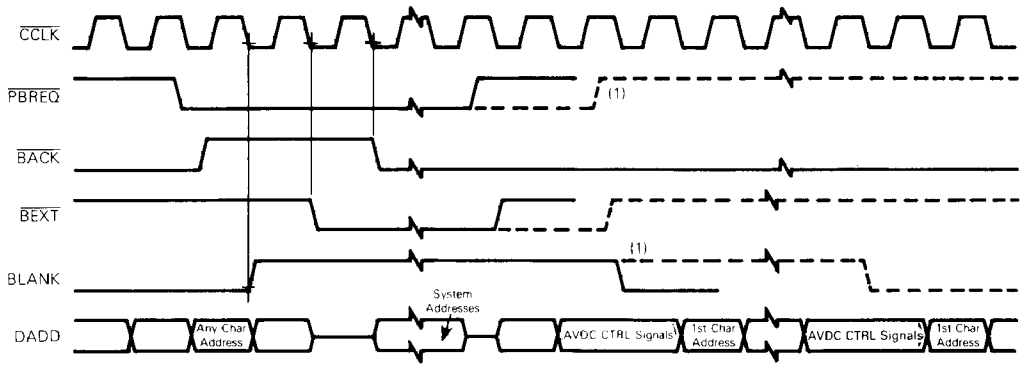
FIGURE 8 — SHARED BUFFER MODE TIMING



NOTES:
1. If $\overline{\text{PBREQ}}$ is negated after the next to last $\overline{\text{CCLK}}$ of the horizontal blanking interval, the next scan line will also be blanked.
2. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

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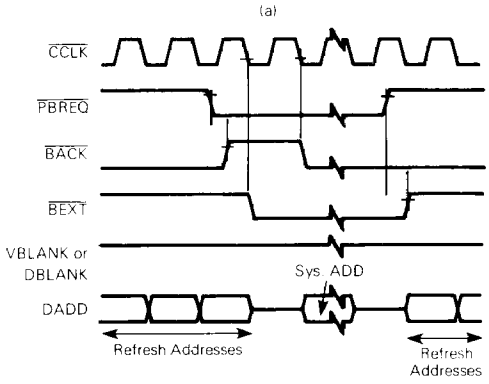
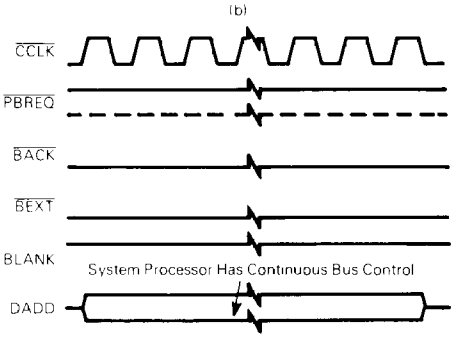
FIGURE 9 — SHARED AND TRANSPARENT MODE TIMING



a) During Vertical Blank or after 'display off' command in shared mode only. See Figure 7 for transparent timing



b) After 'display off and 3-state' command

the other modes, but circuitry must be added to route the data from the display memory to the data bus inputs of the AVDC. Additionally, when not operating in row buffer mode, care must be taken to assure that the CPU does not attempt to access the AVDC while it is reading the row table. One way of preventing this is to latch prior to reading or writing the AVDC. The AVDC should only be accessed if the latch is low, indicating that the last line of the row is not active.

Figure 13 illustrates a typical hardware implementation for use in conjunction with independent and transparent modes, and Figure 14 shows the timing for row table operation.

OPERATION

After power is applied, the AVDC will be in an inactive state. Two consecutive "master reset" commands are necessary to release this circuitry and ready the AVDC for operation. Two register groups exist within the ADC; the initialization registers and the display control registers. The initialization registers select the system configuration, monitor timing, cursor shape, display memory domain, pointer address, scrolling region, double height and width condition, and screen format. These are loaded first and normally require no modification except for certain special visual

FIGURE 10 — ROW BUFFER MODE CONFIGURATION

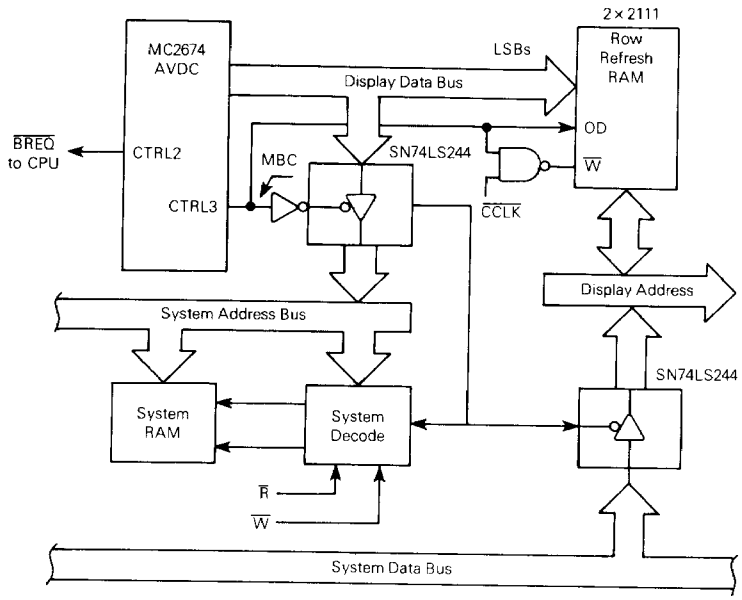
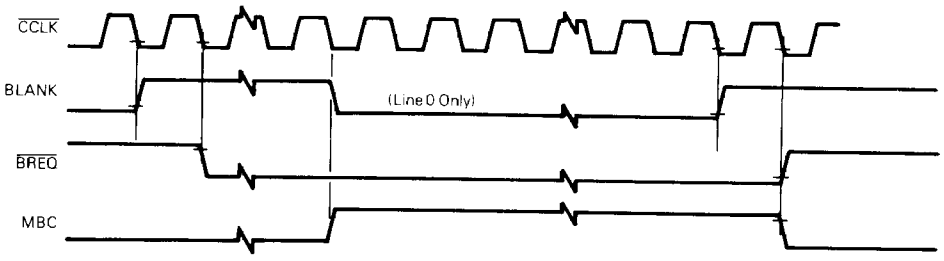


FIGURE 11 — ROW BUFFER MODE TIMING



NOTES:
1. If row table addressing is enabled, BREQ will be asserted at the middle of the last scan line of the prior row, and MBC will be asserted at the beginning of BLANK.
2. All voltage measurements are referenced to ground. All time measurements are at the 0.8 V to 2.0 V level for inputs and outputs. Input levels are 0.4 V to 2.4 V.

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FIGURE 12 — ROW TABLE ADDRESS FORMAT

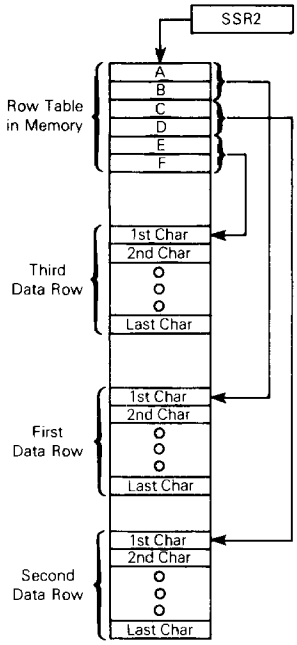


FIGURE 13 — ROW TABLE MODE CONFIGURATION (NON-ROW BUFFER MODES)

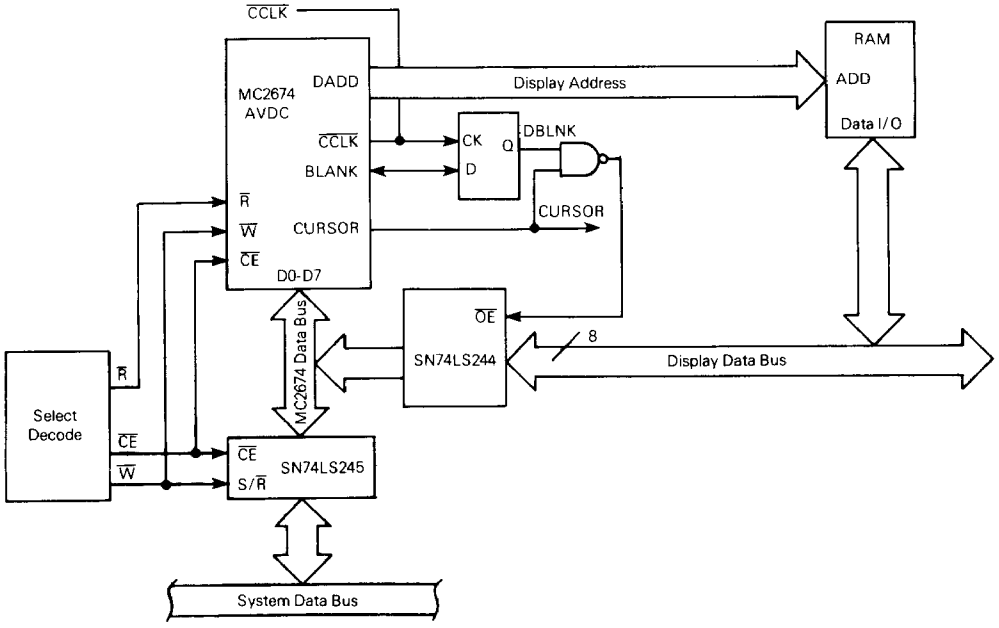
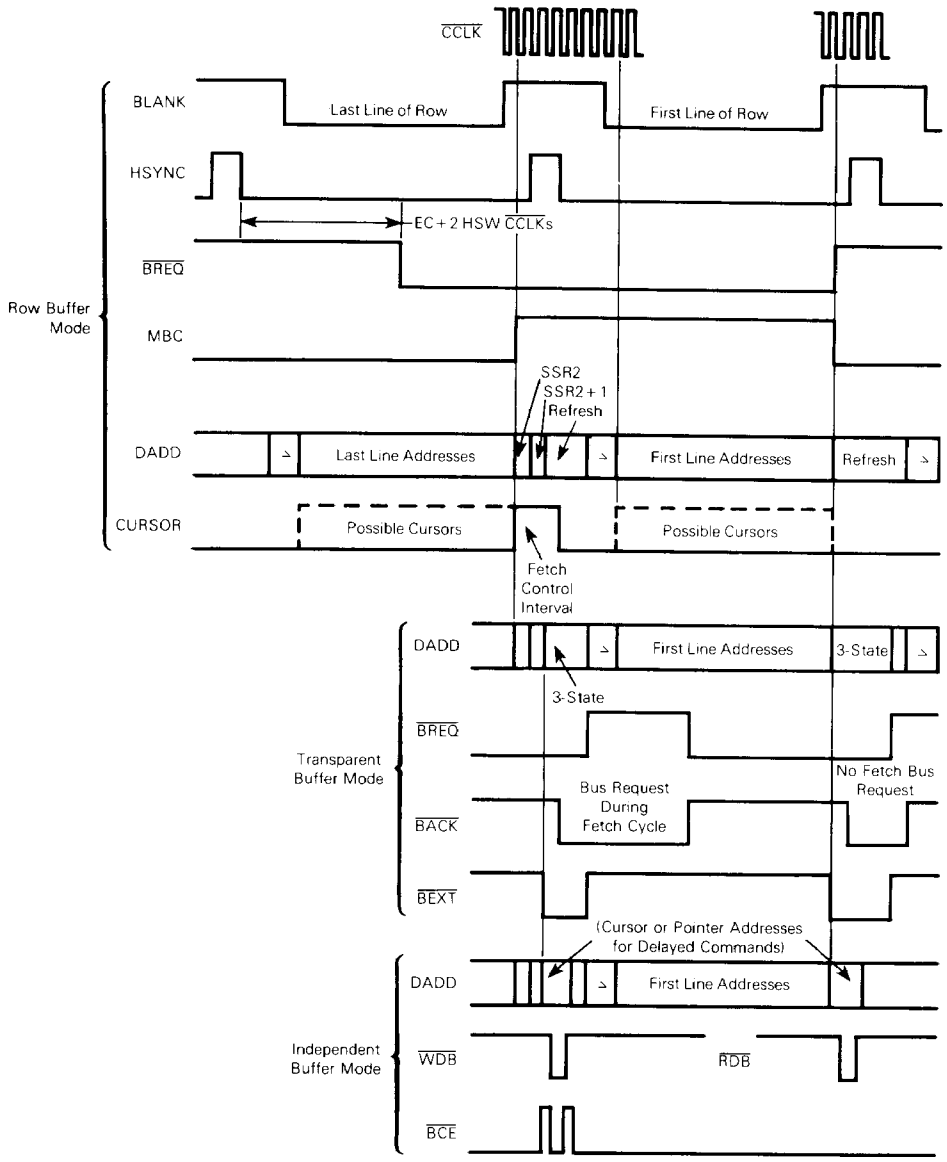


FIGURE 14 — ROW TABLE MODE TIMING



↘ = Multiplexed Control Signals
EC = Equalizing Constant
HSW = Horizontal SYNC Width

3

effects. The display control registers specify the memory address of the base character (upper left corner of screen), the cursor position, and the split screen addresses associated with the scrolling area or an alternate memory. These may require modification during operation.

After initial loading of the two register groups, the AVDC is ready to control the monitor screen. Prior to executing the AVDC commands which turn on the display cursor, the user should load the display memory with the first data to be displayed. During operation, the AVDC will sequentially address the display memory within the limits programmed into its registers. The memory outputs character codes to the system character and graphics generation logic, where they are converted to the serial video stream necessary to display the data on the CRT. The user effects changes to the CRT. The user effects changes to the display by modifying the contents of the display memory, the AVDC display control and command registers, and the initialization registers, if required. Interrupts and status conditions generated by the AVDC supply the "handshaking" information necessary for the CPU to effect real time display changes in the proper time frame if required.

INITIALIZATION REGISTERS

There are 15 initialization registers (IR0-IR14) which are accessed sequentially via a single address. The AVDC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR14) is accessed. The pointer then continues to point to IR14 for further accesses. Upon a power-on or a master reset command, the internal pointer reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the "load IR address pointer" command. These registers are write only and are used to specify parameters such as the system configuration, display format, cursor shape, and monitor timing. Register formats are shown in Figure 15.

3

FIGURE 15 — INITIALIZATION REGISTER FORMATS (Sheet 1 of 4)

IR0

7	6 5 4 3		2	1 0
Double Height/ Width	Scan Lines Per Character Row		Sync Select	Buffer-Mode Select
	Non-Interlaced	Interlaced		
	0000 = 1 Line 0001 = 2 Lines 0010 = 3 Lines • • 1110 = 15 Lines 1111 = 16 Lines	0000 = 2 Lines 0001 = 4 Lines 0010 = 6 Lines • • 1110 = 30 Lines 1111 = Undefined	0 = VSYNC 1 = CSYNC	00 - Independent 01 - Transparent 10 - Shared 11 - Row Buffer

IR1

7	6 5 4 3 2 1 0
Interlace Enable	Equalizing Constant
0 Non-Interlace 1 Interlace	0000000 = 1 $\overline{CCLK}$ 0000001 = 2 $\overline{CCLK}$ • • 1111110 = 127 $\overline{CCLK}$ 1111111 = 128 $\overline{CCLK}$ Calculated from: $EC = 0.5\,(H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}) - 2(H_{SYNC})$

IR2

7	6 5 4 3	2 1 0
Row Table	Horizontal Sync Width	Horizontal Back Porch
0 = Off 1 = On	0000 = 2 $\overline{CCLK}$ 0001 = 4 $\overline{CCLK}$ • • 1110 = 30 $\overline{CCLK}$ 1111 = 32 $\overline{CCLK}$	000 = Not Allowed 001 = 3 $\overline{CCLK}$ • • 110 = 23 $\overline{CCLK}$ 111 = 27 $\overline{CCLK}$

FIGURE 15 — INITIALIZATION REGISTER FORMATS (Sheet 2 of 4)

IR3

7	6	5	4	3	2	1	0
Vertical Front Porch			Vertical Back Porch				
000 = 4 Scan Lines 001 = 8 Scan Lines • • 110 = 28 Scan Lines 111 = 32 Scan Lines			00000 = 4 Scan Lines 00001 = 6 Scan Lines • • 11110 = 64 Scan Lines 11111 = 66 Scan Lines				

IR4

7	6	5	4	3	2	1	0
Character Blink Rate	Active Character Rows Per Screen						
0 = 1/64 VSYNC 1 = 1/128 VSYNC	0000000 = 1 Row 0000001 = 2 Rows • • • 1111110 = 127 Rows 1111111 = 128 Rows						

IR5

7	6	5	4	3	2	1	0
Active Characters Per Row							
00000010 = 3 Characters 00000011 = 4 Characters • • 11111110 = 255 Characters 11111111 = 256 Characters							

IR6

7	6	5	4	3	2	1	0
First Line of Cursor				Last Line of Cursor			
0000 = Scan Line 0 0001 = Scan Line 1 • • 1110 = Scan Line 14 1111 = Scan Line 15				0000 = Scan Line 0 0001 = Scan Line 1 • • 1110 = Scan Line 14 1111 = Scan Line 15			

IR7

7	6	5	4	3	2	1	0
Light Pen Line		Cursor Blink	Cursor Rate	Underline Position			
00 = Scan Line 3 01 = Scan Line 1 10 = Scan Line 5 11 = Scan Line 7		0 = Off 1 = On	0 = 1/32 1 = 1/64	0000 = Scan Line 0 0001 = Scan Line 1 • • 1110 = Scan Line 14 1111 = Scan Line 15			

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FIGURE 15 — INITIALIZATION REGISTER FORMATS (Sheet 3 of 4)

IR8

7	6	5	4	3	2	1	0
Display Buffer First Address LSBs							
H'000' = 0 H'001' = 1 • • H'FFE' = 4,094 H'FFF' = 4,095						NOTE: MSBs are in IR9[3:0]	

IR9

7	6	5	4	3	2	1	0
Display Buffer Last Address				Display Buffer First Address MSBs			
0000 = 1,023 0001 = 2,047 • • 1110 = 15,359 1111 = 16,383				See IR8			

IR10

7	6	5	4	3	2	1	0
Display Pointer Address Lower							
See IR11							

IR11

7	6	5	4	3	2	1	0
LZ Down	LZ Up	Display Pointer Address Upper					
0 = Off 1 = On	0 = Off 1 = On	H'0000' = 0 H'0001' = 1 • • H'3FFF' = 16,383					

IR12

7	6	5	4	3	2	1	0
Scroll Start	Split Register 1						
0 = Off 1 = On	0000000 = Row 1 0000001 = Row 2 • • 1111111 = Row 128						

FIGURE 15 — INITIALIZATION REGISTER FORMATS (Sheet 4 of 4)

IR13

7	6 5 4 3 2 1 0
Scroll End	Split Register 2
0 = Off 1 = On	0000000 = Row 1 0000001 = Row 2 • • 1111111 = Row 128

IR14

7 6	5 4	3 2 1 0
Double 1	Double 2	Lines to Scroll
00 = Normal 01 = Double Width 10 = Double Width and Tops 11 = Double Width and Bottoms	00 = Normal 01 = Double Width 10 = Double Width and Tops 11 = Double Width and Bottoms	0000 = 1 0001 = 2 • • 1110 = 15 1111 = 16

DOUBLE HEIGHT/WIDTH ENABLE (IR0[7]) — When this bit is set, the value in IR14[7:6] is used to control the double height and width conditions of each character row. Assertion of this bit also allows IR14[7:6] to be programmed in two ways:

1. By the CP writing to IR14 directly.
2. When the contents of screen start register 1 (SSR1) upper are changed, either by the CPU writing to this register or by the automatic loading of SSR1 when operating in row table mode, the two most significant bits of SSR1 upper are copied into IR14[7:6]. Thus, the most significant bits of each row table entry can be used to control double height and double width attributes on a row-by-row basis.

IR14[5:4] are not active when this bit is set. When this bit is reset, the double height and width attributes operate as described in IR[14].

SCAN LINES PER CHARACTER ROW (IR0[6:3]) — Both interlaced and non-interlaced scanning are supported by the AVDC. For interlaced mode, two different formats can be implemented, depending on the interconnection between the AVDC and the character generator (see IR1[7]). This field defines the number of scan lines used to compose a character row for each technique. As scanning occurs, the scan line count is output on the LA0-LA3 and ODD pins.

VSYNC/CSYNC (IR0[2]) — This bit selects either vertical sync pulses or composite sync pulses on the VSYNC/CSYNC output (pin 18). The composite sync waveform conforms to EIA RS170 standards, with the vertical interval composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses.

BUFFER MODE SELECT (IR0[1:0]) — Four buffer memory modes may be selectively enabled to accommodate the desired system configuration. See SYSTEM CONFIGURATIONS.

INTERLACE ENABLE (IR1[7]) — Specifies interlaced or non-interlaced timing operation. Two modes of interlaced operation are available, depending on whether L0-L3 or ODD, L0-L2 are used as the line address for the character generator. The resulting displays are shown in Figure 16.

For "interlaced sync" operation, the same information is displayed in both odd and even fields, resulting in enhanced readability. The AVDC outputs successive line numbers in ascending order on the LA0-LA3 lines, one per scan line for each field.

The "interlaced sync and video" format doubles the character density on the screen. The AVDC outputs successive line numbers in ascending order on the odd and LA0-LA2 lines, one per scan line for each field.

EQUALIZING CONSTANT (IR1[6:0]) — This field indirectly defines the horizontal front porch and is used internally to generate the equalizing pulses for the RS170 compatible CSYNC. The value for this field is the total number of character clocks ($\overline{CCLK}$s) during a horizontal line period divided by two, minus two times the number of character clocks in the horizontal sync pulse:

$$EC = \frac{H_{ACT} + H_{FP} + H_{SYNC} + H_{SP}}{2} - 2\,(H_{SYNC})$$

The definition of the individual parameters is illustrated in Figure 17.

Note that when using the attributes controller it will delay the blank pulse three $\overline{CCLK}$s relative to the HSYNC pulse.

ROW TABLE MODE ENABLE (IR2[7]) — Assertion/negation of this bit causes the AVDC to begin/terminate operating in row table mode starting at the next character row. See **ROW TABLE ADDRESS MODE.** By using the split interrupt capability of the AVDC, this mode can be enabled and disabled on a particular character row. This allows a combination of row table and sequential addressing to be utilized to provide maximum flexibility in generating the display.

HORIZONTAL SYNC PULSE WIDTH (IR2[6:3]) — This field specifies the width of the HSYNC pulse in $\overline{CCLK}$ periods.

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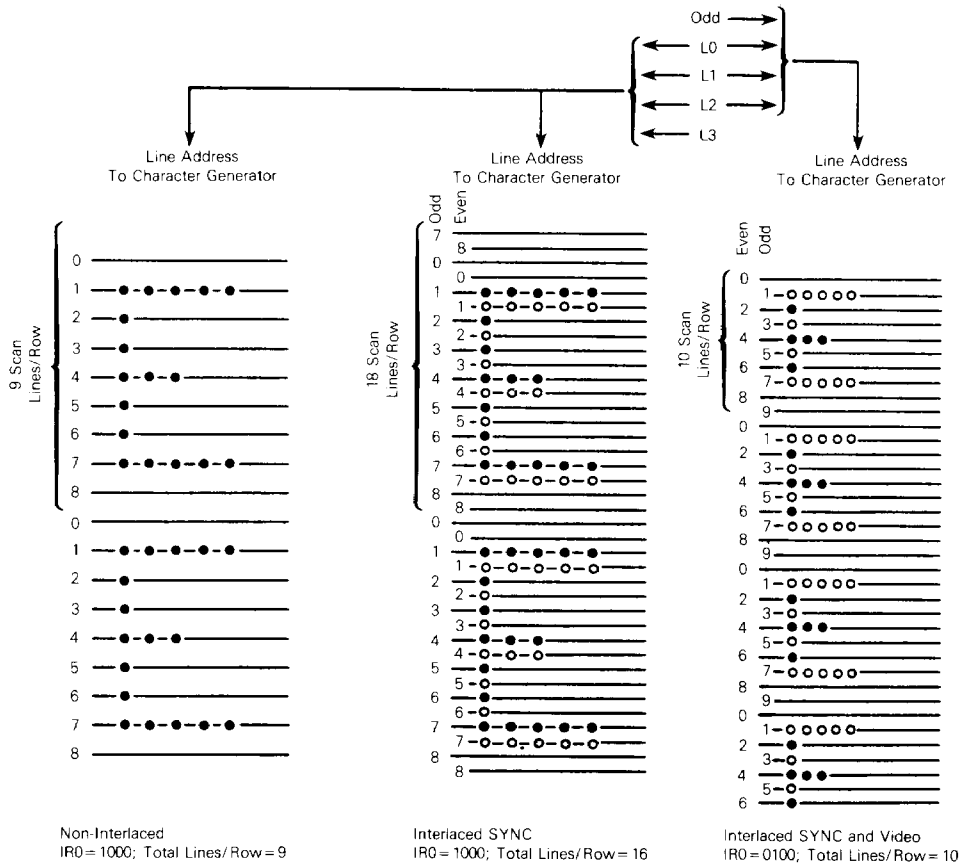
FIGURE 16 – INTERLACED DISPLAY MODES



Non-Interlaced
IR0 = 1000; Total Lines/Row = 9

Interlaced SYNC
IR0 = 1000; Total Lines/Row = 16

Interlaced SYNC and Video
IR0 = 0100; Total Lines/Row = 10

HORIZONTAL BACK PORCH (IR2[2:0]) — This field defines the number of $\overline{\text{CCLK}}$s between the trailing edge of HSYNC and the trailing edge of BLANK.

VERTICAL FRONT PORCH (IR3[7:3]) — This field specifies the number of scan line periods between the rising edges of BLANK and VSYNC during the vertical retrace interval. The vertical front porch is extended in increments of scan lines if the ACLL input is low at the end of the programmed value.

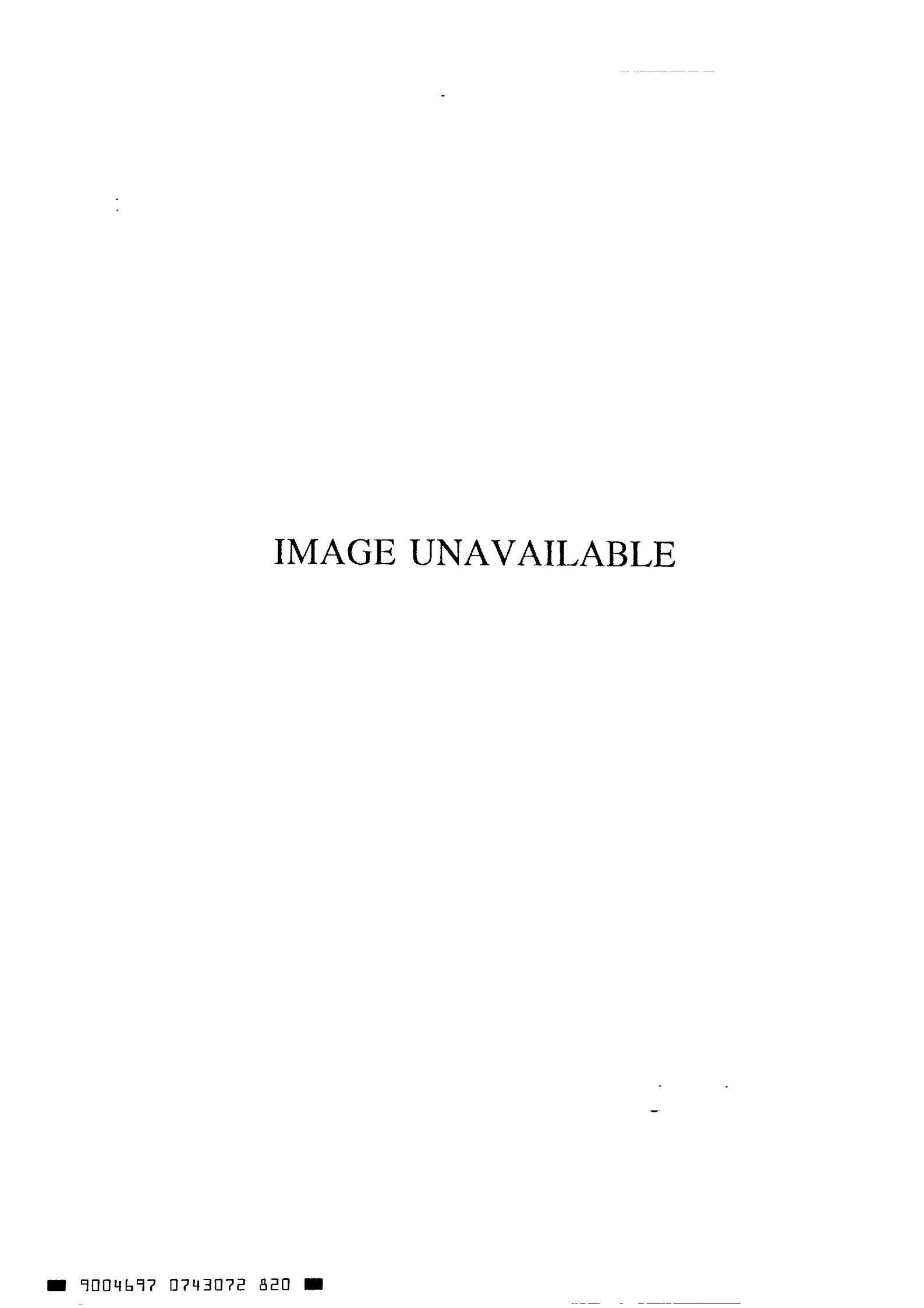
VERTICAL BACK PORCH (IR3[4:0]) — This field determines the number of scan line periods between the falling edges of the VSYNC and BLANK outputs.

CHARACTER BLINK RATE (IR4[7]) — Specifies the frequency for the character blink attribute timing. The blink rate can be specified as 1/64 or 1/128 of the vertical field rate. The timing signal has a duty cycle of 50% and is multiplexed onto the DADD1/BLINK output at the falling edge of each BLANK.

CHARACTER ROWS PER SCREEN (IR4[6:0]) — This field defines the number of character rows to be displayed. The value multiplied by the scan lines per characte row, plus the vertical front porch, the vertical back porch values, and the vertical sync pulse width is the vertical scan period in scan lines.

ACTIVE CHARACTERS PER ROW (IR5[7:0]) — This field determines the number of characters to be displayed on each row of the CRT screen. The sum of this value, the horizontal front porch, the horizontal sync width, and the horizontl back porch is the horizontal scan period in CCLKs.

FIRST AND LAST SCAN LINE OF CURSOR (IR6[7:4], IR6[3:0]) — These two field specify the height and position of the cursor on the character block. The "first" line is the topmost line when scanning from the top to the bottom of the screen.



DISPLAY CONTROL REGISTERS

There are seven registers in this group, each with an individual address. Their formats are illustrated in Figure 18. The command register is used to invoke one of 19 possible AVDC commands as described in COMMANDS. The remaining registers in the group store address values which specify the cursor location, the location of the first character to be be displayed on the screen, and any split screen address locations. The user initializes these registers after powering on the system and changes their values to control the data which is displayed.

SCREEN START REGISTERS 1 AND 2

The screen start 1 registers contain the address of the first character of the first row (upper left corner of the active display). At the beginning of the first scan line of the first row, this address is transferred to the row start register (RSR) and into the memory address counter (MAC). The counter is then advanced sequentially at the character clock rate for the number of times programmed into the active characters per row register (IR5), thus reaching the address of the last character of the row plus one. At the beginning of each subsequent scan line of the first row, the MAC is reloaded from the RSR and the above sequence is repeated. At the end of the last scan line of the first row, the contents of the MAC is loaded into the RSR to serve as the starting memory address for the second character row. This process is repeated for the programmed number of rows per screen. Thus, the data in the display memory is displayed sequentially starting from the address contained in the screen start register. After the ensuing vertical retrace interval, the entire process repeats again.

During vertical blanking, the address counter operation is modified by stopping the automatic load of the contents of the RSR into the counter, thereby allowing the address outputs to free-run. This allows dynamic memory refresh to occur during the vertical retrace interval. The refresh addressing starts at the last address displayed on the screen and increments by one for each character clock during the retrace interval. If the display buffer last address is encountered, refreshing continues from the display buffer first address.

The sequential operation described above will be modified upon the occurrence of any of three events. First, if during the incrementing of the memory address counter the "display buffer last address" (IR9[7:4]) is reached, the MAC will be loaded from the "display buffer first address" register (IR9[3:0] and IR8[7:0]) at the next character clock. Sequential operation will then resume starting from this address. This wraparound operation allows portions of the display buffer to be used for purposes other than storage of displayable data and is completely automatic without any CPU intervention (see Figure 19a).

The sequential row to row addressing can also be modified via split register 1 (IR12) and split register 2 (IR13), under CPU control, or by enabling the row table addressing mode. If bit 6 of screen start register 2 upper (SPL1) is set, the screen start register 2 contents will be loaded automatically into the RSR at the beginning of the first scan line of the row designated by split register 1 (IR12[6:0]). If bit 7 of screen start 2 upper (SPL2) is set, the screen start register 2 contents is automatically loaded into the RSR at the end of the last scan line of the row designated by split register 2 (IR13[6:0]). SPL1 and SPL2 are write only bits and will read as zero when reading screen start register 2.

If the contents of screen start register 1 (upper, lower, or both) are changed during any character row (e.g., row 'n'), the starting address of the next character row (row 'n+1') will be the new value of the screen start register and addressing will continue sequentially from there. This allows features such as split screen operation, partial scroll, or status line display to be implemented. The split screen interrupt feature of the AVDC is useful in controlling the CPU initiated operations. Note that in order to obtain the correct screen display, screen start register 1 must be reloaded with the original (origin of display) value prior to the end of the vertical retrace. See Figure 19b.

3

FIGURE 18 – DISPLAY CONTROL REGISTER FORMATS (Sheet 1 of 2)

7	6	5	4	3	2	1	0
Command Code							
See **COMMANDS** for Command Codes							

Command Registers (Write Only)

7	6	5	4	3	2	1	0
		Upper Register					
DADD15	DADD14	Most Significant Bits					

FIGURE 18 — DISPLAY CONTROL REGISTER FORMATS (Sheet 2 of 2)

7	6	5	4	3	2	1	0
Lower Register (Least Significant Bit)							
H'0000' = 0 H'0001' = 1 Through H'3FFE' = 16,382 H'3FFF' = 16,383			NOTE: Most significant bits are in upper register [5:0]				

NOTES:
1. Bits 7 and 6 of upper register are not used in the cursor address register.
2. Bits 7 and 6 of upper register are always zero when read by the CPU.
3. When IR0[7] = 1, the values written into bits 7 and 6 of screen start 1 upper will also be written into IR14[7:6] to control the double width and double height attributes of the display as follows:

7	6	Attribute
0	0	None
0	1	Double Width Only
1	0	Double Width and Double Height Tops
1	1	Double Width and Double Height Bottoms

Screen Start 1 Register (Read and Write) and Cursor Address Registers (Read and Write)

7	6	5	4	3	2	1	0
		Upper Register					
SPL2 0 = Off 1 = On	SPL1 0 = Off 1 = On	Most Significant Bits					

7	6	5	4	3	2	1	0
Lower Register (Least Significant Bit)							
H'0000' = 0 H'0001' = 1 Through H'3FFE' = 16,382 H'3FFF' = 16,383			NOTE: Most significant bits are in upper register [5:0]				

NOTE:
Bit 7 and bit 6 are always zero when read by the CPU.

Screen Start 2 Registers (Read and Write)

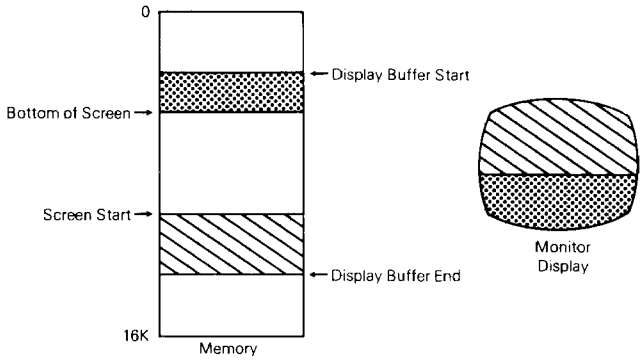
When row table addressing mode is enabled, the first address of the row table is designated in SSR2. The AVDC fetches the next row's starting address from the table during the blanking interval prior to the first scan line of each character row and loads it into SSR1 for use as the starting address of the next row. Since the contents of SSR2 changes as the table entries are fetched, it must be re-initialized to point to the first table entry during each vertical retrace interval.

The values of the two most significant bits of SSR1 upper are multiplexed onto the DADD1/DADD14 and DADD2/DADD15 outputs during the falling edge of BLANK. If IR0[7] = 0, these two bits act as memory page select bits which may be used to extend the display memory addressing range of the AVDC up to 64K. In that case, these two bits act as a two-bit counter which is incremented each time that "wraparound" occurs (see above). Note that the counter is incremented at the falling edge of BLANK and that for proper display operation the wraparound address should be programmed to occur at the last character position of a row. Also, the first address accessed in the new page will be the address contained in the display buffer first address register (IR9[3:0] and IR8[7:0]).

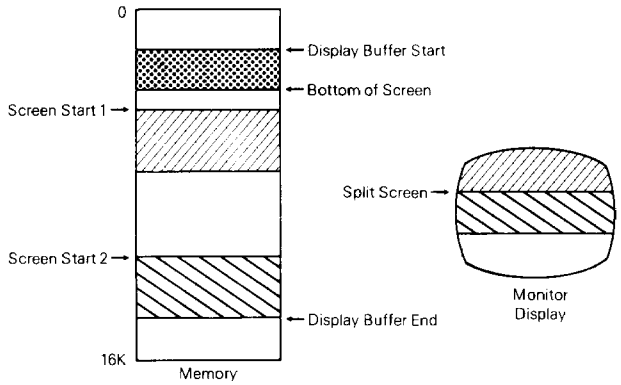
CURSOR ADDRESS REGISTERS

The contents of these registers define the buffer memory address of the cursor. The cursor output will be asserted when the memory address counter matches the value of the

FIGURE 19 – DISPLAY ADDRESSING OPERATION



(a) Display Memory Wraparound



(b) Display Memory Split Screen With Wraparound

cursor address registers for the scan lines specified in IR6. The cursor address registers can be read or written by the CPU or incremented via the "increment cursor address" command. In independent buffer mode, these registers define a buffer memory address for AVDC controlled access in response to "read/write at cursor with/without increment" commands, or the first address to be used in executing the "write from cursor to pointer" command.

INTERRUPT/STATUS REGISTERS

The interrupt and status registers provide information to the CPU to allow it to interact with the AVDC to effect desired changes that implement various display operations. The interrupt register provides information on five display operations. The interrupt register provides information on five possible interrupt conditions, as shown in Figure 20. These conditions can be selectively enabled or disabled (masked) from causing interrupts by certain AVDC commands. An interrupt condition which is enabled (masked bit equal to one) will cause the $\overline{INTR}$ output to be asserted and will cause the corresponding bit in the interrupt register to be set upon the occurrence of the interrupting condition. An interrupt condition which is disabled (mask bit equal to zero) has no effect on either the $\overline{INTR}$ output or the interrupt register.

The status register provides six bits of status information: the five possible interrupt conditions plus the RDFLG bit. For this register, however, the contents are not affected by the state of the mask bits.

Descriptions of each interrupt/status register bit follow. Unless otherwise indicated, a bit, once set, will remain set until reset by the CPU by issuing a "reset interrupt/status bits" command. The bits are also reset by a "master reset" command and upon power-up.

FIGURE 20 — INTERRUPT AND STATUS REGISTER FORMAT

7	6	5	4	3	2	1	0
		RDFLG	VBLANK	Line Zero	Split 1	Ready	Split 2
Not Used Always Read as 0		0 = Busy 1 = Ready	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Busy 1 = Ready	0 = No 1 = Yes

RDFLG (I/SR[5]) — This bit is present in the status register only. A zero indicates that the AVDC is currently executing the previously issued delayed command. A one indicates that the AVDC is ready to accept a new delayed command.

VBLANK (I/SR[4]) — Indicates the beginning of a vertical blanking interval. Set to one at the beginning of the first scan line of the vertical front porch.

LINE ZERO (I/SR[3]) — Set to one at the beginning of the first scan line (line 0) of each active character row.

SPLIT SCREEN 1 (I/SR[2]) — This bit is set when a match occurs between the current character row number and the value contained in split register 1, IR12[6:0]. The equality condition is only checked at the beginning of line zero of each character row.

READY (I/SR[1]) — The delayed commands affect the display and may require the AVDC to wait for a blanking interval before enacting the command. This bit is set to one when execution of a delayed command has been completed. No other delayed command should be invoked until the prior delayed command is completed.

SPLIT SCREEN 2 (I/SR[0]) — This bit is set when a match occurs between the current character row number and the value contained in split register 2 (IR13[6:0]).

COMMANDS

The AVDC commands are divided into two classes: the instantaneous commands which are executed immediately after they are invoked, and the delayed commands which may need to wait for a blanking interval prior to their execution. Command formats are shown in Table 3. The commands are asserted by performing a write operation to the command register with the appropriate bit pattern as the data byte.

TABLE 3 — AVDC COMMAND FORMATS

D7	D6	D5	D4	D3	D2	D1	D0	Hex	Command
Instantaneous Commands									
0	0	0	0	0	0	0	0		Master Reset
0	0	0	1	V	V	V	V		Load IR Pointer with Value V (V = 0 to 14)
0	0	1	d	d	d	1	0*		Disable Graphics
0	0	1	d	d	d	1	1*		Enable Graphics
0	0	1	d	1	N	d	0*		Display Off — Float DADD Bus if N = 1
0	0	1	d	1	N	d	1*		Display On — Next Field (N = 1) or Scan Line (N = 0)
0	0	1	1	d	d	d	0*		Cursor Off
0	0	1	1	d	d	d	1*		Cursor On
0	1	0	N	N	N	N	N		Reset Interrupt/Status: bit Reset where N = 1
1	0	0	N	N	N	N	N		Disable Interrupt: Disable where N = 1
0	1	1	N	N	N	N	N		Enable Interrupt: Enables Interrupts where N = 1
			V B	L Z	S P 1	R D Y	S P 2		Interrupt Bit Assignments
Delayed Commands									
1	0	1	0	0	1	0	0	A4	Read at Pointer Address
1	0	1	0	0	0	1	0	A2	Write at Pointer Address
1	0	1	0	1	0	0	1	A9	Increment Cursor Address
1	0	1	0	1	1	0	0	AC	Read at Cursor Address
1	0	1	0	1	0	1	0	AA	Write at Cursor Address
1	0	1	0	1	1	0	1	AD	Read at Cursor Address and Increment Address
1	0	1	0	1	0	1	1	AB	Write at Cursor Address and Increment Address
1	0	1	1	1	0	1	1	BB	Write from Cursor Address to Pointer Address
1	0	1	1	1	1	0	1	BD	Read from Cursor Address to Pointer Address

NOTES:
*Any combination of these three commands is valid.
d = Don't care.

INSTANTANEOUS COMMANDS

The instantaneous commands are executed immediately after the trailing edge of the write pulse during which the command is issued. These commands do not affect the state of the RDFLG or READY interrupt/status bits and can be invoked at any time.

MASTER RESET

This command initializes the AVDC and can be invoked at any time to return the AVDC to its initial state. Upon power-up, two successive master reset commands must be applied to release the AVDC's internal power-on circuits. In transparent and shared buffer modes, the CTRL1 input must be high when the command is issued. The command causes the following:

1. VSYNC and HSYNC are driven low for the duration of the command and BLANK goes high. After command completion, HSYNC and VSYNC will begin operation and BLANK will remain high until a "display on" command is received.
2. The interrupt and status bits and masks are set to zero, except for the RDFLG flag which is set to a one.
3. The row buffer mode, cursor-off, display-off, and line graphics disable states are set.
4. The initialization register pointer is set to address IR0.
5. IR2[7] is reset.

LOAD IR ADDRESS

This command is used to preset the initialization register pointer with the value "V" defined by D3-D0. Allowable values are 0 to 14.

ENABLE GRAPHICS

After invoking this command, the AVDC will increment the MAC to the next consecutive memory address for each scan line even if more than one scan line per row is programmed. This mode can be used for bit-mapped graphics where each location in the display buffer within the defined area contains the bit pattern to be displayed. This command is row buffered and should be asserted during the character row prior to the row where this feature is required. This allows the user to enter and exit graphics mode on character row boundaries.

To perform split screen operations while in graphics mode use SSR2 only.

DADD0/LG is asserted during the trailing edge of BLANK for each scan line while this mode is active.

DISABLE GRAPHICS

Normal addressing resumes at the next row boundary.

DISPLAY OFF

Asserts the BLANK output. The DADD0 through DADD13 display address bus outputs can be optionally placed in the three-state condition by setting bit 2 to a one when invoking the command.

DISPLAY ON

Restores normal blanking operation either at the beginning of the next field (bit 2 = 1) or at the beginning of the next scan line (bit 2 = 0). Also returns the DADD0-DADD13 drivers to their active state.

CURSOR OFF

Disables cursor operation. Cursor output is placed in the low state.

CURSOR ON

Enables normal cursor operation.

RESET INTERRUPT/STATUS BITS

This command resets the designated bits in the interrupt and status registers. The bit positions correspond to the bit positions in the registers:

Bit 0 – Split 2
Bit 1 – Ready
Bit 2 – Split 1
Bit 3 – Line Zero
Bit 4 – Vertical Blank

DISABLE INTERRUPTS

Sets the interrupt mask to zeros for the designated conditions, thus disabling these conditions from being set in the interrupt register and asserting the INTR output. Bit position correspondence is as above.

ENABLE INTERRUPTS

This command writes the associated interrupt mask bit to a one. This enables the corresponding conditions to be set in the interrupt register and asserts the INTR output. Bit position correspondence is as above.

DELAYED COMMANDS

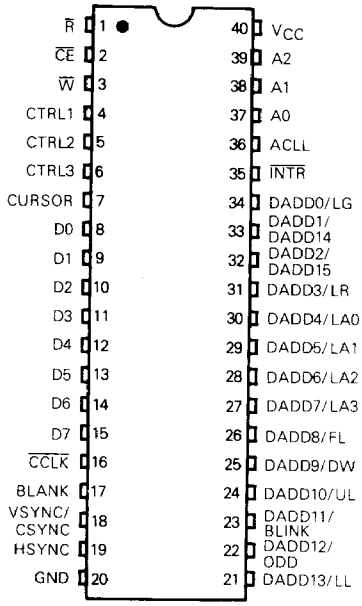
This group of commands is utilized for the independent buffer mode of operation, although the "increment cursor" command can also be used in other modes. With the exception of the "write from cursor to pointer" and "increment cursor" commands, all the commands of this type will be executed immediately or will be delayed depending on when the command is invoked. If invoked during the active screen time, the command is executed at the next horizontal blanking interval. If invoked during a vertical retrace interval or a "display off" state, the command is executed immediately.

The "increment cursor" command is executed immediately after it is issued and requires approximately three $\overline{CCLK}$ periods for completion. The "write from cursor to pointer" command executes during blanking intervals. The AVDC will execute as many writes as possible during each blanking interval. If the command is not completed during the current blanking interval, the command will be held in suspension during the next active portion of the screen and continues during the next blanking interval until the command is completed.

ORDERING INFORMATION (V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

Package Type	Frequency	Order Number
Plastic	2.7 MHz	MC2674B3P
P Suffix	4.0 MHz	MC2674B4P

PIN ASSIGNMENT



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