MN7145 Series

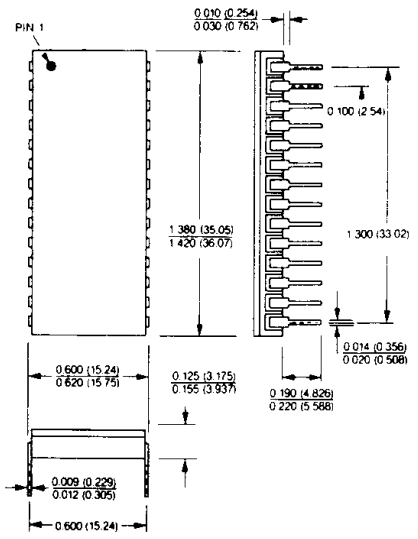
MICRO NETWORKS

8-CHANNEL, 12-Bit
DATA ACQUISITION SYSTEM
with μP INTERFACE

FEATURES

- **Complete, 8-Channel, 12-Bit DAS with MUX, T/H, ADC, Ref. and 3-State Output**
- **25,000 Channels/sec Guaranteed Throughput**
- **Microprocessor Interface (3-State Output, Address Line, Read/Convert, etc.)**
- **Small 28-Pin Side-Brazed DIP**
- **18 Models (3 Input Voltage Ranges)**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

28 PIN DIP



Dimensions In Inches (millimeters)

DESCRIPTION

The MN7145, MN7146 and MN7147 are complete, single-package, 8-channel, 12-bit, data acquisition systems with internal decoding logic and 3-state output buffers which greatly facilitate microprocessor control. Packing a lot of function into a 28-pin, side-brazed, ceramic DIP, MN7145 Series DAS's each contain an 8-channel, overvoltage protected (±35V) multiplexer; a high-speed (10μsec), high-impedance ($10^{10}\Omega$), T/H amplifier; a high-speed (25μsec), 12-bit A/D with reference and clock; and all the timing and control logic (3-state buffer, address line, read/convert line) necessary for μP control. System throughput rate is guaranteed at 25,000 channels/sec for full rated accuracy.

These devices are manufactured using contemporary hybrid assembly techniques, and they illustrate the technology's ability to combine I.C.'s made with different processing technologies into a single functional design that takes advantage of the best aspects of each semiconductor technology. The overvoltage protected mux is CMOS. The T/H is high-speed bipolar with an npo hold cap. The A/D combines high-speed bipolar technology with state-of-the-art thin-film technology and TTL compatible CMOS. Active laser trimming of fully assembled devices compensates for summed accuracy and linearity errors to produce overall system linearity (±½LSB) and accuracy (±0.05%FSR offset error) that may not be achievable when assembling a similar system with individual components. Small size, low power (1 Watt max), high sampling rate and low cost may make the MN7145 Series the most economical way possible to achieve multichannel, 12-bit, data acquisition today.

MN7145 (0 to +10V input range), MN7146 (±5V) and MN7147 (±10V) are fully specified over both 0°C to +70°C (J and K models) and −55°C to +125°C (S and T models) temperature ranges. Assorted linearity grades (± ½LSB, ±1LSB) at room temperature and over temperature are available as outlined in the specification table. All devices guarantee "no missing codes" over temperature (to either the 12-bit or 11-bit level).

February 1988

MICRO NETWORKS
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MN7145 SERIES 8-CHANNEL, 12-Bit, DATA ACQUISITION SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
J and K Models	0°C to +70°C
S, S/B, T, T/B Models	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 19)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 7)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 6)	0 to +7 Volts
Digital Inputs (Pins 3, 4, 8-10)	−0.5 to (+Vdd +0.5) Volts
Analog Inputs: (Pins 11-18)	±Vcc ±20V
(Pins 20, 21)	±Vcc

ORDERING INFORMATION

PART NUMBER — **MN714XX/B CH**

- Select MN7145 (0 to +10V), MN7146(±5V) or MN7147(±10V)
- Select suffix J,K,S or T for desired performance and specified temperature range.
- Add "/B" to "S" or "T" models for Environmental Stress Screening
- Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels		8 Single-Ended		
Input Voltage Ranges: MN7145 MN7146 MN7147		0 to +10 ±5 ±10		Volts Volts Volts
Input Impedance (Note 2): On Channel Off Channels		10^{10} / 100 10^{10} / 10		Ω/pF Ω/pF
Input Bias Current (On Channel): +25°C (Note 2) T_{min} to T_{max} (Note 3)		±1 ±50	 ±250	nA nA
Input Leakage Current (Off Channels, Note 2): +25°C T_{min} to T_{max} (Note 3)		±1 ±50		nA nA
DIGITAL INPUTS				
Logic Levels: A_0, R/$\overline{C}$: Logic "1" Logic "0" MA_0-MA_2 (Note 4): Logic "1" Logic "0"	+2.4 −0.5 +4.0 0		+5.5 +0.8 +5.5 +0.8	Volts Volts Volts Volts
Logic Currents (All Inputs): Logic "1" Logic "0"			±10 ±10	μA μA
DIGITAL OUTPUTS (Status, DBO-DB11)				
Output Coding (Note 5): Unipolar Ranges Bipolar Ranges		Straight Binary Offset Binary		
Logic Levels: Logic "1" ($I_{source} \leq 500\mu A$) Logic "0" ($I_{sink} \leq 1.6mA$)	+2.4		 +0.4	Volts Volts
Leakage (DBO-DB11) in High-Z State		±1	±10	μA
Output Capacitance (Note 2)		5		pF
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supplies +V_{dd} Supply	±13.5 +4.5	±15 +5	±16.5 +5.5	Volts Volts
Power Supply Rejection (Note 6): +V_{CC} Supply −V_{CC} Supply +V_{dd} Supply		±0.002 ±0.002 ±0.002	±0.005 ±0.005 ±0.005	%FSR/% Supply %FSR/% Supply %FSR/% Supply
Current Drains: +V_{CC} Supply −V_{CC} Supply +V_{dd} Supply		+18 −26 +10	+25 −35 +20	mA mA mA
Power Consumption		710	1000	mW
DYNAMIC CHARACTERISTICS				
Conversion Time (Note 7): 12-Bit Conversion 8-Bit Conversion		20 13	25 17	μsec μsec
Throughput Rate	25	35		kHz

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, ±Vcc = ±15V, + Vdd = +5V unless otherwise indicated) (Note 8)

MODEL	MN7145J MN7146J MN7147J	MN7145K MN7146K MN7147K	MN7145S MN7146S MN7147S	MN7145T MN7146T MN7147T	UNITS
Integral Linearity Error:					
Initial (+25°C) (Maximum)	±1	±½	±1	±½	LSB
T_{min} to T_{max} (Maximum, Note 3)	±1	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed:					
Initial (+25°C)	11	12	11	12	Bits
T_{min} to T_{max} (Note 3)	11	12	11	12	Bits
Unipolar Offset Error (Notes 9,10):					
Initial (+25°C) (Maximum)	±0.05	±0.05	±0.05	±0.05	% FSR
Drift (Maximum)	±15	±10	±25	±20	ppm of FSR/°C
Bipolar Offset Error (Notes 9,11):					
Initial (+25°C) (Maximum)	±0.25	±0.1	±0.25	±0.1	% FSR
Drift (Maximum)	±25	±20	±25	±20	ppm of FSR/°C
Gain Error (Notes 9,12):					
Initial (+25°C) (Maximum)	±0.3	±0.3	±0.3	±0.3	%
Drift (Maximum)	±50	±25	±50	±25	ppm/°C

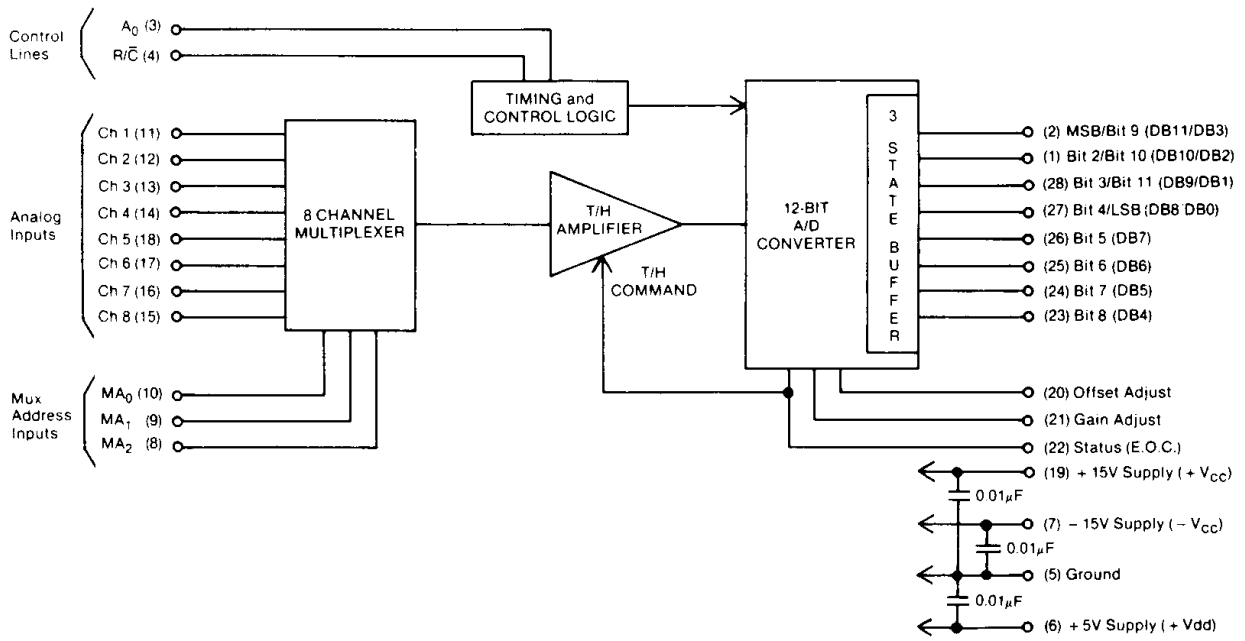
SPECIFICATION NOTES:

1. Detailed timing specifications appear in the Timing sections of this data sheet. FSR = Full Scale Range. MN7145 (0 to +10V input voltage range) and MN7146 (±5V input voltage range) have a 10V FSR. MN7147 (±10V input voltage range) has a 20V FSR.
2. These parameters are listed for reference only and are not tested.
3. J and K models are fully specified for 0°C to +70°C operation. S, S/B, T and T/B models are fully specified for −55°C to +125°C operation. See ordering information.
4. If the multiplexer inputs are driven from standard TTL logic, 1kΩ pullup resistors to +5V should be used.
5. See table of transition voltages in section labeled Digital Output Coding.
6. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
7. Whenever the Status Output (pin 22) is low (logic "0"), the internal T/H is in the track mode and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
8. All performance specifications are specified and tested while sampling and converting at a 25kHz throughput rate.
9. Adjustable to zero with external potentiometer.
10. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN7145 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
11. Bipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN7146 or MN7147 on a bipolar range. The ideal value at which this transition should occur is −F.S. +½LSB. See Digital Output Coding.
12. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

BLOCK DIAGRAM

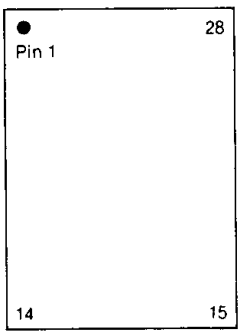


ORDERING INFORMATION

Part Number	Input Voltage Range	Specified Temp. Range	Integral Linearity (1) +25°C	Integral Linearity (1) Temp.	No Missing Codes Over Temp.	Guaranteed Throughput Rate (Channels/sec)	Package
MN7145J	0 to +10V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145K	0 to +10V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7145S	0 to +10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145S/B (2)	0 to +10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7145T	0 to +10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7145T/B (2)	0 to +10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7146J	±5V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146K	±5V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7146S	±5V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146S/B (2)	±5V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7146T	±5V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7146T/B (2)	±5V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7147J	±10V	0°C to +70°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147K	±10V	0°C to +70°C	±½	±½	12 Bits	25,000	28-Pin DIP
MN7147S	±10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147S/B (2)	±10V	−55°C to +125°C	±1	±1	11 Bits	25,000	28-Pin DIP
MN7147T	±10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP
MN7147T/B (2)	±10V	−55°C to +125°C	±½	±1	12 Bits	25,000	28-Pin DIP

1. Maximum error expressed in LSB's for 12 bits.
2. Includes 100% screening to MIL-STD-883.

PIN DESIGNATIONS



1 Bit 2/Bit 10 (DB10/DB2)
2 MSB/Bit 9 (DB11/DB3)
3 Address Line (A_0)
4 Read/Convert (R/$\overline{C}$)
5 Ground
6 +5V Supply (+V_{dd})
7 −15V Supply (−V_{CC})
8 Mux Address A_2 (MA_2)
9 Mux Address A_1 (MA_1)
10 Mux Address A_0 (MA_0)
11 Channel 1 Input
12 Channel 2 Input
13 Channel 3 Input
14 Channel 4 Input
28 Bit 3/Bit 11 (DB9/DB1)
27 Bit 4/LSB (DB8/DB0)
26 Bit 5 (DB7)
25 Bit 6 (DB6)
24 Bit 7 (DB5)
23 Bit 8 (DB4)
22 Status (E.O.C.)
21 Gain Adjust
20 Offset Adjust
19 +15V Supply (+V_{CC})
18 Channel 5 Input
17 Channel 6 Input
16 Channel 7 Input
15 Channel 8 Input

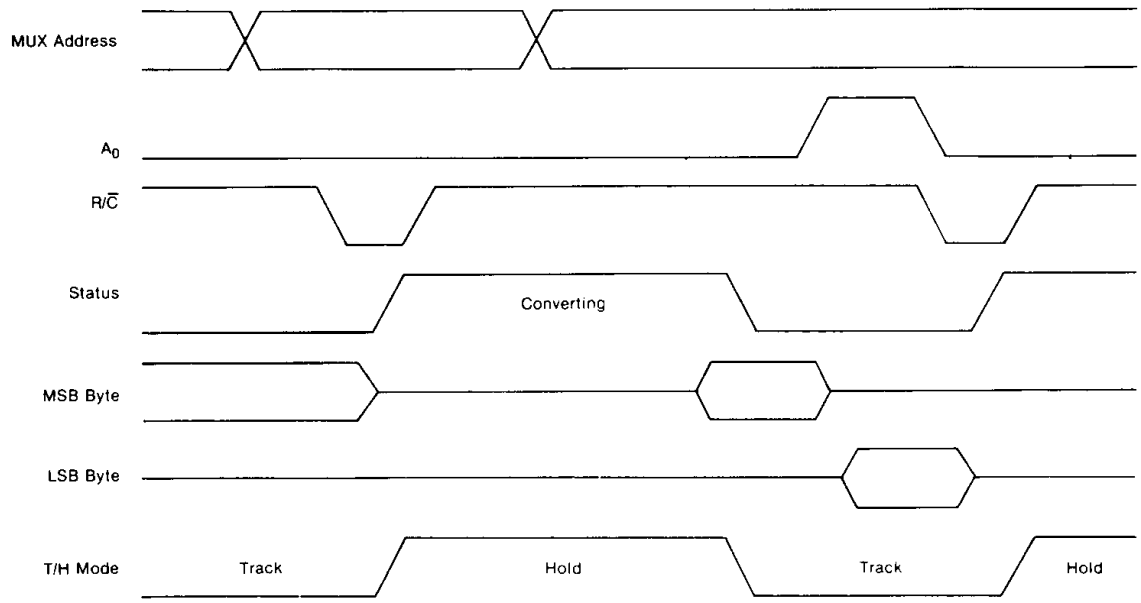
APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — MN7145 Series devices are 8-channel, 12-bit, data acquisition systems with internal 8-channel multiplexer, track-hold (T/H) amplifier, 12-bit analog-to-digital (A/D) converter, and microprocessor interface logic (3-state buffer, address line, read/convert line). A minimal amount of signals need to be supplied externally to these devices in order to achieve true multichannel data acquisition. High input impedance and low input bias currents allow analog signal sources to be connected directly to the multiplexer inputs. Multiplexer channels are randomly selected via three mux address lines (MA_0, MA_1, MA_2). The T/H is controlled directly by the A/D and requires no external commands. The address (A_0) and read/convert (R/$\overline{C}$) lines are used in assorted combinations to: initiate (write) 12-bit conversions, initiate 8-bit conversions, read back MSB data and read back LSB data. In normal operation, a mux address is selected (000 = channel 1, 111 = channel 8), and time must be allowed for the mux to switch and settle and for the T/H to acquire and track the new analog input signal. Then the A/D conversion is initiated by dropping the R/$\overline{C}$ line. Once a conversion has been initiated, the device's Status output (pin 22) rises to a logic "1" signaling that a conversion is in progress. This action drives the T/H into the hold mode instantaneously "freezing" the appropriate analog input and holding it constant while the A/D conversion proceeds. When the conversion is complete, Status drops back to a logic "0"; the T/H is driven back into the track mode; and output data is held in a 3-state buffer ready to be read. At this point, output data is available in two 8-bit bytes (multiplexed on a single set of output lines) and can be enabled by bringing R/$\overline{C}$ high and toggling A_0 (A_0 = "0" enables MSB data byte; A_0 = "1" enables LSB data byte). If R/$\overline{C}$ is brought high during a conversion, output data is automatically enabled when the conversion is complete. The output data lines return to the high-impedance state when R/$\overline{C}$ is brought low initiating a new conversion.

The multiplexer address can be changed during or after a conversion. In order to achieve maximum device performance, the multiplexer address may be changed 1μsec after initiating a conversion. If the multiplexer is updated in this fashion, and a new channel is selected while a conversion is in process, the T/H will immediately start to acquire and track

the new analog input signal when the conversion is complete. This allows the microprocessor to read output data while the T/H is acquiring the next analog input signal. The diagram below illustrates the relationships of the timing signals previously discussed. For more detailed timing information, see the timing section of this data sheet.

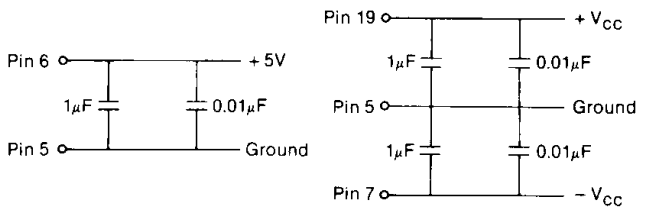
TIMING DIAGRAM



LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and decoupling is necessary to obtain specified accuracy from MN7145 Series devices. It is critically important that the devices' power supplies be filtered, well-regulated and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power-supply pins; the supply decoupling capacitors should be connected directly from Vdd (pin 6), + Vcc (pin 19) and − Vcc (pin 7) to Ground (pin 5). Suitable decoupling capacitors are 1μF tantalum types in parallel with 0.01μF ceramic discs. See diagram below.

POWER SUPPLY DECOUPLING



Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Analog input runs should be well separated from digital clock lines and other noise sources. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to the device as possible. If external adjustment potentiometers are not used, Offset Adjust (pin 20) and Gain Adjust (pin 21) should be left open. Do not ground.

Ground (pin 5) should be connected to system analog ground as close to the unit as possible, preferably through a large analog ground plane beneath the package.

CONTROL FUNCTIONS—Operating MN7145 Series devices under microprocessor control is most easily understood by examining the control-line funtions in a truth table. Table 1 below is a summary of the control-line functions. Table 2 is the control-line truth table.

Table 1: MN7145 Series Control Line Functions

Pin Designations	Definition	Function
MA_0-MA_2 (Pins 8-10)	MUX Address In	Selects MUX channel to be held and converted.
R/C̄ (Pin 4)	Read/Convert ("1" = Read) ("0" = Convert)	R/C̄ 1−0 edge is used to initiate 8 or 12-bit conversions. R/C̄ = "1" enables output data during a read cycle.
A_0 (Pin 3)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data, A_0 selects the output data format. A_0 = "0" enables high and middle bits. A_0 = "1" enables low bits and trailing "0's".

Multiplexer input channels on MN7145 Series devices are randomly accessed via Address lines (MA_0, MA_1, MA_2). The multiplexer address may be changed after a conversion cycle is complete. However, if desired, the multiplexer address may be changed during a conversion cycle. If doing so, caution must be used to ensure that the address is not updated within 1μsec of having initiated the conversion.

The Read/Convert input (R/$\overline{C}$, pin 4) is used in combination with the Byte Address/Short Cycle input (A_0, pin 3) to initiate either 8 or 12-bit conversion cycles and to read back output data stored in the A/D's 3-state output buffer. Conversion cycles are initiated by bringing R/$\overline{C}$ low. Read cycles are initiated by bringing R/$\overline{C}$ high. R/$\overline{C}$ may remain low during a conversion or it may be brought back high. If it is returned high, it must be done so within 1.5μsec after the conversion begins. If R/$\overline{C}$ is left low during a conversion, it should not be brought high until after the status line has fallen indicating that the conversion is complete.

Output data is only enabled when Status = "0" and R/$\overline{C}$ = "1". However, if R/$\overline{C}$ has been brought high during the conversion, output data will automatically be enabled 300nsec (minimum) prior to the fall of Status. If R/$\overline{C}$ is left low during a conversion, the output lines will remain in the high-impedance state when Status returns low. R/$\overline{C}$ must then be brought high to read output data.

The Byte Address/Short Cycle input (A_0, pin 3) is used in combination with R/$\overline{C}$ when initiating conversions and reading output data. When initiating a conversion, the signal applied to A_0 determines whether a 12-bit (A_0 = "0") or an 8-bit conversion is initiated (A_0 = "1"). As discussed earlier, conversion cycles are initiated by the falling edge of R/$\overline{C}$. When reading digital output data from MN7145 Series devices, the signal applied to A_0 determines which 8-bit data byte is multiplexed to the eight digital output lines. When A_0 = "0", the MSB byte (MSB through bit 8) is enabled. When A_0 = "1", the LSB byte (bit 9 through LSB) is enabled.

Table 2: MN7145 Series Truth Table

Control Lines					
R/$\overline{C}$	A_0	MA_2	MA_1	MA_0	Device Operation
X	X	0	0	0	Select MUX Channel 1
X	X	0	0	1	Select MUX Channel 2
X	X	0	1	0	Select MUX Channel 3
X	X	0	1	1	Select MUX Channel 4
X	X	1	0	0	Select MUX Channel 5
X	X	1	0	1	Select MUX Channel 6
X	X	1	1	0	Select MUX Channel 7
X	X	1	1	1	Select MUX Channel 8
1→0	0	X	X	X	Initiate 12-Bit Conversion on Selected Channel
1→0	1	X	X	X	Initiate 8-Bit Conversion on Selected Channel
1	0	X	X	X	Enable 8 MSB's (high and middle bits)
1	1	X	X	X	Enable 4 LSB's (low bits) and 4 trailing "0's"
0	X	X	X	X	Output Data Disabled (high-impedance state)

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (2.4V minimum).
2. "0" indicates TTL logic low (0.8V maximum).
3. X indicates "don't care".
4. 1→0 indicates logic transition (falling edge).
5. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4 LSB's	

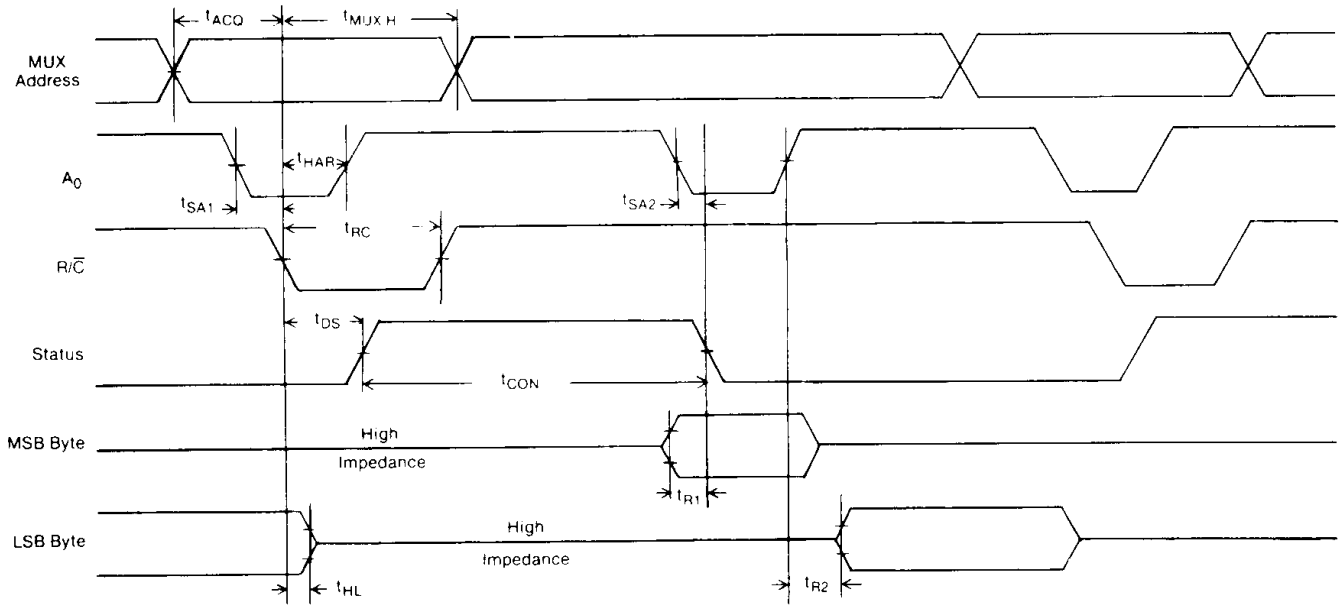
TIMING - MUX ADDRESSING—MN7145 Series devices' input multiplexer is randomly addressed by applying the desired channel address (000 = channel 1, 111 = channel 8) to the address lines (MA_0, MA_1, MA_2). Once the desired channel is selected, 10μsec must be allowed for T/H acquisition time (t_{ACQ}) prior to initiating a conversion. The multiplexer address may be updated as early as 1μsec (t_{MUXH}) after the conversion cycle has begun if this is necessary to meet system timing requirements. This address hold time (t_{MUXH}) ensures that the T/H amplifier has fully switched into the hold mode prior to being presented with the signal on the next channel.

TIMING - INITIATING CONVERSIONS—As stated earlier, the falling edge of R/$\overline{C}$ in combination with A_0 initiates either 8-bit conversion cycles (A_0 = "1") or 12-bit conversion cycles (A_0 = "0"). If the multiplexer address has been changed prior to initiating a conversion, a minimum of 10μsec must be allowed for T/H acquisition time. As stated earlier, the multiplexer address may be changed during an ongoing conversion. In this case, the T/H will be commanded back into the track mode and will start acquiring the new channel's signal as soon as the ongoing conversion is complete.

Timing for a typical 12-bit conversion cycle is shown below. In this example, the multiplexer is addressed; 10μsec T/H acquisition time is allowed; and A_0 is set to a logic "0" all prior to initiating the 12-bit conversion cycle. A_0 must remain valid for 50nsec while R/$\overline{C}$ is low to ensure that a 12-bit conversion cycle is properly initiated (t_{HAR} = 50nsec min.). Status output rises to a logic "1" 200nsec after R/$\overline{C}$ is brought low (t_{DS} = 200nsec max.) commanding the T/H amplifier into the hold mode and signaling that a conversion cycle is in progress. While Status is high, the output buffers return to the high-impedance state and output data cannot be read. The multiplexer address is updated after a minimum address hold time of 1μsec (t_{MUXH} = 1μsec min.). In this example, R/$\overline{C}$ is returned high during the conversion cycle so that output data will be automatically enabled upon completion of the cycle. Once a conversion has started, additional R/$\overline{C}$ falling edges will be ignored. However, if A_0 changes state after a conversion begins, additional R/$\overline{C}$ falling edges will latch the new state of A_0, possibly causing a wrong cycle length (8 vs. 12 bits) for that conversion. Not shown in the example below, R/$\overline{C}$ may remain low during the conversion in which case the output data will remain in the high-impedance state when Status returns low at the end of the conversion. Output data can then be enabled by bringing R/$\overline{C}$ high and asserting A_0 as desired.

TIMING - RETRIEVING DATA—When the conversion cycle is complete and Status output is low, the combination of signals applied to R/$\overline{C}$ and A_0 allows output data bytes to be read (A_0 = "0" MSB byte, A_0 = "1" LSB byte). In the example below, R/$\overline{C}$ is returned high during the conversion, and A_0 is set so that the MSB byte is automatically enabled 300nsec before the end of the conversion cycle. After the MSB byte has been accessed by the system, the LSB byte is multiplexed to the data output lines by bringing A_0 high. Break-before-make action ensures that MSB and LSB data bytes will not be enabled at the same time. Data access time is 150nsec from the change of A_0 (t_{R2} = 150nsec max.). If one desires, R/$\overline{C}$ may remain low during the conversion, in which case, output data will not be enabled until Status is low and R/$\overline{C}$ is brought high. In this case, data access from R/$\overline{C}$ = "1" is similarly 150nsec.

TIMING DIAGRAM



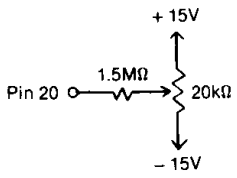
MN7145 Series Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{ACQ}	T/H Acquisition Time	10	6		μsec
t_{MUXH}	Multiplexer Address Hold Time	1			μsec
t_{SA1}	A_0 Setup to R/C̄ Low	0			nsec
t_{SA2}	A_0 Setup to Status Low	100	50		nsec
t_{HAR}	A_0 Valid During R/C̄ Low	50			nsec
t_{RC}	R/C̄ Pulse Width	50			nsec
t_{DS}	Status Delay from R/C̄ Low		100	200	nsec
t_{R1}	Status Delay After Data Valid	300	500	1000	nsec
t_{R2}	Data Access Time from A_0		60	150	nsec
t_{HL}	Data Valid After R/C̄ Low	25			nsec
t_{CON}	Conversion Time:				
	8-Bit Cycle	10	13	17	μsec
	12-Bit Cycle	15	20	25	μsec

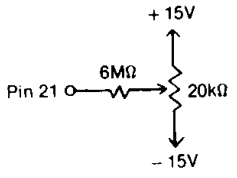
OPTIONAL OFFSET AND GAIN ADJUSTMENTS—MN7145 Series devices will operate as specified without additional adjustments. If desired, however, system absolute accuracy error can be improved by following the trimming procedure below. Adjustments should be made following warmup, and to avoid interaction, the offset adjustment should be made before the gain adjustment. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. Series resistors can be ±20% carbon composition or better. If these adjustments are not used, pins 20 and 21 should be left open. Do not ground. If gain and offset adjusting is performed on MN7145 Series devices, reference voltages may be applied to any of the analog input channels. It is recommended that offset and gain adjustments be made while the system is performing continuous or at least repeated conversions.

OFFSET ADJUSTMENT—Connect the offset potentiometer as shown below and apply an analog input voltage equivalent to + ½ LSB (MN7145) or − FS + ½ LSB (MN7146/7147). See Digital Output Coding section for the appropriate analog input voltages. While the device is performing repeated conversions, monitor the output and adjust the offset potentiometer "down" until all output bits are "0". Then adjust "up" until the LSB "flickers" on and off.

GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the analog input voltage equivalent to + FS − 1½ LSB. See Digital Output Coding section for the appropriate analog input voltages. While the device is performing repeated conversions, monitor the output and adjust the gain potentiometer "up" until all output bits are "1". Then adjust "down" until the LSB "flickers" on and off.



OFFSET ADJUST

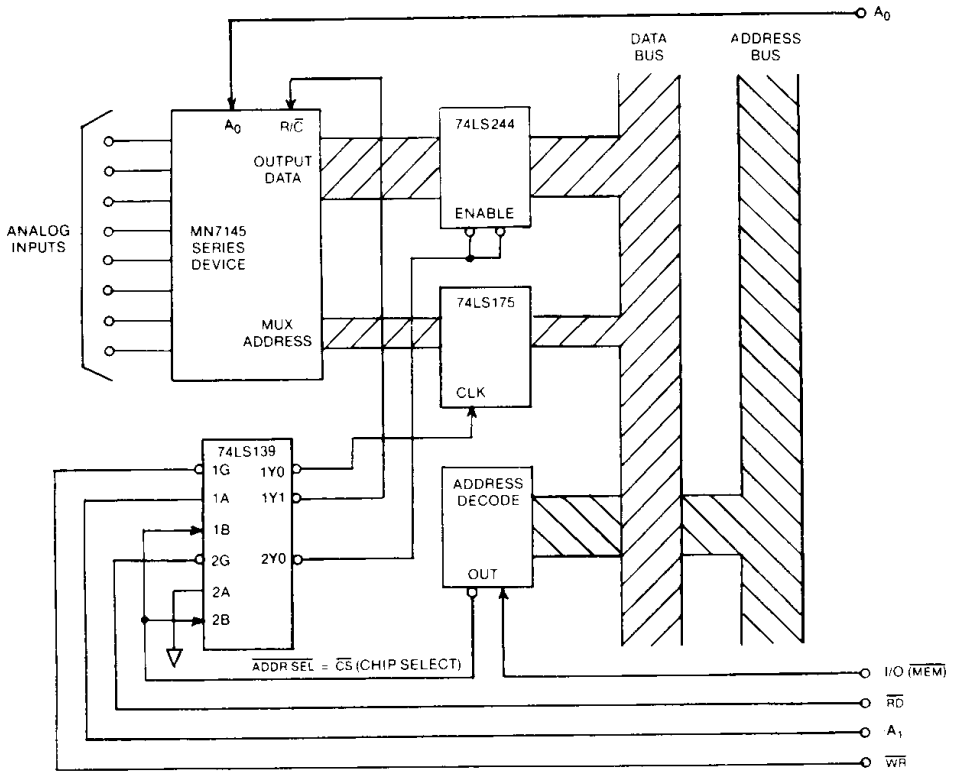


GAIN ADJUST

DIGITAL OUTPUTS—MN7145 Series devices have 8 digital output lines (pins 1, 2, 23-28) on which a 12-bit data word can be read in two 8-bit bytes. In the read mode, the state of A_0 determines if the MSB byte (A_0 = "0") or the LSB byte (A_0 = "1") is multiplexed to the digital output lines. Break-before-make action guarantees that the MSB and LSB bytes will not be enabled at the same time. Digital output data can only be read between conversions because output data lines are returned to the high impedance state whenever a conversion is in progress. See Pin Designations for data bit (DB0-DB11) assignments.

MICROPROCESSOR INTERFACE—The MN7145 Series DAS can be interfaced with most popular microprocessors. The DAS may be addressed either as a memory location (memory mapped) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM to which READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O ENABLE can be substituted for MEMORY ENABLE or $\overline{I/OR}$ and $\overline{I/OW}$ substituted for $\overline{MEMR}$ and $\overline{MEMW}$. The accompanying diagram shows a typical scheme to implement this interface.

STS is not used in this example; the μP must read data 30μsec after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).



DIGITAL OUTPUT CODING

Analog Input Voltage (Volts)			Digital Output
MN7145	MN7146	MN7147	
0 to +10V	±5V	±10V	MSB LSB
+10.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+4.9963	+9.9927	1111 1111 111Ø*
+5.0012	+0.0012	+0.0024	1000 0000 000Ø*
+4.9988	−0.0012	−0.0024	ØØØØ ØØØØ ØØØØ*
+4.9963	−0.0037	−0.0073	0111 1111 111Ø*
+0.0012	−4.9988	−9.9976	0000 0000 000Ø*
0.0000	−5.0000	−10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input range, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN7147 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition will occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".