

SPICE Device Model Si5441DC

Vishay Siliconix

P-Channel 2.5-V (G-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

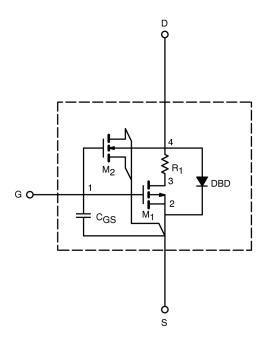
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm qd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	1.02	V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	60	А
Drain-Source On-State Resistance ^a	r _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -3.9 \text{ A}$	0.043	Ω
		$V_{GS} = -3.6 \text{ V}, I_D = -3.7 \text{ A}$	0.049	
		V _{GS} = -2.5 V, I _D = -3.1 A	0.069	
Forward Transconductance ^a	g _{fs}	$V_{DS} = -10 \text{ V}, I_{D} = -3.9 \text{ A}$	12	S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.1 A, V _{GS} = 0 V	-0.80	V
Dynamic ^b				
Total Gate Charge	Qg	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.9 \text{ A}$	10.5	nC
Gate-Source Charge	Q_{gs}		3	
Gate-Drain Charge	Q_{gd}		2.5	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = -10 \text{ V, } R_L = 10 \Omega$ $I_D \cong -1 \text{ A, } V_{GEN} = -4.5 \text{ V, } R_G = 6 \Omega$ $I_F = -1.1 \text{ A, } \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	23	ns
Rise Time	t _r		29	
Turn-Off Delay Time	$t_{\text{d(off)}}$		39	
Fall Time	t _f		46	
Source-Drain Reverse Recovery Time	t _{rr}		32	

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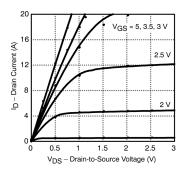
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

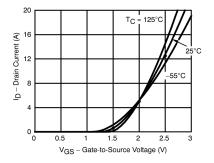


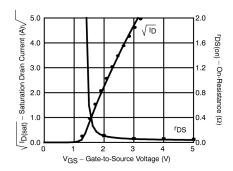


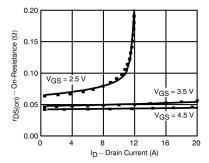
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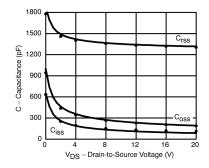
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

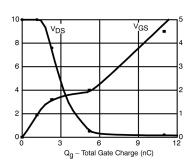












Note: Dots and squares represent measured data.

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