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GigaBit Logic

10G070
10G070K

Variable Modulus Divider
2.0 GHz Clock Rate
10G PicoLogic™ Family

FEATURES

- 2.0 GHz operation (min. @ 25°C)
- 0°C to 85°C commercial temp. range, 10G070
- -40°C to 100°C extended temp. range, 10G070K
- Fixed divide by 5, 6, 10, 11, 20, 21, 40, 41
- Variable modulus operation selectable for divide by 5 and 6, 10 and 11, 20 and 21, or 40 and 41
- Wire-OR output capability
- Mode pin allows 10G PicoLogic, TTL, and CMOS control of N or N+1 division ratio
- 10G PicoLogic, TTL/CMOS I/O compatible
- Available in flatpack, C-leaded or leadless chip carrier and die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

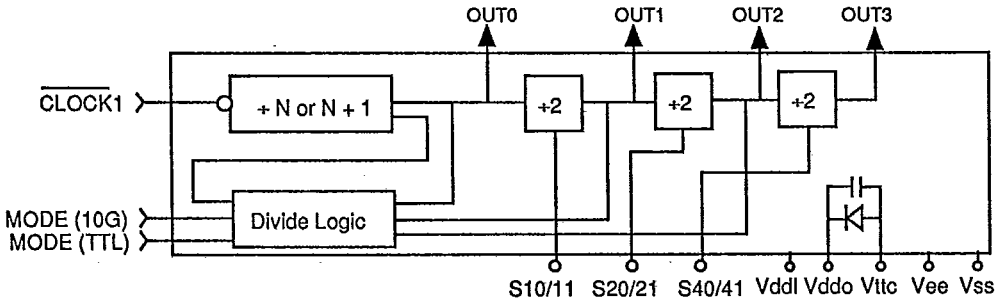
APPLICATIONS

- Frequency synthesizers and phase locked loops (with 10G061 Synchronous Counter and 16G044 Phase Frequency Comparator)

FUNCTIONAL DESCRIPTION

The 10G070 is an ultra-fast 2.0 GHz performance variable modulus divider for use in frequency synthesis and phase locked loop applications. By strapping the S10/11, S20/21, and S40/41 pins to VSS or VEE one of the following four N and N+1 division ratio pairs can be programmed: 5 and 6,10 and 11, 20 and 21, and 40 and 41. When the MODE input is switched to a logic high the counter will divide by N (5, 10, 20, or 40). When the MODE input is switched to a logic low the counter will divide by N+1 (6, 11, 21, or 41). A fixed divide ratio can be obtained by fixing the logic level of the MODE input. When the 10G070 is used to divide by 5 or 6, the output appears on the OUT0 pin. For division by 10 or 11, 20 or 21, and 40 or 41 the output appears on the OUT1, OUT2 and OUT3 pins, respectively. For divide by N ratios, all lower order ratios are simultaneously available.

BLOCK DIAGRAM



10G070, 10G070K ORDERING INFORMATION

PACKAGE TYPE	SPEED				
	10G070 (0°C to 85°C)			10G070K (-40°C to 100°C)	
	1.5 GHz	1.3 GHz	1.0 GHz	1.5 GHz	1.0 GHz
36 pin Leadless carrier	10G070-2L36	10G070-L36	10G070-3L36	10G070K-2L36	10G070K-L36
36 pin Flatpack	10G070-2F	10G070-F	10G070-3F	10G070K-2F	10G070K-F
40 pin Leadless carrier	10G070-2L	10G070-L	10G070-3L	10G070K-2L	10G070K-L
40 pin C- Leaded carrier	10G070-2C	10G070-C	10G070-3C	10G070K-2C	10G070K-C
Unpackaged Dice			10G070-3X		10G070K-X

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FUNCTIONAL DESCRIPTION (cont.)

Also, divide by 5 and 10 are always available. The Mode input has two pins; MODE(10G) for 10G PicoLogic control interface, and MODE(TTL) for TTL and CMOS control interface. When driving the MODE(10G) input the MODE(TTL) pin should be left open. Similarly, when driving the MODE(TTL) input the MODE(10G) pin should be left open. It should be noted that the 10G070 inputs are not ECL compatible. A 10G002 XOR/XNOR/Line Receiver can be used as an ECL to GaAs level translator. The 10G070 has optional clamp inputs to provide flexibility when interfacing to other components. When connected to a supply voltage at the input threshold of -1.3V, input clamps VICH and VICL allow the 10G070 to be driven with input signals greater than 2.0Vp-p without damage to the internal gates. This is particularly useful when the 10G070 CLOCK pin is driven directly from a voltage controlled oscillator (VCO). When not used, input clamp VICH should be connected to VDDL (GND) and VICL to VSS (-3.4V). Logic clamps VLCH and VLCL provide a means of limiting the voltage swing of internal gates, thus increasing the performance of the divider. The recommended voltages for VLCH and VLCL are indicated with the notes for the AC characteristics specifications. When not used the VLCH and VLCL pins may be left open. The output driver high level clamp, VDCH, is not used when driving GaAs logic, but may be used to limit VOH when driving ECL. See App. Note 4 for details.

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PIN DESCRIPTIONS

$\overline{\text{CLOCK}}$	High speed clock input. The falling edge of CLOCK causes the outputs to change.
MODE (10G)	Mode control input. When high the device counts by N, when low the device counts by N+1. The input is 10G level compatible. When MODE(TTL) is used then MODE(10G) must be left open.
MODE (TTL)	Mode control input. When high the device counts by N, when low, the device counts by N+1. This input is level shifted internally to make it TTL compatible. When MODE(10G) is used MODE (TTL) must be left open.
OUT0-OUT3	Divide by 5 or 6 output, OUT0 Divide by 10 or 11 output, OUT1 Divide by 20 or 21 output, OUT2 Divide by 40 or 41 output, OUT3.
S10/11	Select 10/11inputs.
S20/21	Select 20/21 inputs.
S40/41	Select 40/41 inputs. Program the valid output by strapping these inputs to VSS or VEE according to the programming table in the 10G070 Operation section of this datasheet.
VDDO	Output driver ground (0V).
VDDL	Internal logic ground (0V).
VSS	-3.4V power supply.
VEE	-5.2V power supply.
VTTC	The AC return pin for the internal VDDO decoupling capacitor. VTTC is not brought into the 10G070 die. VTTC is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. May be used to limit VOH when driving ECL. When not in used, VDCH should be connected to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times at the CLOCK input. .
VLCH, VLCL	Logic clamp voltages. When connected as specified in the AC Characteristic Notes these pins clamp the internal logic voltage swing of the device, thus enhancing the AC performance of the part. When not used these pins may be left open.
VTRIM	Input threshold adjustment voltage. A value of VTRIM more or less negative than VEE will adjust all the input thresholds around their nominal value of -1.3V. Connect to VEE or leave open when not used.

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10G070 PROGRAMMING

The operation of the 10G070 is described by the following function select table. The S10/11, S20/21, S40/41 inputs are strapped to select a fixed set of N/N+1 division ratios. The MODE input is logically controlled to select a variable modulus divide by N and N+1 operation or strapped to select a fixed N or N+1 divider operation. The MODE control input may be arbitrarily changed throughout most of the count cycle without affecting the output. However, the MODE input must be stable at the desired logic high or logic low level for the specified set-up and hold time before and after the high to low CLOCK transition that causes the chosen output to transition from a low (0) to a high (1).

S40/41	S20/21	S10/11	MODE	DIVISION RATIO	OUTPUT PIN
VSS	VSS	VSS	0	6	OUT0
VSS	VSS	VSS	1	5	OUT0
VSS	VSS	VEE	0	11	OUT1
VSS	VSS	VEE	1	10	OUT1
VSS	VEE	VEE	0	21	OUT2
VSS	VEE	VEE	1	20	OUT2
VEE	VEE	VEE	0	41	OUT3
VEE	VEE	VEE	1	40	OUT3

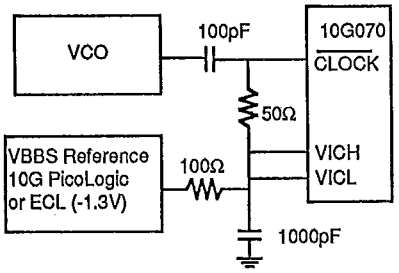
Another distinctive feature of the 10G070 Variable Modulus Divider is the availability of lower order divide ratio outputs.The table below shows the simultaneously available outputs for any given divide ratio. This feature will allow designers additional flexibility in synthesizer design.

	OUTPUTS			
PROGRAMMED RATIO	OUT0 (÷5/6)	OUT1 (÷10/11)	OUT2 (÷20/21)	OUT3 (÷40/41)
÷40	÷5	÷10	÷20	÷40
÷41	7x5 + 1x6	3x10 + 1x11	1X20 +1X21	÷41
÷20	÷5	÷10	÷20	---
÷21	3x5 + 1x6	1x10 + 1x11	÷21	---
÷10	÷5	÷10	---	---
÷11	1x5 + 1x6	÷11	---	---
÷5	÷5	—	---	---
÷6	÷6	—	---	---

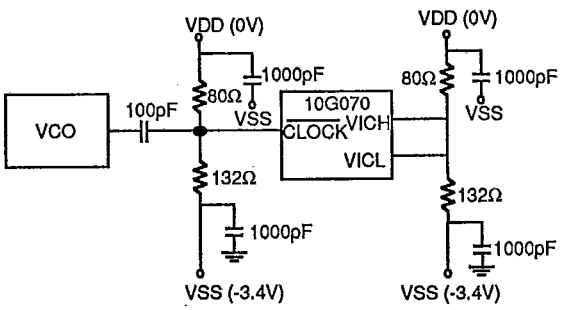
VOLTAGE CONTROLLED OSCILLATOR (VCO) INTERFACE

The $\overline{\text{CLOCK}}$ pin of the 10G070 has an input threshold of -1.3V. To interface the device to a general purpose VCO an AC coupling network is recommended. There are two common cases; one in which the input threshold VBB (-1.3V) is available, and another when VBB is not available.

VCO Interface to 10G070 With VBB Reference



VCO Interface to 10G070 Without VBB Reference



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STATE TRANSITIONS

DIVIDE BY 5/6 MODE

N/N+1 Divider

OUT0	Q1	Q0
1	1	1
1	1	0
1	0	0
0	0	0
0	0	1
0	1	1

MODE = 1 DIVIDE BY 5

MODE = 0 DIVIDE BY 6

OUT 1 = OUT2 = OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N+1 divider.

Use OUT0 as chip output.

DIVIDE BY 10/11 MODE

N/N+1 DIVIDER

OUT1	OUT 0	Q1	Q2
1	1	1	1
1	1	1	0
1	1	0	0
1	0	0	0
1	0	0	1
1	0	1	1
0	1	1	0
0	1	0	0
0	0	0	0
0	0	0	1
0	0	1	1

MODE = 0 DIVIDE BY 11

MODE = 1 DIVIDE BY 10

OUT2 = OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N+1 divider. Use OUT1 as chip output.

DIVIDE BY 20/21 MODE

N/N+1 DIVIDER

OUT2	OUT1	OUT0	Q1	Q0
1	1	1	1	1
1	1	1	1	0
1	1	1	0	0
1	1	0	0	0
1	1	0	0	1
1	1	0	1	1
1	0	5 count subcycle (Note 1)		
0	1	5 count subcycle (Note 1)		
0	0	1	1	0
0	0	1	0	0
0	0	0	0	0
0	0	0	0	1
0	0	0	1	1

MODE = 0 DIVIDE BY 21

MODE = 1 DIVIDE BY 20

OUT3 = 0. Q0 and Q1 are internal flip-flops in the N/N+1 divider. Use OUT2 as chip output.

DIVIDE BY 40/41 MODE

N/N+1 DIVIDER

OUT3	OUT2	OUT1	OUT0	Q1	Q2
1	1	1	1	1	1
1	1	1	1	1	0
1	1	1	1	0	0
1	1	1	0	0	0
1	1	1	0	0	1
1	1	1	0	1	1
1	1	0	5 count subcycle (Note 1)		
1	0	1	5 count subcycle (Note 1)		
1	0	0	5 count subcycle (Note 1)		
0	1	1	5 count subcycle (Note 1)		
0	1	0	5 count subcycle (Note 1)		
0	0	1	5 count subcycle (Note 1)		
0	0	0	1	1	0
0	0	0	1	0	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	1	1

MODE = 0 DIVIDE BY 41

MODE = 1 DIVIDE BY 40

Q0 and Q1 are internal flip-flops in the N/N+1 divider. Use OUT3 as chip output.

Note 1: To avoid unnecessarily long state transition tables, the five count subcycle on Q0, Q1 and OUT0 has been omitted. The state transition table for this subcycle is:

OUT0	Q1	Q0
1	1	0
1	0	0
0	0	0
0	0	1
0	1	1

Pins OUT1, OUT2, and OUT3 do not change during this five count subcycle.

Q0 and Q1 are internal flip-flops in the N/N+1 divider.

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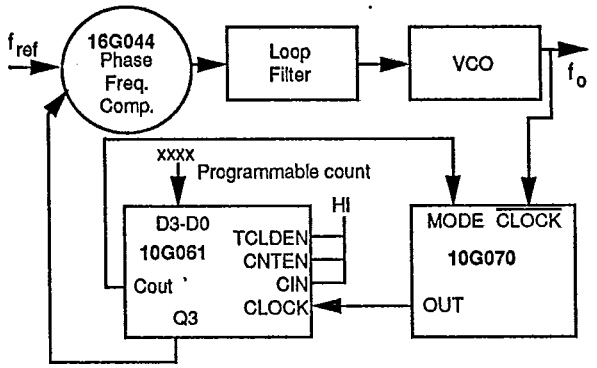
FREQUENCY SYNTHESIS APPLICATIONS

The 10G070, in combination with GigaBit's 10G061 Four Stage Synchronous Programmable Counter, provides the components necessary to design very high speed (2GHz) programmable counters for application in synthesizer phase locked loops using the pulse swallowing, or swallow counter technique. This technique uses programmable counters to toggle the MODE control of the 10G070 between modulus N and N+1 to switch among a large number of synthesizer output frequencies. Further information is provided in the 10G061 datasheet. A typical programmable frequency synthesizer block diagram is shown.



ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65 °C to +150 °C	
TJ	Junction Temperature	-55 °C to +150 °C	
TC	Case Temperature Under Bias	-55 °C to +125 °C	2
VDDO	Output Driver Supply Voltage	-0.8 V to +1.0 V	
VSS	Supply Voltage	-4.0 V to +0.5 V	
VEE	Supply Voltage	-7.0 V to VSS + 0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = -3.4 V, VEE = -5.2 V	-4.0 V to +0.5 V	
VINTTL	Voltage Applied to MODE(TTL); Continuous	-4.0 V to +4.0 V	
IIN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +7.0 V	3
IOUT	Current From Any Output; Continuous	-70 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	
VDCH	Output Driver Clamp Voltage	VSS to VDDO	4
IDCH	Output Driver Clamp Current	-20 mA	
VICH	Input Clamp High Voltage	-2.0V to VDDL	5
IICH	Input Clamp High Current	-20mA	
VICL	Input Clamp Low Voltage	VSS to -0.4V	5
IICL	Input Clamo Low Current	20 mA	
VLCH	Logic Clamp High Voltage	-2.0V to VDDL	5
ILCH	Logic Clamp High Current	-40mA	
VLCL	Logic Clamp Low Voltage	VSS TO 0.4V	5
ILCL	Logic Clamp Low Current	-40 mA	

Notes:
1. All voltages specified with VDDL defined as 0 V. Positive current is defined as current into the device.
2. TC is measured at case bottom.
3. Subject to IOUT and power dissipation limitations.
4. Subject to IDCH and power dissipation limitations.
5. Subject to clamp current and power dissipation limitations.

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USER NOTES:

Unlike most PicoLogic circuits, the input threshold of the 10G070 is not stablized with a VBB feedback circuit. Therefore, the threshold of all inputs will vary from their nominal -1.3V room temperature level with variations in VSS and temperature. VTRIM may be used to adjust input threshold. Alternatively, it is necessary to drive each used input with large peak-to-peak level signals as shown for VIH and VIL in the DC Characteristics table. Under high speed conditions, the clock input should be ≥2Vp-p to achieve maximum speed as described in the notes to th AC Characteristics tables. Other PicoLogic devices can be used as drivers to provide these levels by terminating the outputs to VSS instead of the more usual VTT.

10G070 RECOMMENDED OPERATING CONDITIONS (note 3)

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC1	Case Operating Temp. (10G070)	0	25	85	°C	1
TC2	Case Operating Temp. (10G070K)	-40	25	100	°C	1
VDDL	Logic Supply Voltage		GND		V	
VDDO	Output Driver Supply Voltage	-0.8	GND	+1.0	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	
VTT	Load Termination Supply Voltage	VSS	-2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2
VICH	Input Clamp High Voltage	-1.8	VDDL	VDDL	V	
VICL	Input Clamp Low Voltage	VSS	VSS	-0.8	V	
VLCH	Logic Clamp High Voltage	-1.8	VDDL	VDDL	V	
VLCL	Logic Clamp Low Voltage	VSS	VSS	-0.8	V	
VDCH	Output Driver Clamp High Voltage	-2.5	-2.0	VDDO	V	4
VTRIM	Input Threshold Adjust Voltage	VEE-1	VEE	VEE+1	V	

NOTES 1. Tcase measured at case bottom. **User attention to device thermal management is recommeded.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.
3. See GigaBit Application Note - 4 for a discussion of interfacing requirements to and from PicoLogic devices.
4. When driving GaAs logic, VDCH is not used. To limit VOH when driving ECL, see App. Note 4.

10G070/K DC CHARACTERISTICS (Notes 1,2)

TC = -40°C to +100°C, VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
VOH	Output Voltage High	-0.8	-0.6	-0.3	V		
VOL	Output Voltage Low	-2.0	-1.9	-1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	
VIH1	Input Voltage High (70)	-0.6		VDDL	V		4,5
VIL1	Input Voltage Low (70)	VSS		-1.9	V		4,5
VIH2	Input Voltage High (70K)	-0.6		VDDL	V		4,5
VIL2	Input Voltage Low (70K)	VSS		-2.1	V		4,5
VIH(TTL)	Input Voltage High TTL	2.8		3.5	V		
VIL(TTL)	Input Voltage Low TTL	-1.0		0.8	V		
IIN	Input Current		200	500	uA	VIN = -0.6V to -1.9V	
ISS	Power Supply Current		110	200	mA		
IEE	Power Supply Current		18	25	mA		
PD	Power Dissipation		500	850	mW		3

Notes: 1. These characteristics are applicable from DC to 500MHz.
2. Test conditions (unless otherwise indicated):
VTT = -2.0V VTRIM = VEE
VTTC = VTT RLOAD = 50Ω to -2.0V
IOH is the available output current at VOH = -0.8V.
3. At nominal supply voltages and 50% duty cycle. Exclusive of VDDO output source follower power (typically 15 mW/output) and output clamp power (if any).
4. CLOCK input rise and fall times ≤ 2ns (measured from the 20% and 80% points).
5. Input levels are 10G PicoLogic compatible.

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AC CHARACTERISTICS (Note 1)

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VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.5		2.0			1.5		GHz	2,3
T2	CLOCK Low Time	333		250			333		ps	2,3
T3	CLOCK High Time	333		250			333		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	690		500			690		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	345		250			345		ps	4
T6	CLOCK Low to OUT0		1.9			1.5		1.9	ns	
T7	CLOCK Low to OUT1		3.0			2.5		3.0	ns	
T8	CLOCK Low to OUT2		4.1			3.5		4.1	ns	
T9	CLOCK Low to OUT3		5.3			4.5		5.3	ns	

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VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.3		1.75			1.3		GHz	2,3
T2	CLOCK Low Time	385		285			385		ps	2,3
T3	CLOCK High Time	385		285			385		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	770		575			770		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	385		285			385		ps	4
T6	CLOCK Low to OUT0		2.3			1.9		2.3	ns	
T7	CLOCK Low to OUT1		4.6			3.0		4.6	ns	
T8	CLOCK Low to OUT2		6.3			4.1		6.3	ns	
T9	CLOCK Low to OUT3		8.2			5.3		8.2	ns	

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VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= 0°C		Tc = +25°C			Tc= +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.0		1.5			1.0		GHz	2,3
T2	CLOCK Low Time	415		333			415		ps	2,3
T3	CLOCK High Time	415		333			415		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	835		690			835		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	415		345			415		ps	4
T6	CLOCK Low to OUT0		2.5			2.2		2.5	ns	
T7	CLOCK Low to OUT1		5.0			3.6		5.0	ns	
T8	CLOCK Low to OUT2		7.0			4.9		7.0	ns	
T9	CLOCK Low to OUT3		9.0			6.3		9.0	ns	

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AC CHARACTERISTICS (Note 1)

10G070K-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.5		2.0			1.5		GHz	2,3
T2	CLOCK Low Time	333		250			333		ps	2,3
T3	CLOCK High Time	333		250			333		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	690		500			690		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	345		250			345		ps	4
T6	CLOCK Low to OUT0		1.9			1.5		1.9	ns	
T7	CLOCK Low to OUT1		3.0			2.5		3.0	ns	
T8	CLOCK Low to OUT2		4.1			3.5		4.1	ns	
T9	CLOCK Low to OUT3		5.3			4.5		5.3	ns	

10G070K-3 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYM-BOL	PARAMETER	Tc= -40°C		Tc = +25°C			Tc= +100°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	CLOCK Maximum Toggle Frequency	1.0		1.5			1.0		GHz	2,3
T2	CLOCK Low Time	500		333			500		ps	2,3
T3	CLOCK High Time	500		333			500		ps	2,3
T4	MODE to CLOCK Low (Mode Setup Time)	1000		690			1000		ps	4
T5	CLOCK Low to MODE (Mode Hold Time)	500		345			500		ps	4
T6	CLOCK Low to OUT0		3.0			1.9		3.0	ns	
T7	CLOCK Low to OUT1		5.0			3.0		5.0	ns	
T8	CLOCK Low to OUT2		7.0			4.1		7.0	ns	
T9	CLOCK Low to OUT3		9.0			5.3		9.0	ns	

NOTES:

1. Test Conditions, unless otherwise stated:
   Ta = 25°C; VICH = 0V; VLCL = -1.25V; VOH ≥ -0.8V
   VDDL = VDDO = 0V; VICL = VSS; VDCH = 0V; VOL ≤-1.8V
   VEE = -5.2V; VLCH = -1.5V; VDCL = VSS; RLOAD = 50Ω to -2.0V
   VSS = -3.4V; VTTC = -2.0V; Output rise and fall times≤500ps (20% - 80%)
2. CLOCK rise and fall times ≤ 150 ps (measured from the 20% and 80% points).
3. Test conditions: CLOCK input = 2V pp sine wave, -1.3V DC offset.
4. The MODE control input may be arbitrarily changed throughout most the count cycle without affecting the output. However, the MODE input must be stable at the desired logic high or low level for the specified setup and hold time, respectively, before and after the high to low CLOCK transition that causes the chosen output to transition from a low (0) to a high (1).

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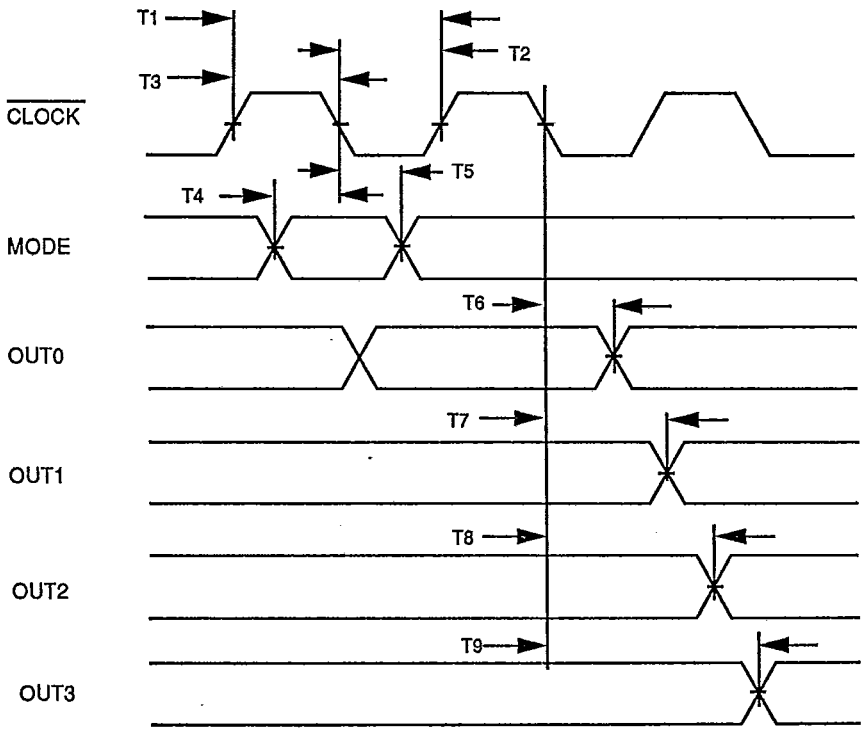
GigaBit Logic

10G070
10G070K

PHASE NOISE				
OFFSET (Hz)		RAW L(f)	CORRECTED dBc/Hz	NOTES
(+5)	1K	-120.1	-106.1	Fin = 500MHz Noise Floor = -160dBc/Hz Input reference correction is 14dBc/Hz (+5) and 15.6dBc/Hz (+6).
	2.5K	-126.0	-112.0	
	5.0K	-127.8	-113.8	
	7.5K	-133.9	-119.9	
	10.0K	-136.5	-122.5	
	15.0K	-136.7	-122.7	
	20.0K	-139.2	-125.2	
	25.0K	-136.0	-122.0	
(+6)	1K	-121.7	-106.1	
	2.5K	-127.6	-112.0	
	5.0K	-129.4	-113.8	
	7.5K	-135.5	-119.9	
	10.0K	-138.1	-122.5	
	15.0K	-138.3	-122.7	
	20.0K	-140.8	-125.2	
	25.0K	-137.6	-122.0	

SWITCHING WAVEFORMS



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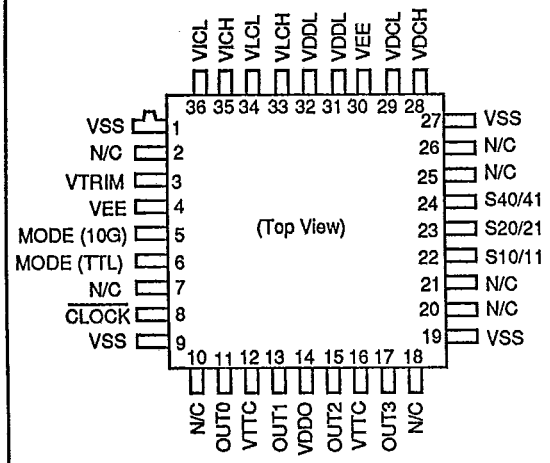
GigaBit Logic

10G070
10G070K

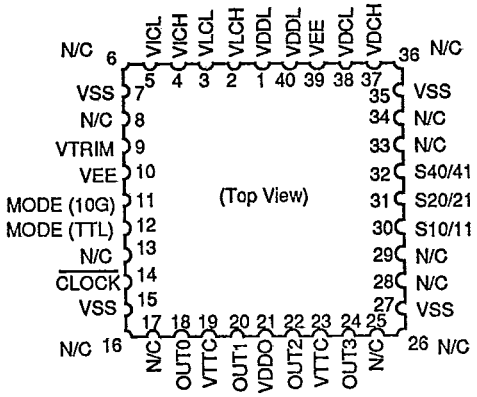
PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
PACKAGE TYPE "F"



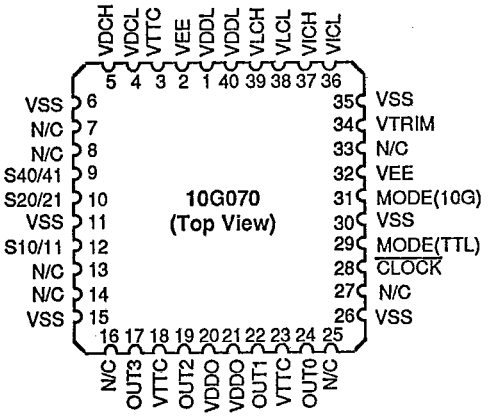
NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect. The package lid and bottom surface are at VSS potential.

36 PIN LEADLESS CHIP CARRIER
PACKAGE TYPE "L36"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect. The package lid, bottom heat vias, and 4 N/C corner pins (6,16,26,36) are at Vss potential.

40 PIN LEADLESS AND C-LEADED CHIP CARRIERS
PACKAGE TYPES "L" AND "C"



Note: N/C = No Connection

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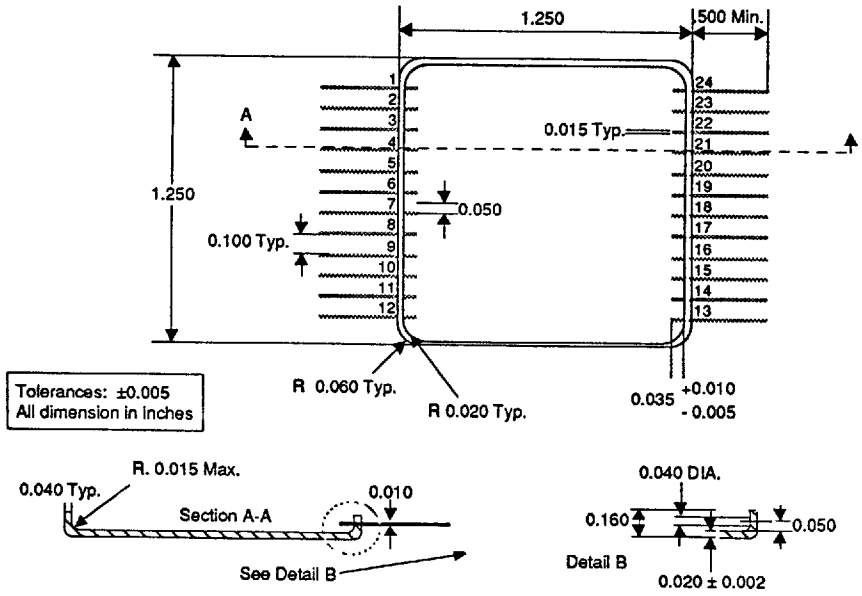
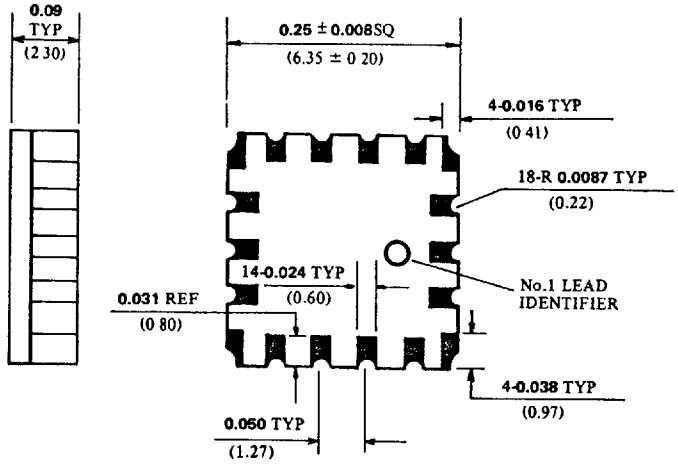
GigaBit Logic

24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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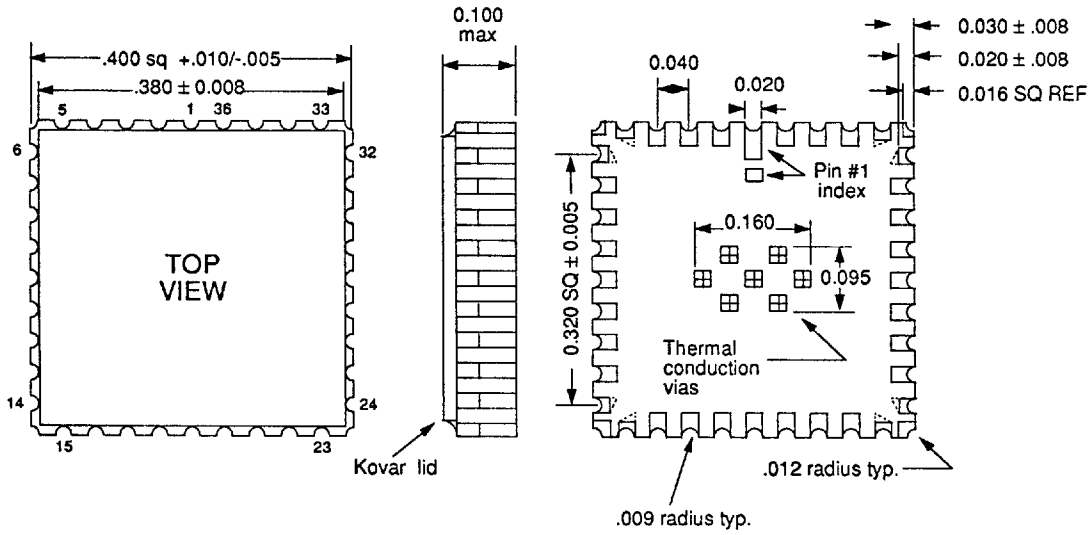
GigaBit Logic

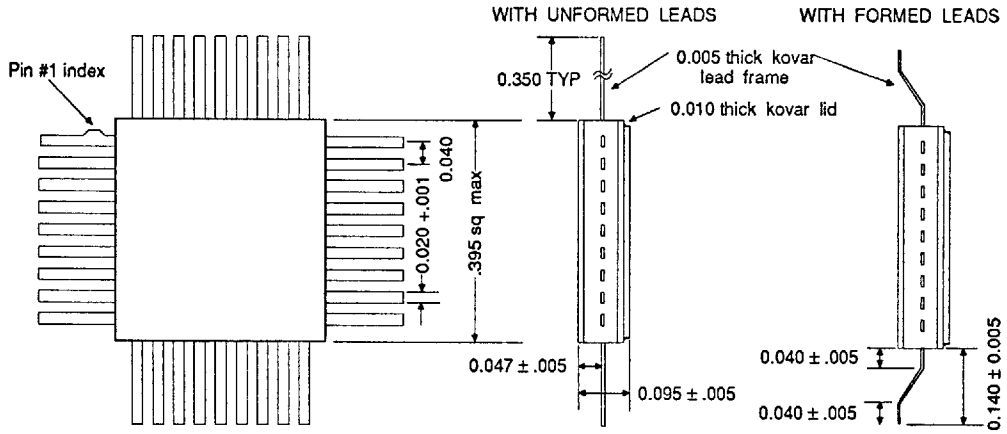
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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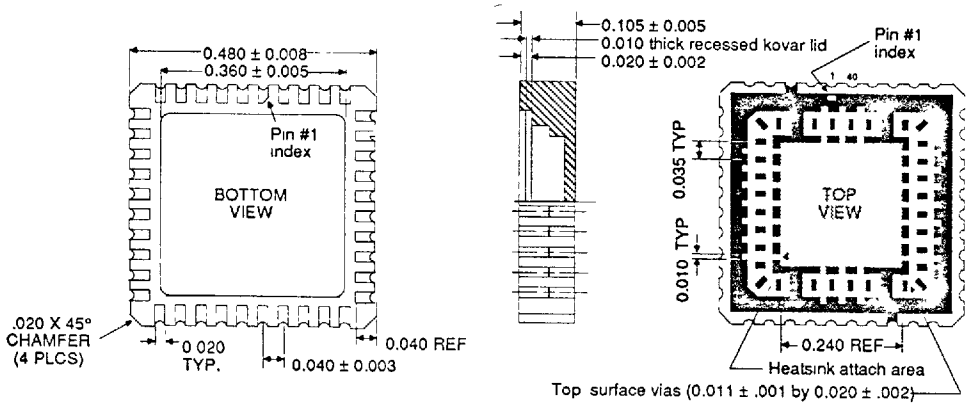
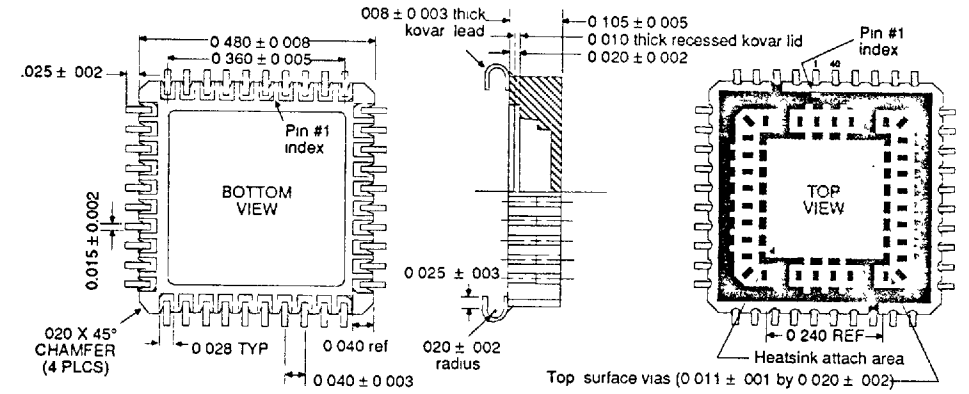
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

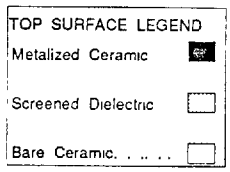


40 PIN LEADED CHIP CARRIER
TYPE C

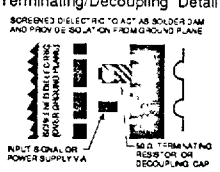


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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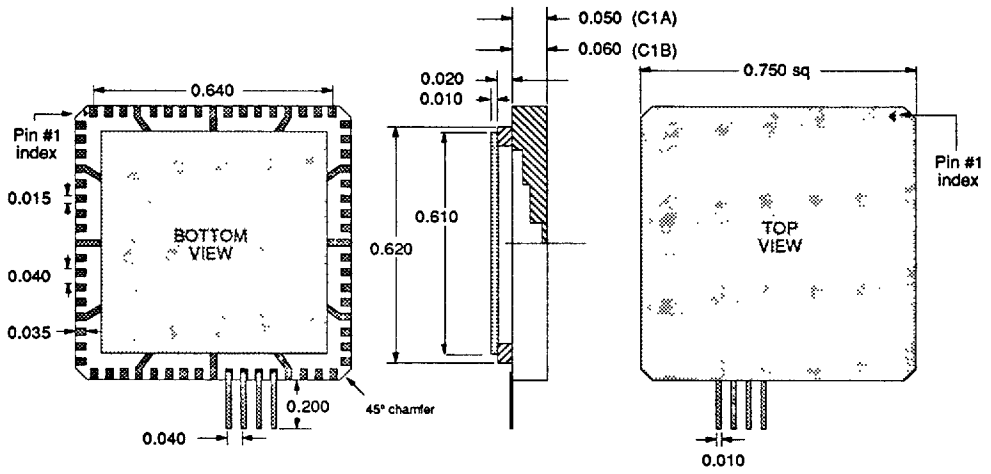
GigaBit Logic

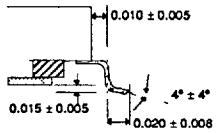
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3