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GigaBit Logic

16G040

High Speed Clock & Data Recovery Circuit 2.0 Gbit/s NRZ Data Rate

FEATURES

- Clock recovery and data retiming and regeneration subsystem
- 2.0 Gbit/s performance
- Patented, self-acquiring PLL GaAs IC design
- Easy interface to 10G041A Time Division DEMUX
- Loop bandwidth externally controllable for fast acquisition time
- Available in C-leaded or leadless chip carriers, or as unpackaged die
- Complete PLL CDR available for 100 to 625 Mb/s data rates: 16G041-H

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FUNCTIONAL DESCRIPTION

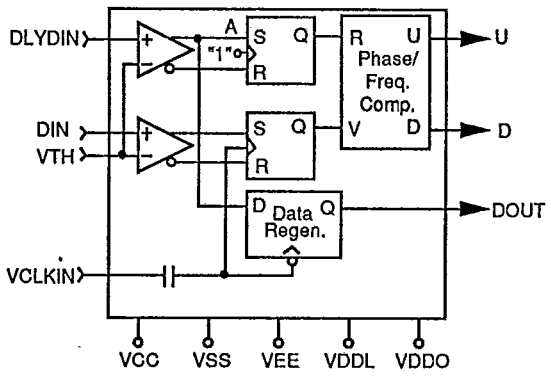
The 16G040 contains the high speed circuitry needed to implement a phase locked loop (PLL) for both clock extraction from high speed digital data streams, as well as data retiming and regeneration. Performance extends to 2.0 Gbit/s. With an external loop filter and VCO, extremely fast acquisition time loops can be realized. The 16G040 is available in GigaBit's standard 40 I/O C-leaded and leadless ceramic chip carrier packages and as unpackaged dice (16G040-2X).

Unlike SAW-filter clock and data recovery approaches which first filter the clock component from incoming data and then retimes it using the extracted clock, the PLL-based 16G040 is capable of synchronizing an external VCO directly to an incoming digital data stream, while simultaneously retiming and regenerating the data stream. In addition, the VCO will generate a clock output even in the absence of data. This might be critical if the recovered clock drives a state machine or any other logic circuitry that might go into a metastable state in the absence of a clock. In operation, the PLL-based 16G040 is capable of unaided frequency acquisition, eliminating the need for special circuits to "pull" the loop into lock when the incoming data rate differs from the initial frequency of the VCO. Compared with other approaches to clock recovery, the 16G040 offers the advantages of a PLL-based approach including wide center frequency tunability range, low cost and high reliability.

APPLICATION

- High speed fiber optic and microwave receivers and repeaters

16G040 BLOCK DIAGRAM



ORDERING INFORMATION

Package	Part No. (up to 2.0 Gb/s @ 25°C)
C-leaded CC	16G040-2C
Leadless CC	16G040-2L
Dice	16G040-2X

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The 16G040 requires a fixed external delay (non-critical, between 1/4 and 1/2 bit period) between inputs DIN (Data In) and DLYDIN (Delayed Data In). GigaBit Application Note 7, titled "Application of the 16G041 Clock and Data Recovery Circuit" provides necessary background material and should be carefully reviewed.

A key subcircuit included in the 16G040 is the phase/frequency comparator. This component is also available as a stand-alone product, the 16G044, with a detailed datasheet which supplements the information contained in this datasheet.

16G040 PLL OPERATION

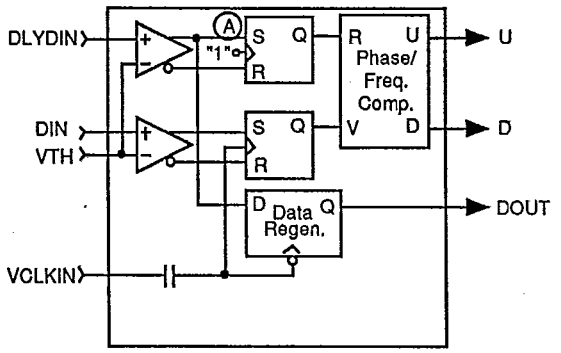
When interconnected to form a phase locked loop as shown in the Typical PLL Circuit diagram (Fig. 2), two modes of operation are possible: 1) the VCO frequency is equal to the input data rate; that is, the loop is in frequency lock but is not phase locked; 2) the initial VCO frequency is unequal to the input data rate but the data rate is within the loop capture range.

PHASE OFFSET OPERATION

When the loop is in frequency but not phase locked, the outputs of the phase/frequency comparator (PFC) will produce pulses which, when low pass filtered and subtracted, provide an error signal that is applied to the Vtune input of the VCO to correct the phase offset. With reference to the 16G040 block diagram (Fig. 1), the signal on the PFC "V" input leads the signal on the"R" input when the rising edge of the clock applied to the clocked S-R latch leads the rising edge of the delayed data input applied to the transparent S-R latch ("A" in the block diagram). "V" lags "R" when the rising edge of the clock input lags the signal at A .

The relative phase of "V" with respect to "R" is sensed by a phase/frequency comparator. The phase/ frequency comparator is an edge-triggered digital device which produces pulses in "U" when "R" leads "V" and in "D" when "R" lags "V". The width of these pulses is equal to the amount by which "R" leads or lags "V". Only one output is active at a time. The difference between the "U" and "D" outputs is fed back to the VCO through an appropriate loop filter, which then "servos" the VCO in the direction necessary to correct this phase offset.

Figure 1
16G040 BLOCK DIAGRAM



PIN DESCRIPTIONS

DIN	High speed, serial data input.
DLYDIN	Delayed data input.
VTH	Threshold bias control to the input comparators. -1.3V≤Vcm≤0V.
VCLKIN	AC-coupled clock input, typically driven from the VCLKOUT pin.
U, D	Phase error outputs of the phase/freq. comparator.
DOUT	Reclocked, regenerated data output.
VCC	+5.0V power supply connections.
VSS	-3.4V power supply.
VEE	-5.2V power supply pins.
VDDL	Ground connections.
VDDO	Output driver ground connection for data regenerator and phase/freq. comparator.

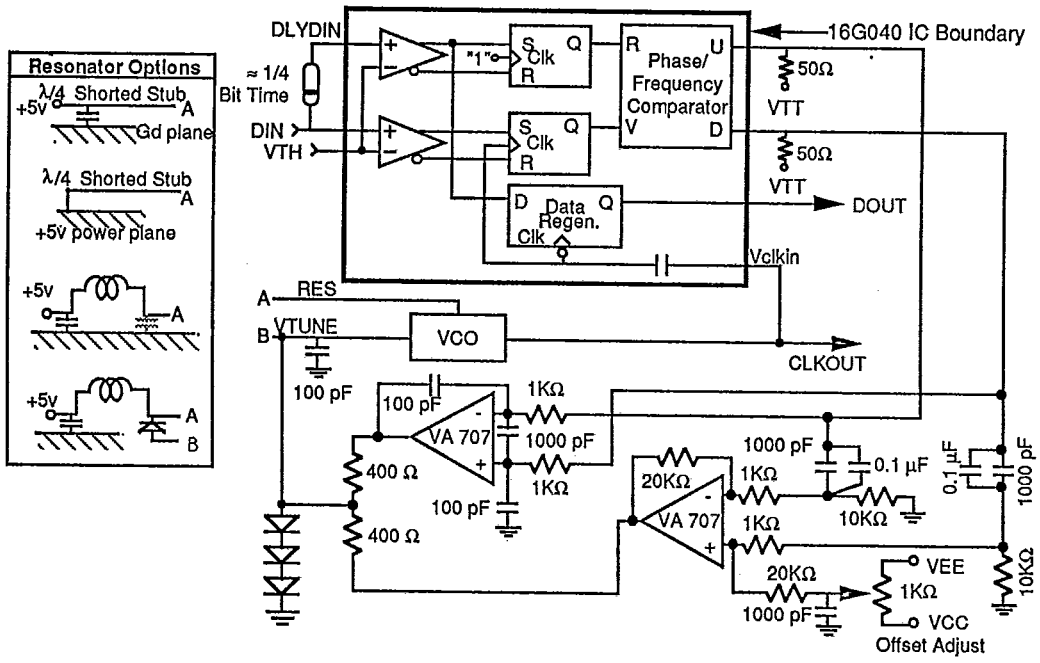


FIGURE 2

Typical Clock Recovery PLL Implementation

When the loop is in lock, the rising edges of "A" are exactly lined up with the rising edges in "CLK". This ensures that the falling edge-triggered D- type flip-flop, which is used as a "decision circuit" to detect the digital data, is clocking precisely in the middle of the data bit, and thus has maximum timing margin to prevent jitter-induced bit errors.

When the loop is phase locked, then both the PFC "U" and "D" outputs are low, resulting in a zero error voltage being applied to the loop filter. Therefore, the tendency is for the loop to hold its frequency once it is locked. This condition also occurs in the absence of any rising edges (often called "missed transitions") in the input data.

When the loop is locked, missing transitions will not cause loss of lock as long as the frequency of transitions exceeds 10 times the loop filter cutoff frequency, as a rule of thumb. However, during acquisition, long strings of "1's" and "0's" will cause an increase in loop acquisition time since these strings of constant data present no phase information to the loop. In this case, the effective phase detector gain factor (Kd) is reduced, according to: Kd effective = Ptr X Kd where Ptr is given by (number of transitions) ÷ (number of bits).

This factor can be called the "probability of transitions", or more accurately, the "transitions ratio" and is a measure of the spectral richness at the clock frequency of a digital data stream. A lower Kd (all other factors constant) lowers the closed loop gain of the PLL, resulting in a longer acquisition time.

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DEFINITION OF TERMS

LOOP ACQUISITION TIME
The total time taken by the PLL to establish lock is called the acquisition time. Acquisition time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth.

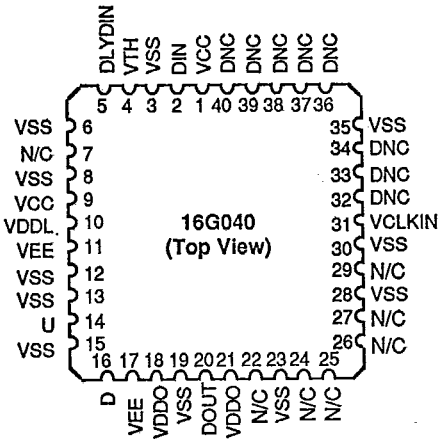
LOOP CAPTURE RANGE
The frequency range centered about the initial VCO free-running frequency over which the loop can acquire lock with the input signal. The capture range is a measure of how close the input signal frequency must be to that of the VCO to acquire lock assuming an initial condition of no incoming data. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system.

LOOP LOCK RANGE
The frequency range centered about the initial VCO free-running frequency over which the loop can track the input signal once lock has been achieved.

The lock range is limited by the range of error voltage that can be generated by the loop filter and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

FREQUENCY ACQUISITION
When the initial VCO frequency is unequal to the input data rate, the phase/frequency comparator produces "beat notes" which drive the VCO in the direction which will correct the frequency error. This acquisition process is highly complex and does not lend itself to simple mathematical analysis. The capture range of the loop is a function of the standard PLL parameters such as the phase detector gain, loop filter bandwidth, VCO control gain and the delay between the DIN and DLYDIN pins.

PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation.
N/C = no connection.
DNC = Do Not Connect

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ABSOLUTE MAXIMUM RATINGS
(Beyond which useful life may be impaired) (Notes 1, 4)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS	NOTES
TSTOR	Storage Temperature	-65 °C to +150 °C	
TJ	Junction Temperature	-55 °C to +150 °C	
TC	Case Temperature Under Bias	-55 °C to +125 °C	2
VDDO	Output Driver Supply Voltage	VSS to +1.0 V	
VCC	Supply Voltage	+1.0 V to +7.0 V	
VSS	Supply Voltage	-4.0 V to +0.5 V	
VEE	Supply Voltage	-7.0 V to VSS +0.5 V	
VIN	Voltage Applied to Any Input; Continuous VSS = -3.4 V, VEE = -5.2 V	-4.0 V to +0.5 V	
I IN	Current Into Any Input; Continuous	-0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VTT	Load Termination Supply	-6.0 V to VDDO +6.0 V	

Notes:
1. All voltages specified with VDDL= Gnd. Positive current is defined as current into the device.
2. TC is measured at case top.
3. Subject to IOUT and power dissipation limitations.
4. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode transistors, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case Operating Temperature	0	25	85	°C	1
VDDL	Ground Connections		Gnd		V	
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VCC	Supply Voltage	4.75	5.0	5.25	V	
VSS	Supply Voltage	-3.5	-3.4	-3.3	V	
VEE	Supply Voltage	-5.5	-5.2	-5.1	V	
VTT	Load Termination Supply Voltage	VSS	-2.0	-2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	2

Notes:
1. Tcase measured at case top. **HEATSINKING IS REQUIRED.** See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of all aspects of device thermal management. Heatsinks are available from GigaBit (See Section 5).
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.

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16G040 OPEN LOOP SPECIFICATIONS						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Data Inputs						
VIH	Input high voltage	-1.0		0.0	V	Vth = -1.3V
VIL	Input low voltage	-2.0		-1.6	V	Vth = -1.3V
CMR	Common mode range	-1.6		-1.0	V	
IIN	Input current	-300		300	µA	Vin = VIH max to VIL min
Clock Input						
Vckdc	DC voltage bias	-1.3		0	V	
Pck	Input power	0		13	dBm	
Phase/Frequency Comparator Outputs						
Kd	Large signal gain constant	250/π	300/π		mV/rad	Alternating 1,0 pattern
kd	Small signal gain constant	125/π	150/π		mV/rad	Alternating 1,0 pattern
VOH	Output peak voltage	-0.8	-0.5	-0.3	V	100Ω to Vtt = -2.0V term.
VOL	Output low level voltage	VTT	-1.8	-1.6	V	100Ω to Vtt = -2.0V term.
Data Output						
VOH	Output high level voltage	-0.8	-0.5	-0.3	V	50Ω to Vtt = -2.0V term.
VOL	Output low level voltage	Vtt	-1.8	-1.7	V	50Ω to Vtt = -2.0V term.
tdD	Clock output falling edge to data output delay		TBD		ps	
Power Supply Currents						
ICC	Loop components supply		63		mA	
IEE	currents		-128		mA	
ISS	VSS supply current		-121		mA	
PD	Power Dissipation		1.4		W	

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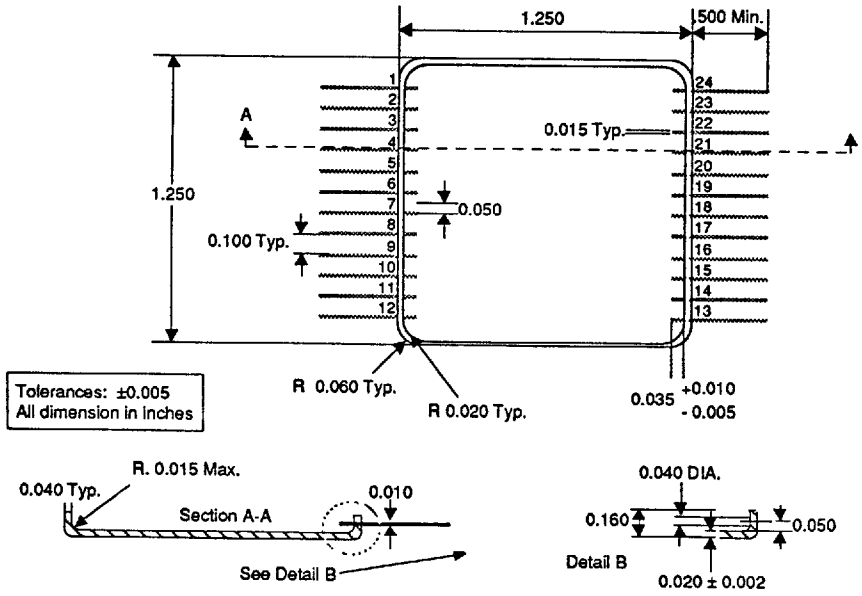
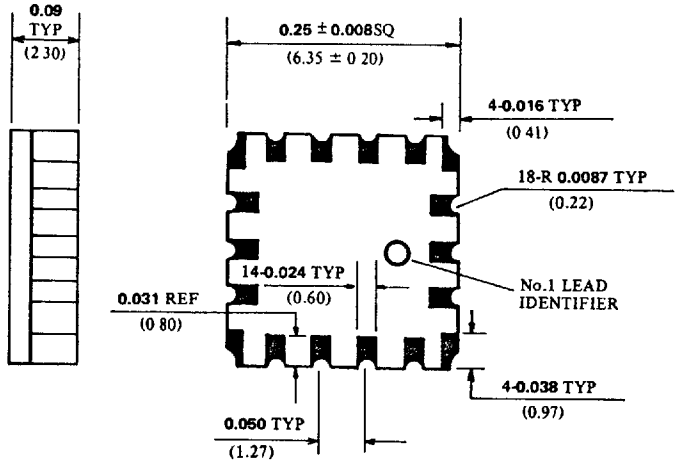
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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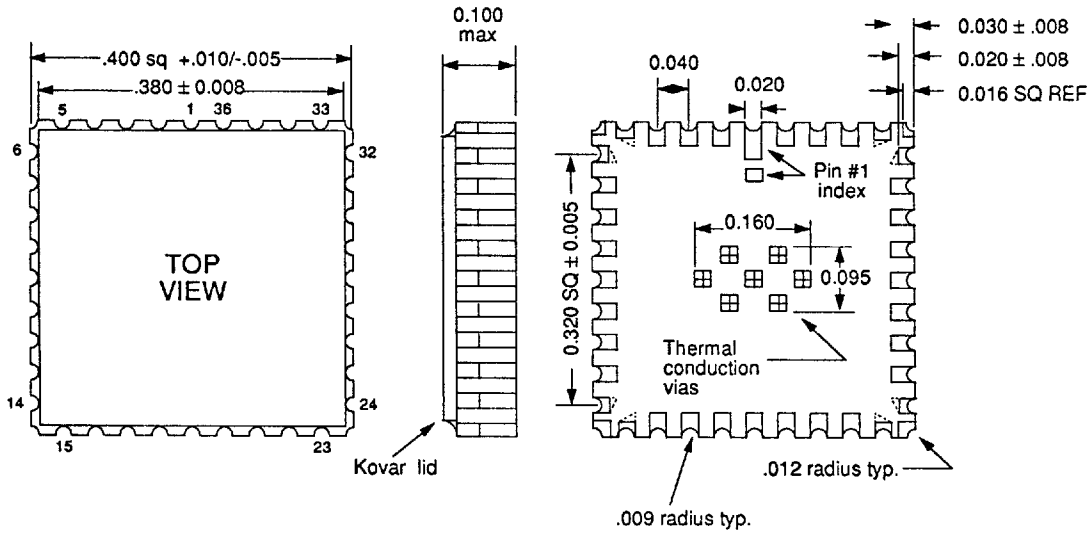
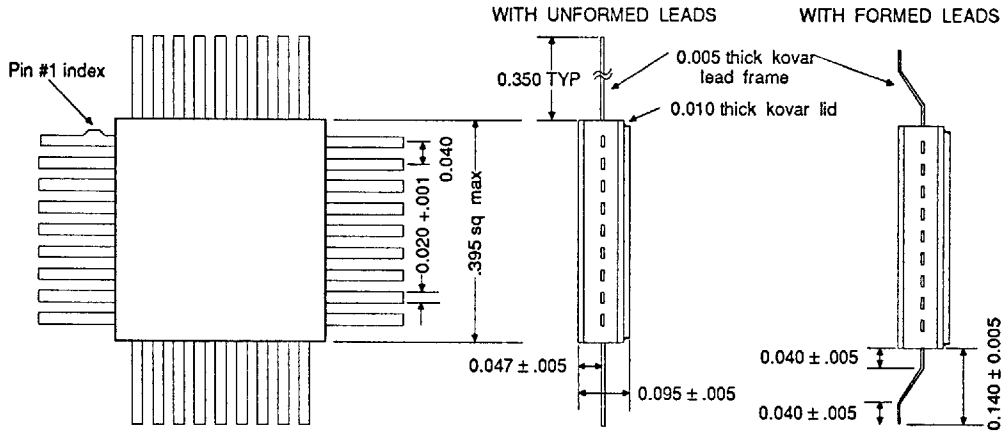
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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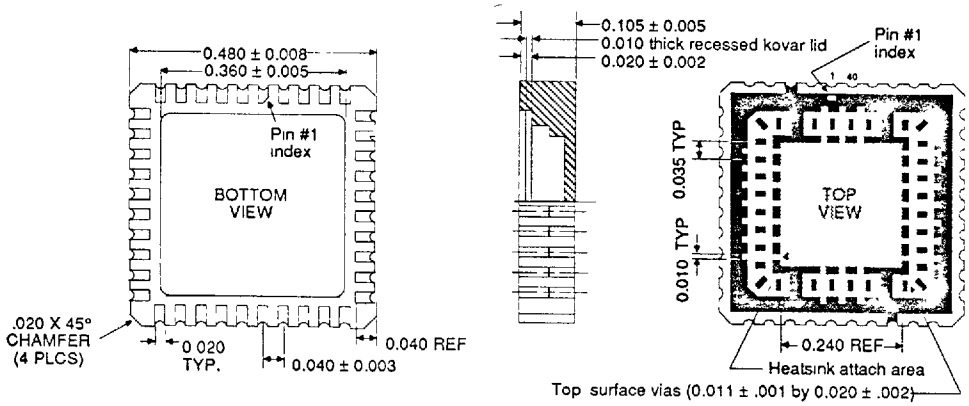
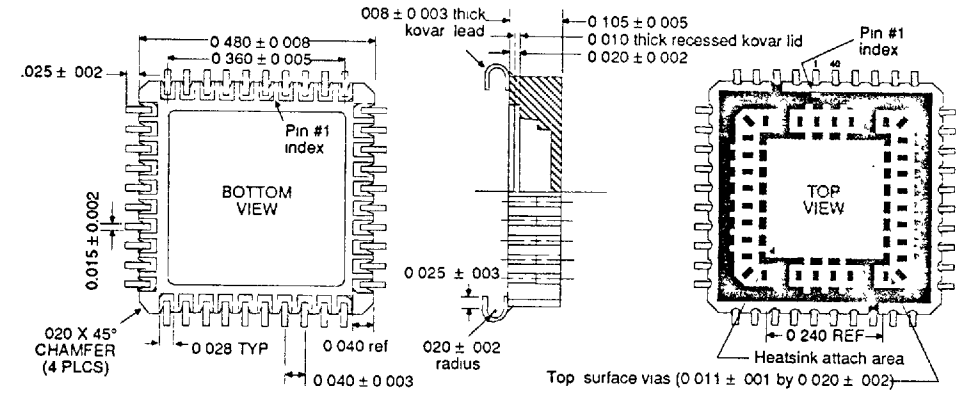
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

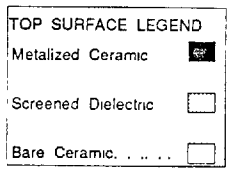


40 PIN LEADED CHIP CARRIER
TYPE C

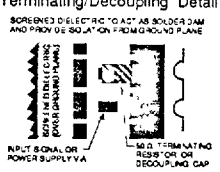


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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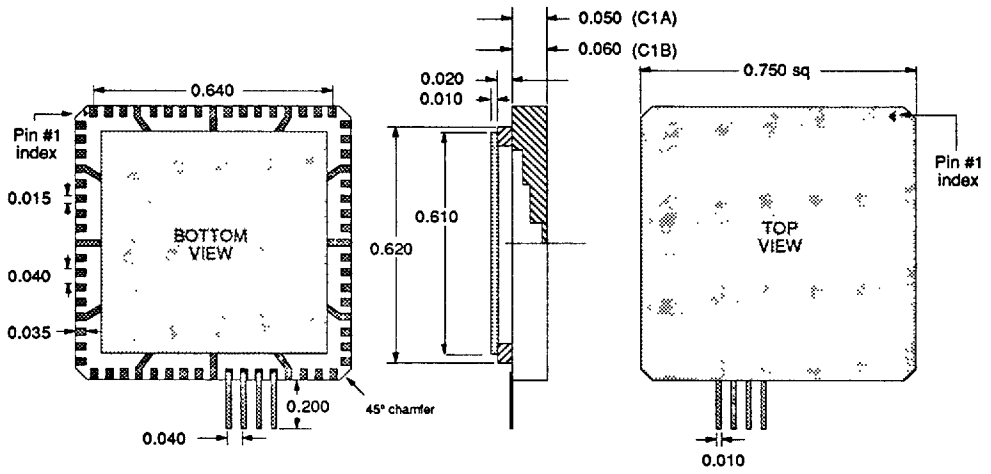
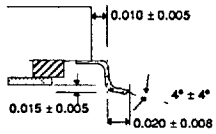
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3