# Am29C60A

## CMOS Cascadable 16-Bit Error Detection and Correction Unit

Advanced Micro Devices

### DISTINCTIVE CHARACTERISTICS

- Boosts Memory Reliability
  Corrects all single-bit errors. Detects all double- and some triple-bit errors. Reliability of dynamic RAM systems is increased more than sixty-fold.
- Very High Speed, Low Power
  Perfect for MOS microprocessors, minicomputers, main-frame systems, and engineering workstations.

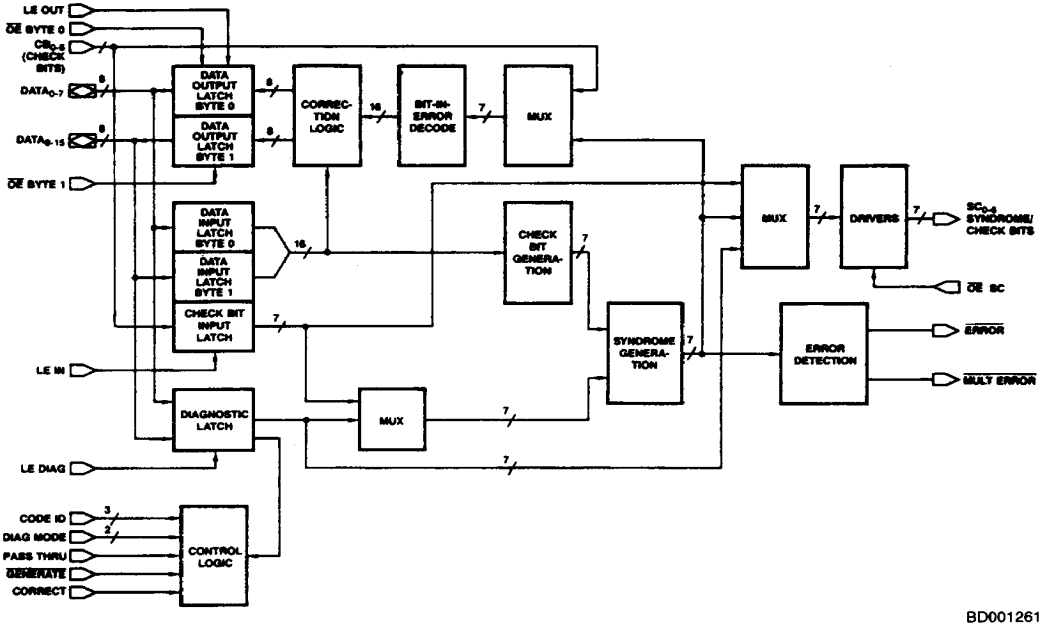
  High-performance systems can use the Am29C60 EDC in check-only mode to avoid memory system slowdown.
- Handles Data Words From 8 Bits to 64 Bits
  The Am29C60A EDC cascades: one EDC for 8 bits or 16 bits, two for 32 bits, four for 64 bits.
- Easy Byte Operations
  Separate byte enables on the data output latch simplify the steps and cut the time required for byte writes.
- Built-In Diagnostics
  The processor may completely exercise the EDC under software control to check for proper operation of the EDC.
- Compatible with the bipolar Am2960 Family.

### GENERAL DESCRIPTION

The Am29C60A Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am29C60A corrects any single-bit errors and detects all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The Am29C60A is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Am29C60A also features two diagnostic modes in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions.

### BLOCK DIAGRAM




BD001261



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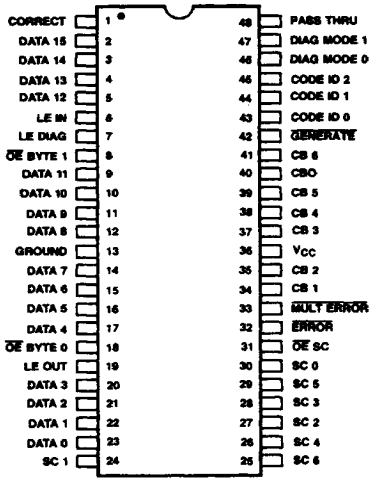
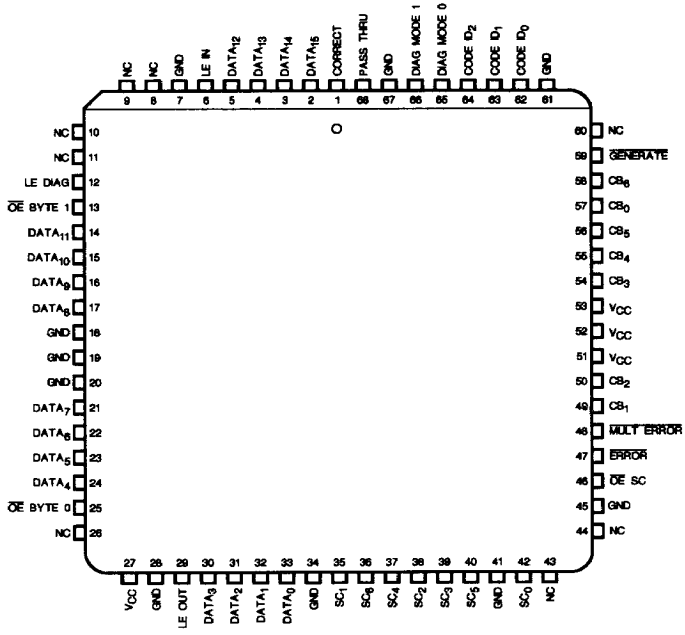
## CONNECTION DIAGRAMS
### Top View

#### DIPs




CD001421

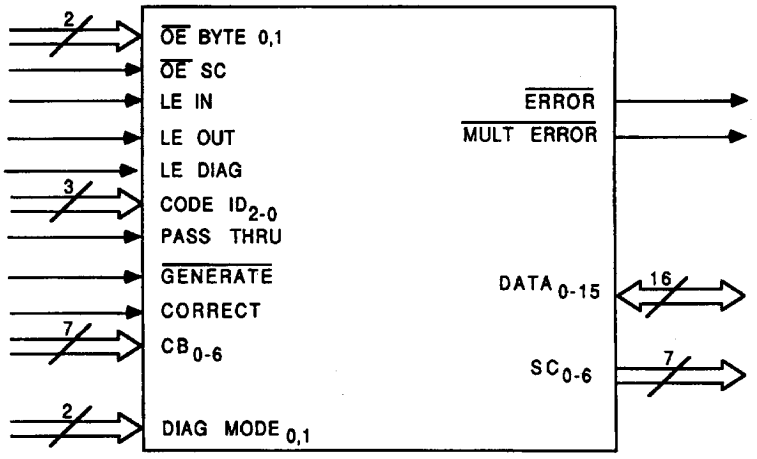
#### PLCC




CD010232

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL




LS002833

Die Size: .137" x .142"
Gate Count: 875

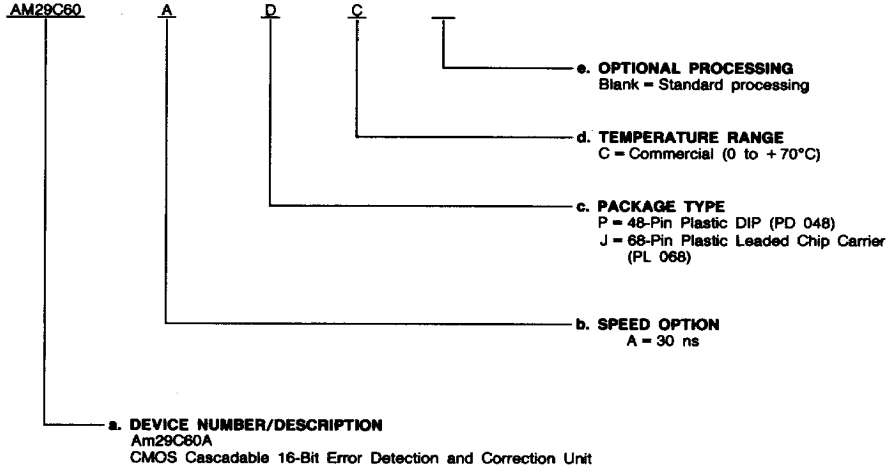
## RELATED AMD PRODUCTS

| Part No. | Description |
|---|---|
| Am29C668 | 4M Configurable Dynamic Memory Controller/Driver |
| Am29C660E | 9 ns 32-Bit Cascadable EDC |
| Am29C983A | 9-Bit x 4-Port Multikple Bus Exchange, High Speed |
| Am29C985 | 9-Bit x 7-Port Multiple Bus Exchange w/Parity |
| Am29C676 | 11-Bit DRAM Driver |
| Am2965/6 | 8-Bit DRAM Driver (Inverting, Non-inverting) |

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| AM29C60A | PC, JC |

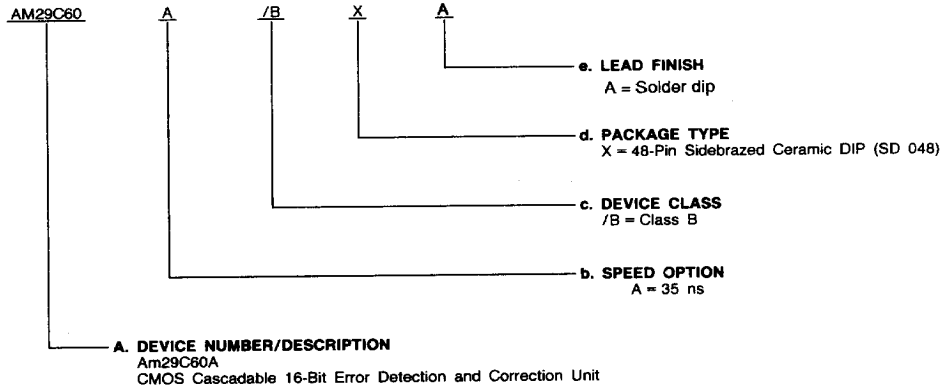
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Device Class**
**d. Package Type**
**e. Lead Finish**




| Valid Combinations | |
|---|---|
| AM29C60A | /BXA |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A tests consists of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

## PIN DESCRIPTION

**$CB_{0-6}$ Check Bits (Input)**
The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.

**CODE $ID_{2-0}$ Code Identification (Input)**
These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits, and their respective modified Hamming codes are designated 16/22, 32/39, and 64/72. Special CODE ID input 001 ($ID_2$, $ID_1$, $ID_0$) is also used to instruct the EDC to take the signals CODE $ID_{2-0}$, DIAG $MODE_{0-1}$, CORRECT, and PASS THRU from the Diagnostic Latch, rather than from the input control lines.

**CORRECT Correct (Input)**
When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When the signal is LOW, the EDC drives data directly from the Data Input Latch to the Data Output Latch without correction.

**$DATA_{0-15}$ Data (Input/Output; Three State)**
These bidirectional data lines provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

**DIAG $MODE_{0-1}$ Diagnostic Mode Select (Input)**
These two lines control the initialization and diagnostic operation of the EDC.

**$\overline{\text{ERROR}}$ Error Detected (Output)**
When the EDC is in Detect or Correct Mode, this output goes LOW if one or more syndrome bits are asserted, indicating one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.

**$\overline{\text{GENERATE}}$ Generate Check Bits (Input)**
When this input is LOW, the EDC is in the Check Bit Generate Mode. When HIGH, the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes, the EDC detects single and multiple errors and generates syndrome bits based on the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected; corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs, and indicates in a coded form the number of errors and the bit-in-error.

**LE DIAG Diagnostic Latch Enable (Input)**
When this input is HIGH, the Diagnostic Latch follows the 16-bit data on the input lines. When it is LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{2-0}$, DIAG $MODE_{0-1}$, CORRECT, and PASS THRU.

**LE IN Latch Enable – Data Input Latch (Input)**
This input controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

**LE OUT Latch Enable – Data Output Latch (Input)**
This input controls the latching of the Data Output Latch. When it is LOW, the Data Output Latch is latched to its previous state. When it is HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed unchanged through the correction network into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

**$\overline{\text{MULT ERROR}}$ Multiple Errors Detected (Output)**
When the EDC is in Detect or Correct Mode, this output, if LOW, indicates that two or more bit errors have been detected. If HIGH, either one or no errors have been detected. In Generate Mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.

**$\overline{\text{OE}}$ BYTE 0, 1 Output Enable Bytes 0, 1 (Input)**
These lines control the three-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch, and when HIGH, these lines force the Data Output Latch into the high-impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

**$\overline{\text{OE}}$ SC Output Enable, Syndrome/Check Bits (Input)**
When this input is LOW, the three-state output lines $SC_{0-6}$ are enabled. When the input is HIGH, the SC outputs are in the high-impedance state.

**PASS THRU Pass Thru (Input)**
This line, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs ($SC_{0-6}$) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

**$SC_{0-6}$ Syndrome/Check Bits (Output; Three State)**
These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are three-state outputs.

## FUNCTIONAL DESCRIPTION

The CMOS version saves system power with no loss in performance. The Am29C60A is a performance upgrade of the Am29C60 but is not a parametric equivalent to the bipolar Am2960A.

The CMOS EDC circuit contains proprietary output buffers to decrease the on-chip-generated noise caused by current changes through fast logic. This minimizes "ground bounce" and ensures proper chip performance of these high-speed CMOS solutions in the system environment.

Please refer to EDC Product Specifications Booklet (Literature #03565E/0) for detailed functional description and applications information.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Case)
Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
High Output State ..... −0.5 V to $V_{CC}$ Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5.0 mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Ambient Temperature ($T_A$) ..... 0°C to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Case Temperature ($T_C$) ..... −55°C to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −300 µA | | $V_{CC}$ − 0.2 | | V |
| | | | MIL $I_{OH}$ = −12 mA | | 2.4 | | |
| | | | COM'L $I_{OH}$ = −15 mA | | 2.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 300 µA | | | 0.2 | V |
| | | | MIL $I_{OL}$ = 8 mA | | | 0.5 | |
| | | | COM'L $I_{OL}$ = 16 mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 5) | | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 5) | | | | 0.8 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max. $V_{IN}$ = 0.5 V | $DATA_{0-15}$ (Note 3) | | | −10 | µA |
| | | | All Other Inputs | | | −10 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. $V_{IN}$ = 2.7 V | $DATA_{0-15}$ (Note 3) | | | 10 | µA |
| | | | All Other Inputs | | | 10 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = Max., | | | | 10 | µA |
| $I_{OZH}$ $I_{OZL}$ | Off State (High-Impedance) Output Current | $V_{CC}$ Max. | $DATA_{0-15}$ | $V_O$ = 2.4 | | 40 | µA |
| | | | | $V_O$ = 0.5 | | −40 | |
| | | | $SC_{0-6}$ | $V_O$ = 2.4 | | 40 | |
| | | | | $V_O$ = 0.5 | | −40 | |
| $I_{OS}$ | Output Short-Circuit Current (Note 2) | $V_{CC}$ = Max. $V_O$ = 0 V | | | −30 | −140 | mA |
| $I_{CC}$ | Power Supply (Note 4) | $V_{CC}$ = Max. | COM'L | | | 50 | mA |
| | | | MIL | | | 50 | |
| | | $V_{CC}$ = 5.0 V (Note 6) | $T_A$ = +25°C | | | 30 | |
| $I_{CCQC}$ | Quiescent Power Supply (CMOS) | $V_{CC}$ = Max. | COM'L | | | 5 | mA |
| | | | MIL | | | 5 | |
| | | $V_{CC}$ = 5.0 V (Note 6) | $T_A$ = +25°C | | | 2 | |

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Range for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
3. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with outputs disabled (high impedance).
4. Worst-case $I_{CC}$ is at minimum temperature. Test conditions:
$C_L$ = 50 pF, f = 10 MHz, $V_{IN}$ = 50% duty cycle for all inputs at 3.4 V and 0.4 V, $\overline{OE}$ = GND.
5. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
6. Not production tested. Typical $I_{CC}$ ($V_{CC}$ = 5.0 V and $T_A$ = 25°C) represents nominal units.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Notes 1 and 2)

The following table specifies the guaranteed device performance over the commercial operating range of 0°C to +70°C (ambient), with $V_{CC}$ 4.75 to 5.25 V. All input switching is between 0 V and 3 V at 1 V/ns, and measurements are made at 1.5 V. All outputs have maximum DC load. All units are in nanoseconds (ns).

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 1 | $t_{PD}$ | $DATA_{0-15}$ (Note 3) | $SC_{0-6}$ | | 20 |
| | | | $DATA_{0-15}$ | | 30 |
| | | | $\overline{ERROR}$ | | 20 |
| | | | $\overline{MULT\ ERROR}$ | | 23 |
| 2 | $t_{PD}$ | $CB_{0-6}$ ($CODE\ ID_{2-0}$ 000, 011) | $SC_{0-6}$ (Note 7) | | 14 |
| | | | $DATA_{0-15}$ | | 25 |
| | | | $\overline{ERROR}$ | | 20 |
| | | | $\overline{MULT\ ERROR}$ | | 23 |
| 3 | $t_{PD}$ | $CB_{0-6}$ ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111) | $SC_{0-6}$ (Note 7) | | 17 |
| | | | $DATA_{0-15}$ | | 25 |
| | | | $\overline{ERROR}$ | | 20 |
| | | | $\overline{MULT\ ERROR}$ | | 23 |
| 4 | $t_{PD}$ | $\overline{GENERATE}$ | $SC_{0-6}$ (Note 7) | | 17 |
| | | | $DATA_{0-15}$ | | 25 |
| | | | $\overline{ERROR}$ (Note 7) | | 16 |
| | | | $\overline{MULT\ ERROR}$ | | 17 |
| 5 | $t_{PD}$ | CORRECT (Not Internal Control Mode) | $SC_{0-6}$ | | - |
| | | | $DATA_{0-15}$ | | 20 |
| | | | $\overline{ERROR}$ | | - |
| | | | $\overline{MULT\ ERROR}$ | | - |
| 6 | $t_{PD}$ | DIAG MODE (Not Internal Control Mode) | $SC_{0-6}$ (Note 7) | | 22 |
| | | | $DATA_{0-15}$ | | 27 |
| | | | $\overline{ERROR}$ (Note 7) | | 19 |
| | | | $\overline{MULT\ ERROR}$ (Note 7) | | 21 |
| 7 | $t_{PD}$ | PASS THRU (Not Internal Control Mode) | $SC_{0-6}$ | | 22 |
| | | | $DATA_{0-15}$ | | 25 |
| | | | $\overline{ERROR}$ | | 18 |
| | | | $\overline{MULT\ ERROR}$ | | 21 |
| 8 | $t_{PD}$ | $CODE\ ID_{2-0}$ | $SC_{0-6}$ | | 23 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ | | 25 |
| | | | $\overline{MULT\ ERROR}$ | | 28 |

Notes: See notes at end of this section.

**SWITCHING CHARACTERISTICS** over **COMMERCIAL** operating range (Cont'd.)

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 9 | $t_{PD}$ | LE IN (From latched to transparent) | $SC_{0-6}$ | | 22 |
| | | | $DATA_{0-15}$ | | 32 |
| | | | $\overline{ERROR}$ | | 22 |
| | | | $\overline{MULT\ ERROR}$ | | 25 |
| 10 | $t_{PD}$ | LE OUT (From latched to transparent) | $SC_{0-6}$ | | – |
| | | | $DATA_{0-15}$ | | 13 |
| | | | $\overline{ERROR}$ | | – |
| | | | $\overline{MULT\ ERROR}$ | | – |
| 11 | $t_{PD}$ | LE DIAG (From latched to transparent; Not Internal Control Mode) | $SC_{0-6}$ | | 22 |
| | | | $DATA_{0-15}$ | | 32 |
| | | | $\overline{ERROR}$ | | 22 |
| | | | $\overline{MULT\ ERROR}$ | | 25 |
| 12 | $t_{PD}$ | Internal Control Mode: LE DIAG (From latched to transparent) | $SC_{0-6}$ | | 28 |
| | | | $DATA_{0-15}$ | | 38 |
| | | | $\overline{ERROR}$ | | 28 |
| | | | $\overline{MULT\ ERROR}$ | | 31 |
| 13 | $t_{PD}$ | Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic latch) | $SC_{0-6}$ | | 28 |
| | | | $DATA_{0-15}$ | | 38 |
| | | | $\overline{ERROR}$ | | 28 |
| | | | $\overline{MULT\ ERROR}$ | | 31 |
| 14 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE IN | 5 | |
| 15 | $t_{HOLD}$ | | | 3 | |
| 16 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) | | 5 | |
| 17 | $t_{HOLD}$ | | | 3 | |
| 18 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE OUT | 24 | |
| 19 | $t_{HOLD}$ | | | 2 | |
| 20 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) (CODE ID 000, 011) | | 21 | |
| 21 | $t_{HOLD}$ | | | 0 | |
| 22 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) (CODE ID 010, 100, 101, 110, 111) | | 21 | |
| 23 | $t_{HOLD}$ | | | 0 | |
| 24 | $t_{SET}$ | $\overline{GENERATE}$ (Notes 4, 5) | | 26 | |
| 25 | $t_{HOLD}$ | | | 0 | |
| 26 | $t_{SET}$ | CORRECT (Notes 4, 5) | | 22 | |
| 27 | $t_{HOLD}$ | | | 0 | |
| 28 | $t_{SET}$ | DIAG MODE (Notes 4, 5) | | 22 | |
| 29 | $t_{HOLD}$ | | | 0 | |
| 30 | $t_{SET}$ | PASS THRU (Notes 4, 5) | | 22 | |
| 31 | $t_{HOLD}$ | | | 0 | |
| 32 | $t_{SET}$ | $CODE\ ID_{2-0}$ (Notes 4, 5) | | 25 | |
| 33 | $t_{HOLD}$ | | | 0 | |

Notes: See notes at end of this section.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cont'd.)

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 34 | $t_{SET}$ | LE IN (Notes 4, 5) | LE OUT | 28 | |
| 35 | $t_{HOLD}$ | | | 0 | |
| 36 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE DIAG | 3 | |
| 37 | $t_{HOLD}$ | | | 5 | |
| 38 | $t_{EN}$ | $\overline{OE}$ BYTE 0,1 ENABLE (Note 6) | $DATA_{0-15}$ | | 14 |
| 39 | $t_{DIS}$ | | | | 23 |
| 40 | $t_{EN}$ | $\overline{OE}$ SC DISABLE (Note 6) | $SC_{0-6}$ | | 16 |
| 41 | $t_{DIS}$ | | | | 21 |
| 42 | $t_{PW}$ | MINIMUM PULSE WIDTH: LE IN, LE OUT, LE DIAG | | 12 | |

Notes: 1. $C_L = 50$ pF.
2. Certain parameters are combinational propagation delay calculations.
3. Data IN or LE IN to Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Setup and Hold times relative to Latch Enables (Latching up data).
5. Setup and Hold times are not tested, but are guaranteed by characterization.
6. Output disable tests specified with $C_L = 5$ pF and measured to 0.5 V change of output voltage level. Testing is performed at $C_L = 50$ pF and correlated to $C_L = 5$ pF.
7. Not production tested. Guaranteed by characterization.

**SWITCHING CHARACTERISTICS** over **MILITARY** operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 1 and 2)

The following table specifies the guaranteed device performance over the Military operating range of −55°C to +125°C (case), with $V_{CC}$ 4.5 to 5.5 V. All input switching is between 0 V and 3 V at 1 V/ns and measurements are made at 1.5 V. All outputs have maximum DC load. All units are in nanoseconds (ns).

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 1 | $t_{PD}$ | $DATA_{0-15}$ (Note 3) | $SC_{0-6}$ | | 24 |
| | | | $DATA_{0-15}$ | | 35 |
| | | | $\overline{ERROR}$ | | 24 |
| | | | $\overline{MULT\ ERROR}$ | | 27 |
| 2 | $t_{PD}$ | $CB_{0-6}$ ($CODE\ ID_{2-0}$ 000, 011) | $SC_{0-6}$ (Note 7) | | 17 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ | | 24 |
| | | | $\overline{MULT\ ERROR}$ | | 27 |
| 3 | $t_{PD}$ | $CB_{0-6}$ ($CODE\ ID_{2-0}$ 010, 100, 101, 110, 111) | $SC_{0-6}$ (Note 7) | | 19 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ | | 24 |
| | | | $\overline{MULT\ ERROR}$ | | 27 |
| 4 | $t_{PD}$ | $\overline{GENERATE}$ | $SC_{0-6}$ (Note 7) | | 20 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ (Note 7) | | 21 |
| | | | $\overline{MULT\ ERROR}$ | | 25 |
| 5 | $t_{PD}$ | CORRECT (Not Internal Control Mode) | $SC_{0-6}$ | | – |
| | | | $DATA_{0-15}$ | | 25 |
| | | | $\overline{ERROR}$ | | – |
| | | | $\overline{MULT\ ERROR}$ | | – |
| 6 | $t_{PD}$ | DIAG MODE (Not Internal Control Mode) | $SC_{0-6}$ (Note 7) | | 25 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ (Note 7) | | 21 |
| | | | $\overline{MULT\ ERROR}$ (Note 7) | | 24 |
| 7 | $t_{PD}$ | PASS THRU (Not Internal Control Mode) | $SC_{0-6}$ | | 25 |
| | | | $DATA_{0-15}$ | | 28 |
| | | | $\overline{ERROR}$ | | 21 |
| | | | $\overline{MULT\ ERROR}$ | | 24 |
| 8 | $t_{PD}$ | $CODE\ ID_{2-0}$ | $SC_{0-6}$ | | 26 |
| | | | $DATA_{0-15}$ | | 31 |
| | | | $\overline{ERROR}$ | | 28 |
| | | | $\overline{MULT\ ERROR}$ | | 31 |

Notes: See notes at end of this section.

**SWITCHING CHARACTERISTICS** over **MILITARY** operating range (Cont'd.)

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 9 | $t_{PD}$ | LE IN (From latched to transparent) | $SC_{0-6}$ | | 26 |
| | | | $DATA_{0-15}$ | | 37 |
| | | | $\overline{ERROR}$ | | 26 |
| | | | $\overline{MULT\ ERROR}$ | | 29 |
| 10 | $t_{PD}$ | LE OUT (From latched to transparent) | $SC_{0-6}$ | | – |
| | | | $DATA_{0-15}$ | | 16 |
| | | | $\overline{ERROR}$ | | – |
| | | | $\overline{MULT\ ERROR}$ | | – |
| 11 | $t_{PD}$ | LE DIAG (From latched to transparent; Not Internal Control Mode) | $SC_{0-6}$ | | 24 |
| | | | $DATA_{0-15}$ | | 37 |
| | | | $\overline{ERROR}$ | | 26 |
| | | | $\overline{MULT\ ERROR}$ | | 29 |
| 12 | $t_{PD}$ | Internal Control Mode: LE DIAG (From latched to transparent) | $SC_{0-6}$ | | 30 |
| | | | $DATA_{0-15}$ | | 43 |
| | | | $\overline{ERROR}$ | | 32 |
| | | | $\overline{MULT\ ERROR}$ | | 35 |
| 13 | $t_{PD}$ | Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic latch) | $SC_{0-6}$ | | 30 |
| | | | $DATA_{0-15}$ | | 43 |
| | | | $\overline{ERROR}$ | | 32 |
| | | | $\overline{MULT\ ERROR}$ | | 35 |
| 14 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE IN | 5 | |
| †15 | $t_{HOLD}$ | | | 3 | |
| 16 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) | | 5 | |
| †17 | $t_{HOLD}$ | | | 3 | |
| 18 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE OUT | 27 | |
| †19 | $t_{HOLD}$ | | | 2 | |
| 20 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) (CODE ID 000, 011) | | 24 | |
| †21 | $t_{HOLD}$ | | | 0 | |
| 22 | $t_{SET}$ | $CB_{0-6}$ (Notes 4, 5) (CODE ID 010, 100, 101, 110, 111) | | 24 | |
| †23 | $t_{HOLD}$ | | | 0 | |
| 24 | $t_{SET}$ | $\overline{GENERATE}$ (Notes 4, 5) | | 29 | |
| †25 | $t_{HOLD}$ | | | 0 | |
| 26 | $t_{SET}$ | CORRECT (Notes 4, 5) | | 25 | |
| †27 | $t_{HOLD}$ | | | 0 | |
| 28 | $t_{SET}$ | DIAG MODE (Notes 4, 5) | | 25 | |
| †29 | $t_{HOLD}$ | | | 0 | |
| 30 | $t_{SET}$ | PASS THRU (Notes 4, 5) | | 25 | |
| †31 | $t_{HOLD}$ | | | 0 | |
| 32 | $t_{SET}$ | CODE $ID_{2-0}$ (Notes 4, 5) | | 28 | |
| †33 | $t_{HOLD}$ | | | 0 | |

Notes: See notes at end of this section.

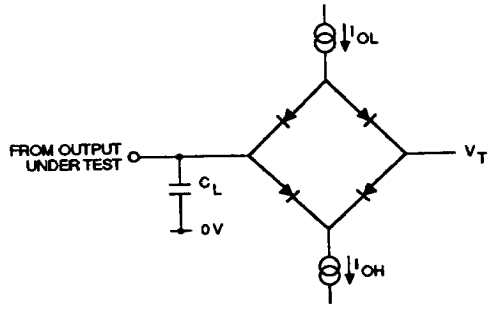
**SWITCHING CHARACTERISTICS** over **MILITARY** operating range (Cont'd.)

| No. | Parameter Symbol | Data Path Description | | Am29C60A | |
|---|---|---|---|---|---|
| | | From Input | To Output | Min. | Max. |
| 34 | $t_{SET}$ | LE IN (Notes 4, 5) | LE OUT | 30 | |
| †35 | $t_{HOLD}$ | | | 0 | |
| 36 | $t_{SET}$ | $DATA_{0-15}$ (Notes 4, 5) | LE DIAG | 5 | |
| †37 | $t_{HOLD}$ | | | 3 | |
| 38 | $t_{EN}$ | $\overline{OE}$ BYTE 0,1 ENABLE (Note 6) | $DATA_{0-15}$ | | 28 |
| 39 | $t_{DIS}$ | | | | 25 |
| 40 | $t_{EN}$ | $\overline{OE}$ SC DISABLE (Note 6) | $SC_{0-6}$ | | 28 |
| 41 | $t_{DIS}$ | | | | 25 |
| 42 | $t_{PW}$ | MINIMUM PULSE WIDTH: LE IN, LE OUT, LE DIAG | | 12 | |

Notes: 1. $C_L = 50$ pF.
2. Certain parameters are combinational propagation delay calculations.
3. Data IN or LE IN to Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Setup and Hold times relative to Latch Enables (Latching up data).
5. Setup and Hold times are not tested, but are guaranteed by characterization.
6. Output disable tests specified with $C_L = 5$ pF and measured to 0.5 V change of output voltage level. Testing is performed at $C_L = 50$ pF and correlated to $C_L = 5$ pF.
7. Not production tested. Guaranteed by characterization.

† = Not Included in Group A Tests.

## SWITCHING TEST CIRCUIT

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Notes: 1. $C_L = 50$ pF for all tests except output enable/disable (includes scope probe, wiring, and stray capacitance without device in test fixture).
2. $C_L = 5$ pF for output enable/disable tests.
3. $V_T = 1.5$ V.

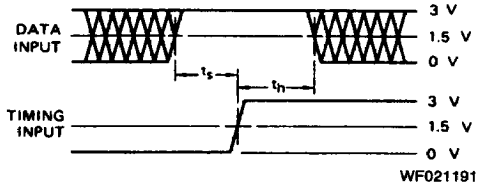
### Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Ensure the part is adequately decoupled at the test head. Large changes in $V_{CC}$ current as the device switches may cause erroneous function failures due to $V_{CC}$ changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach $V_{IL}$ or $V_{IH}$ until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Changing the CODE ID inputs can cause loss of data in some of the Am29C60 internal latches. Specifically, the entire checkbit latch and bits 6 and 7 of the diagnostic latch are indeterminate after a change in CODE ID inputs.

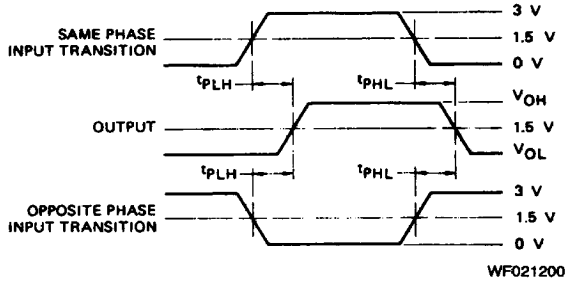
Logic simulations should store "x" (i.e., "don't care") in these bits after CODE ID change. Test programs should reload these registers before they are used.

## SWITCHING TEST WAVEFORMS

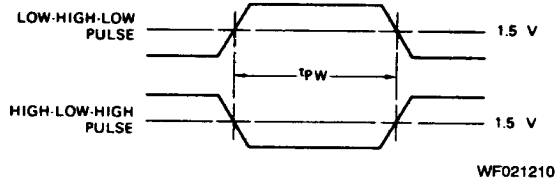



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

**Setup and Hold Times**



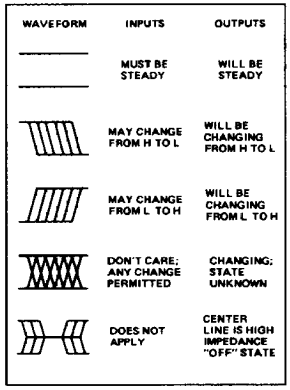

**Propagation Delay**



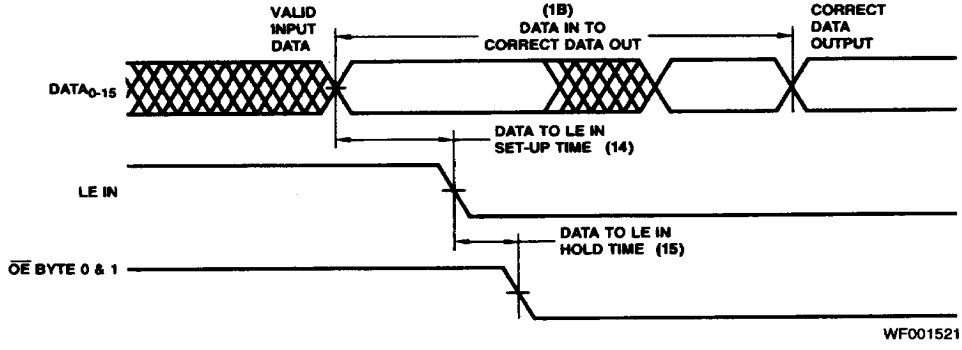

**Pulse Width**

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS




KS000010

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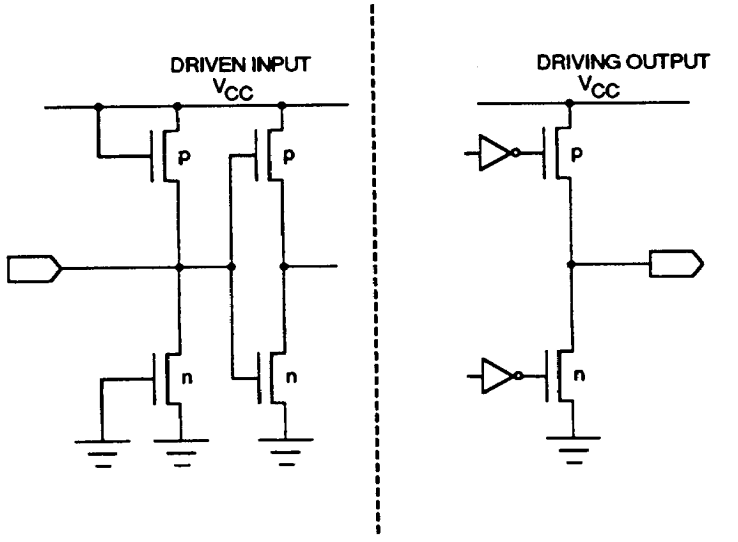
**DATA IN/LE IN to Correct DATA OUT**

## EQUIVALENT INPUT/OUTPUT CIRCUIT DIAGRAMS

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