Aptos SEMICONDUCTOR

AP9A110

128K x 8 High Output Drive, High-Speed CMOS Static RAM with 2V Data Retention

Features

- Drives a 150 pF load vs. 30 pF industry-standard load
- Fast access times: 10, 12, 15 and 20 ns
- 2V/250 µA standby
- Fast output enable (t_{DOE}) for cache applications
- Low active power: 350 mW at 20 ns
- Low standby power
- Fully static operation, no clock or refresh required
- TTL-compatible inputs and outputs
- Single +5V power supply
- Packaged in industry standard 32-Pin SOJ

Functional Description

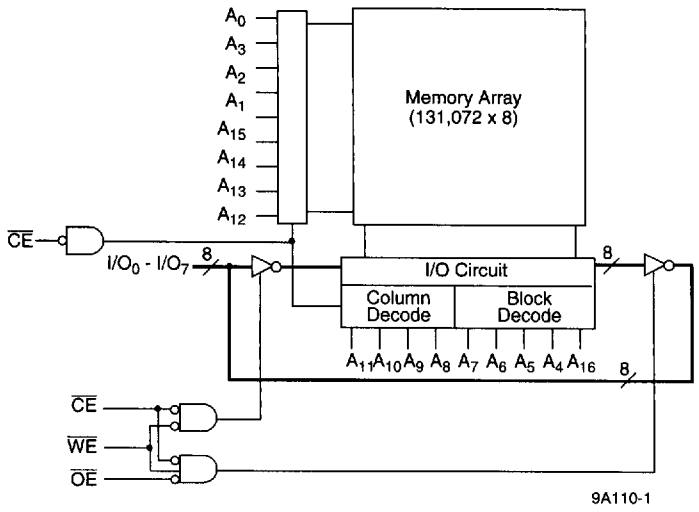
The Aptos AP9A110 is a high speed, low power, 128K word by 8-bit CMOS static RAM. It is fabricated using Aptos' high-performance CMOS, double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns (Max).

When Chip Enable ($\overline{CE}$) is HIGH the device assumes a standby mode at which the power dissipation can be reduced down to 50 µW (Typ.) at CMOS input levels at 2V V_{CC}.

Easy memory expansion is provided by using asserted LOW $\overline{CE}$ and asserted LOW output enable inputs ($\overline{OE}$). The asserted LOW write enable ($\overline{WE}$) controls both writing and reading of the memory.

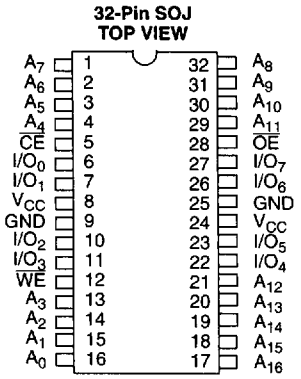
The AP9A110 is pin-compatible with other 128K x 8 center power and ground SRAMs in the SOJ package.

Block Diagram



9A110-1

Pin Configuration



9A110-2

Selection Guide

	AP9A110-10	AP9A110-12	AP9A110-15	AP9A110-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)	100	90	85	70
Maximum Standby Current (mA)	15	15	15	15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

V_{CC} Supply Relative to GND ..... -1.0 V to +7.0 V

Voltage on Any Pin Relative to GND ..... -0.5 V to V_{CC} +0.5 V

Short Circuit Output Current [1] ..... ±50 mA

Power Dissipation ..... 1.0 W

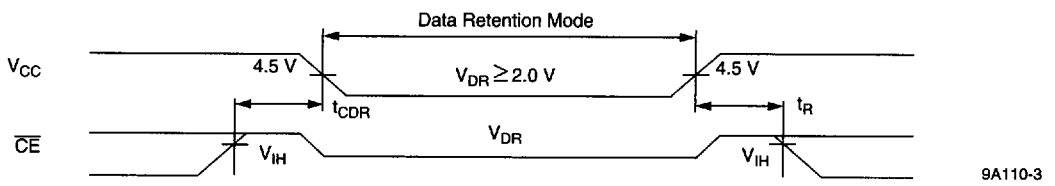
Electrical Characteristics Over the Operating Range (0 °C ≤ T_A ≤ 70 °C, V_{CC} = 5V ±10%) *-Commercial*

Symbol	Parameter	Test Conditions	9A110-10		9A110-12		9A110-15		9A110-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = fmax.		100		90		85		70	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, f = 0		60		60		60		60	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f=fmax.		15		15		15		15	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2 V, f = 0		2		2		2		2	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-1	1	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = - 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage [2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Data Retention Characteristics

Symbol	Description	Test Conditions [3]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	V_{CC} = V_{DR} = 2.0V, $\overline{CE}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2 V		250	µA
t_{CDR} [4]	Chip Deselect to Data Retention Time		0		ns
t_R [4]	Operation Recovery Time		t_{RC}		ns

Data Retention Wave Form



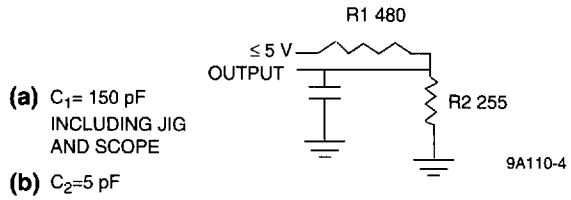
Capacitance [4]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	5	pF

Notes:

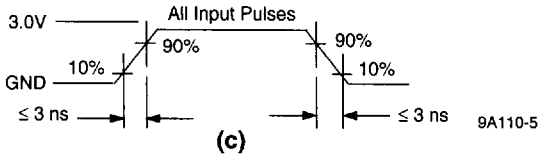
1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. V_{IL} = -3.0 V for pulse width less than 3 ns.
3. Tested initially and after any design or process changes that may effect these parameters.
4. No input may exceed V_{CC} +0.5V.

AC Test Loads and Waveforms [5, 6]



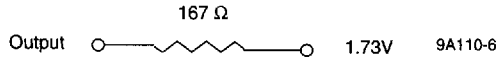
(a) C_1= 150 pF INCLUDING JIG AND SCOPE

(b) C_2=5 pF INCLUDING JIG AND SCOPE



(c)

Equivalent to: Thevenin Equivalent



Switching Characteristics Over the Operating Range [7, 8, 9, 10]

Parameter	Description	9A110-10		9A110-12		9A110-15		9A110-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address Access Time		10		12		15		20	ns
t_{OHA}	Output Hold Time	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ Access Time		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		4		5		7		8	ns
t_{LZOE}	$\overline{OE}$ to Low-Z Output	0		0		0		0		ns
t_{HZOE} [6]	$\overline{OE}$ to High-Z Output		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ to Low-Z Output	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ to High-Z Output		4		6		8		9	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		10		12		15		20	ns
Write Cycle [11]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ to Write End	8		8		10		12		ns
t_{AW}	Address to Set-up Time to Write End	8		8		10		12		ns
t_{HA}	Address Hold to Write End	0		0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		0		ns
t_{PWE1} [12]	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	8		8		10		12		ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	10		12		12		15		ns
t_{SD}	Data Set-up to Write End	6		6		7		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE} [6]	$\overline{WE}$ LOW to High-Z Output		6		6		7		9	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	2		2		2		2		ns

Notes:

5. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
6. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.
7. $\overline{WE}$ is HIGH for a Read Cycle.
8. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
9. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.
10. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.
11. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any signal can be deasserted to terminate the write. The Data Input Set-up and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
12. Tested with $\overline{OE}$ High.

Pin Descriptions

A_0 - A_{16}: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

$\overline{CE}$: Chip Enable Input

$\overline{CE}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}$ is asserted (LOW) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is deasserted.

$\overline{WE}$: Write Enable Input

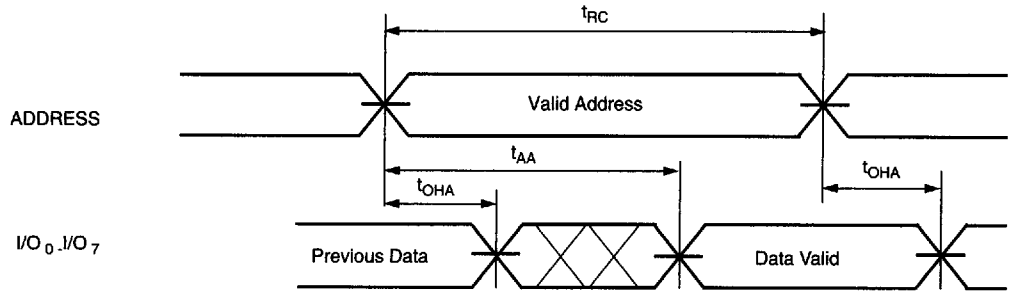
The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

I/O_0 - I/O_7: Common Input/Output Pins

GND: Ground

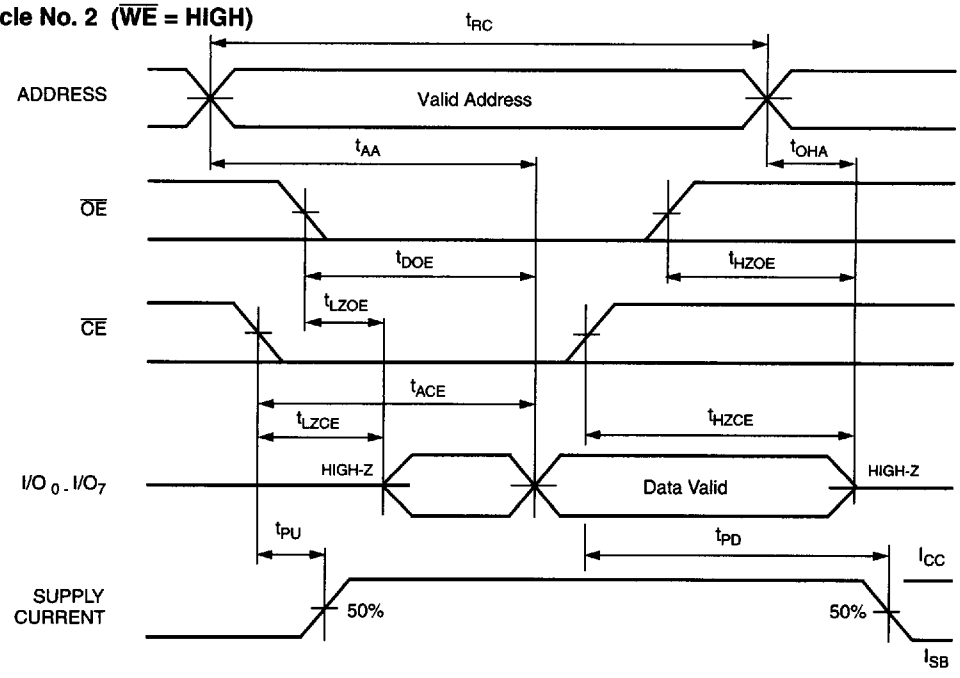
Switching Waveforms

Read Cycle No. 1 ($\overline{CE}$ = LOW, $\overline{OE}$ = LOW, $\overline{WE}$ = HIGH)



9A110-7

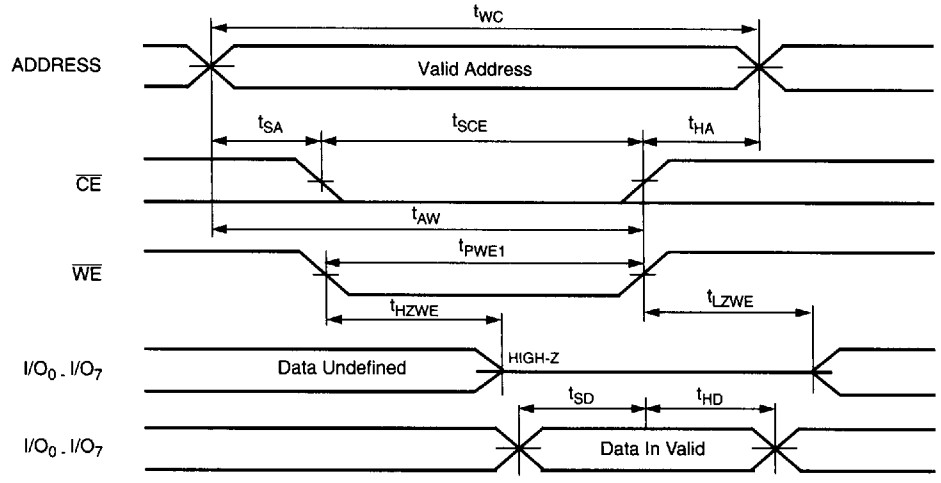
Read Cycle No. 2 ($\overline{WE}$ = HIGH)



9A110-8

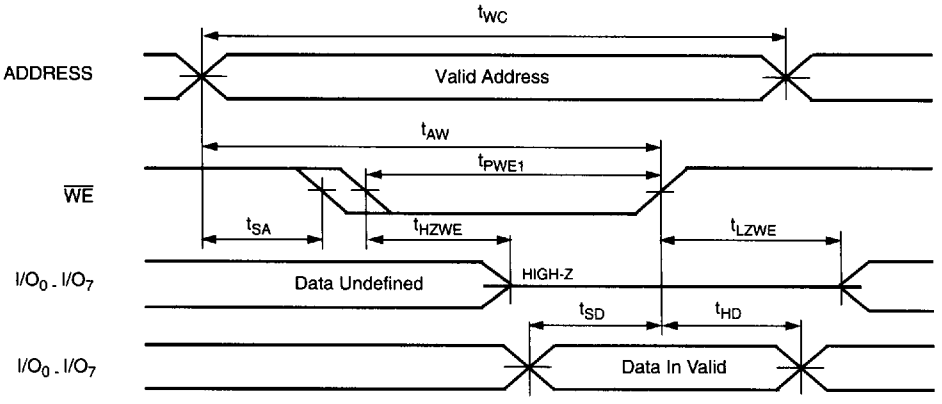
Switching Waveforms (continued)

Write Cycle No.1 ($\overline{CE}$ controlled, $\overline{OE}$ is HIGH or LOW: $\overline{CE}$ Terminates Write)



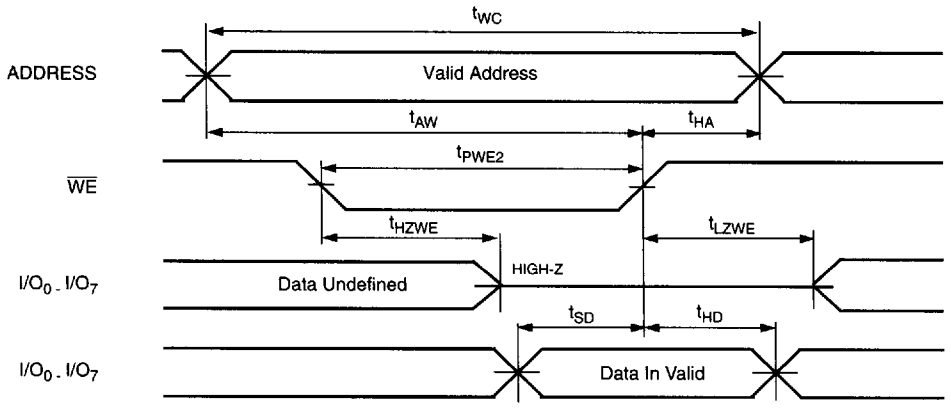
9A110-9

Write Cycle No.2 ($\overline{WE}$ controlled, $\overline{OE}$ is HIGH, $\overline{CE}$ is LOW: $\overline{WE}$ Terminates Write)



9A110-10

Write Cycle No.3 ($\overline{WE}$ controlled, $\overline{OE}$ is LOW, $\overline{CE}$ is LOW: $\overline{WE}$ Terminates Write)



9A110-11

Truth Table

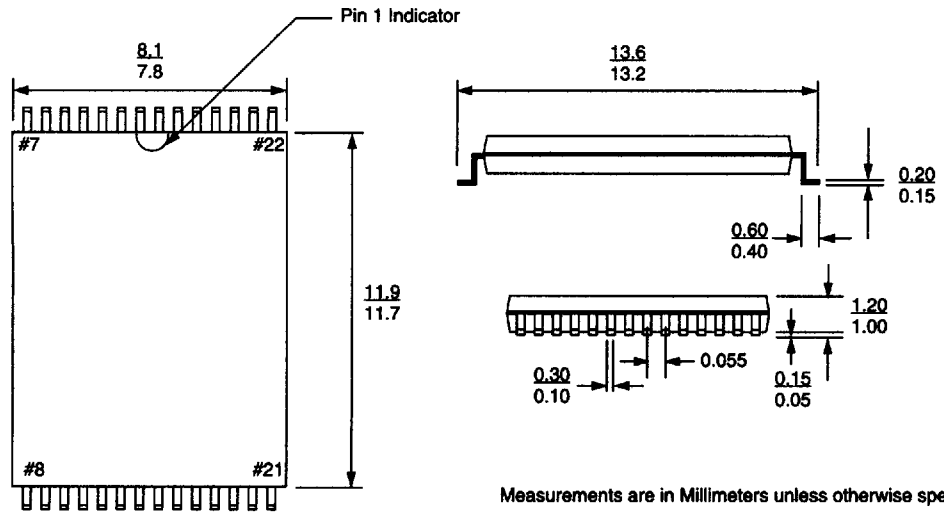
Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O	I_{CC}
Standby	X	H	X	High-Z	I_{SB1}, I_{SB2}
Selected/Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

Ordering Information

Speed	Part Number	Package Name	Package Type	Temperature Range
10	AP9A110-10VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	Commercial
12	AP9A110-12VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	
15	AP9A110-15VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	
20	AP9A110-20VC	V32.1	32-Pin (400-Mil) Small Outline J-Bend	

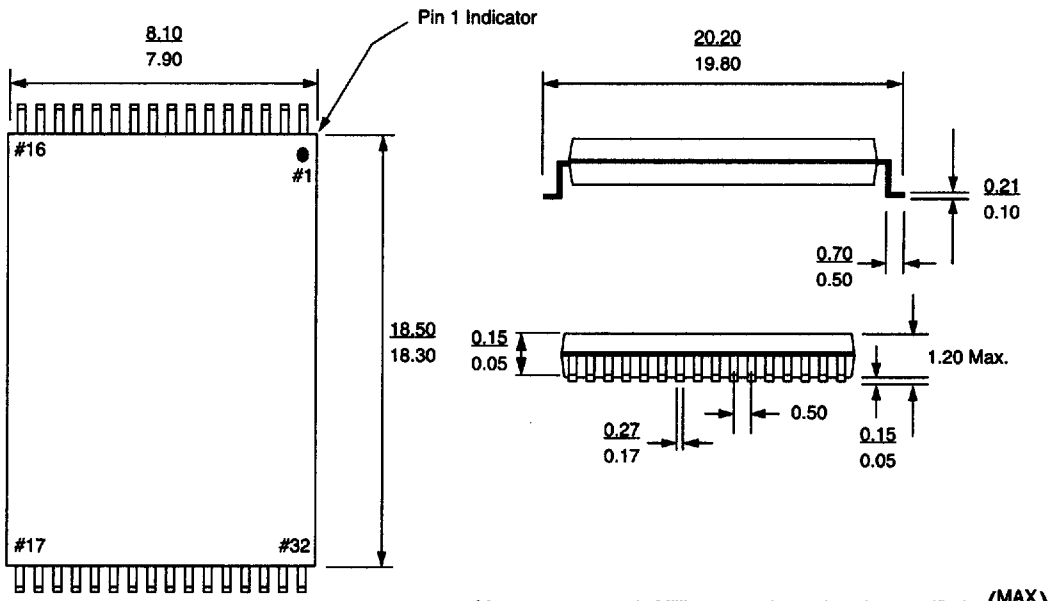
Document # DS-00015-Rev *

T28.1 - 28-Pin Thin Small Outline Package (TSOP)



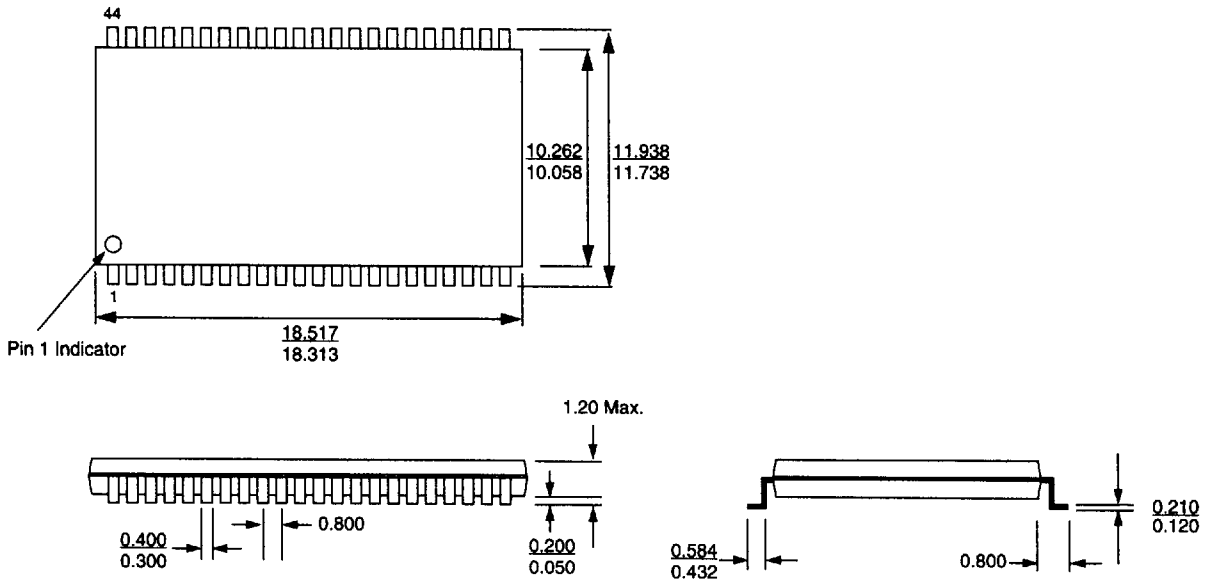
Measurements are in Millimeters unless otherwise specified. (MAX/MIN)

T32.1 - 32-Pin Thin Small Outline Package (TSOP)



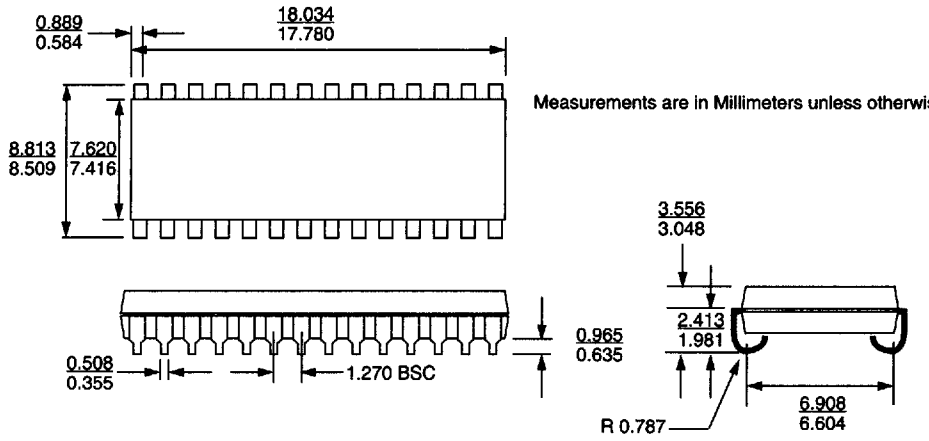
Measurements are in Millimeters unless otherwise specified. (MAX/MIN)

T44.1 - 44-Pin (400-Mil) Thin Small Outline Package (TSOP)



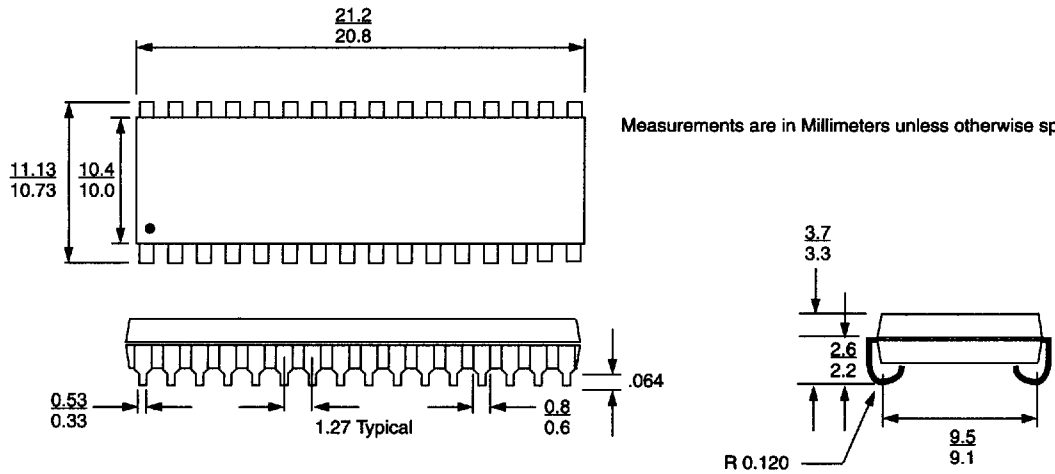
Measurements are in Millimeters unless otherwise specified. (MAX/MIN)

V28.1 - 28-Pin (300-Mil) Small Outline J-Bend (SOJ)



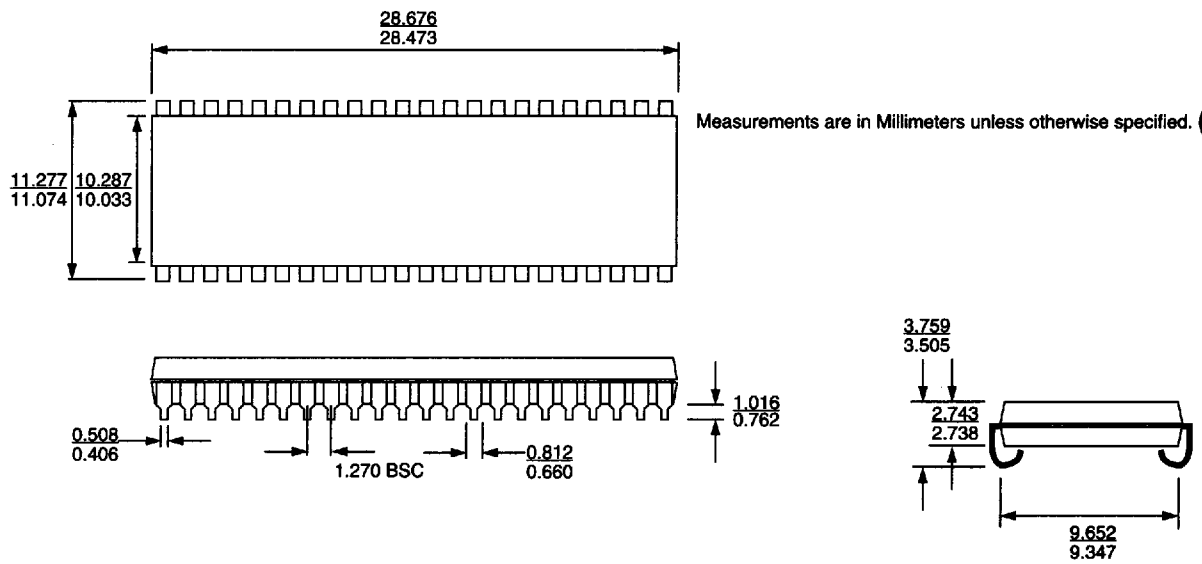
Measurements are in Millimeters unless otherwise specified. (MAX/MIN)

V32.1 - 32-Pin (400-Mil) Small Outline J-Bend (SOJ)



Measurements are in Millimeters unless otherwise specified. (MAX/MIN)

V44.1 - 44-Pin (400-Mil) Small Outline J-Bend (SOJ)



Measurements are in Millimeters unless otherwise specified. (MAX/MIN)