Data Sheet
March 1992

AT&T Microelectronics

ATT7C185

High-Speed CMOS SRAM 64 Kbits (8K x 8) Common I/O, Output Enable

Features

- High speed — 10 ns maximum access time
- Automatic powerdown during long cycles
- Advanced CMOS technology
- Chip-select powerdown, output enable
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT7164 and CY7C185/186
- Low-power operation
  — Active: 750 mW typical at 25 ns
  — Standby: 500 µW typical
- Package styles available:
  — 28-pin, plastic DIP
  — 28-pin, plastic SOJ

Description

The ATT7C185 device is a high-performance, low-power, CMOS static RAM organized as 8,192 words by 8 bits per word. The eight data-in and data-out signals share I/O pins. Parts are available in five speeds with worst-case access times from 10 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption for the ATT7C185 is 750 mW (typical) at 25 ns.

Dissipation drops to 75 mW (typical) when the memory is deselected (enable is high). Two standby modes are available. Automatic powerdown during long cycles reduces power consumption when the memory is deselected during read or write accesses that are longer than the minimum access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C185 device typically consumes only 30 µW at 3 V, thereby allowing effective battery backup operation.

Pin Information

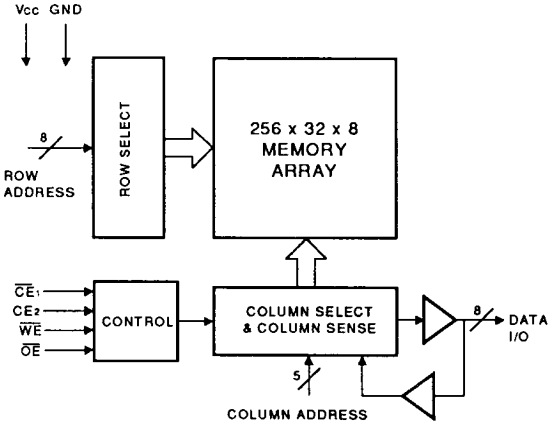


Figure 1. Block Diagram

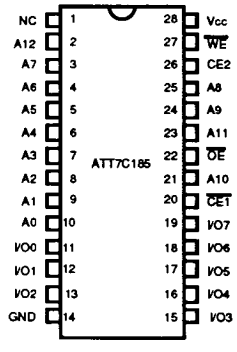


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Function
A0—A12	Address
I/O0—I/O7	Data Input/Output
$\overline{CE1}$ and CE2	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power
NC	No Connect

Functional Description

The ATT7C185 device provides asynchronous (unclocked) operation with matching access and cycle times. One active-low and one active-high chip enable and a 3-state I/O bus with a separate output enable simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A12. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE1}$ low and CE2 high while $\overline{WE}$ remains high. The data in the addressed memory location then appears on the data-out pin within one access time. When $\overline{CE1}$ is high or CE2 or $\overline{WE}$ is low, the output pin stays in a high-impedance state. Writing to an addressed location is accomplished when the $\overline{CE1}$ and $\overline{WE}$ inputs are both low and CE2 is high. Any of these signals can be used to terminate the write operation. Data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C185 device can withstand an injection of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	–55	125	°C
Supply Voltage with Respect to Ground	V_{CC}	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention	0 °C to 70 °C	$2.0\ V \le V_{CC} \le 5.5\ V$

Truth Table

Table 2. Truth Table for the ATT7C185

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Powerdown	Standby (I_{CC2} and I_{CC3})
X	L	X	X	High Z	Powerdown	Standby (I_{CC2} and I_{CC3})
L	H	H	L	Data Out	Read	Active
L	H	L	X	Data In	Write	Active
L	H	H	H	High Z	Output Disabled	Active*

*$I_{CC} \cong I_{CC1}$ at f_0 followed by powerdown after t_{ICHICL} has elapsed.

Electrical Characteristics

Over all Recommended Operating Conditions

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	V_{CC} + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ V_O ≤ V_{CC}, $\overline{CE1}$ = V_{CC}	–10	—	10	µA
Output Short Current	I_{OS}	V_O = Ground, V_{CC} = Max[2]	—	—	–350	mA
V_{CC} Current:						
Inactive[3]	I_{CC2}	—	—	15	30	mA
Standby[4]	I_{CC3}	—	—	100	500	µA
DR Mode	I_{CC4}	V_{CC} = 2.0 V[5]	—	10	250	µA
Capacitance:						
Input ($\overline{WE}$, $\overline{OE}$)	C_I	Ambient temp. = 25 °C, V_{CC} = 5.0 V	—	—	6	pF
Input ($\overline{CE1}$, CE2)	C_I	Ambient temp. = 25 °C, V_{CC} = 5.0 V	—	—	9	pF
Output	C_O	Test frequency = 1 MHz[6]	—	—	8	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously disabled, i.e., $\overline{CE1}$ ≥ V_{IH} or CE2 ≤ V_{IL}.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE1}$ = V_{CC}, CE2 = GND. Input levels are within 0.5 V of V_{CC} or ground.
5. Data retention operation requires that V_{CC} never drops below 2.0 V. $\overline{CE1}$ must be ≥ V_{CC} – 0.3 V. All other inputs meet V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V to ensure full powerdown.
6. This parameter is not 100% tested.

Table 4. Electrical Characteristics by Speed

Parameter	Symbol	Test Condition	Speed					Unit
			25 ns	20 ns	15 ns	12 ns	10 ns	
Max V_{CC} Current, Active	I_{CC1}	*	150	185	240	275	300	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE1}$ and $\overline{WE}$ ≤ V_{IL} and CE2 ≤ V_{IH}. Input pulse levels are 0 V to 3.0 V. Max I_{CC} shown applies over the active operating temperature range.

Timing Characteristics

Table 5. Read Cycle[1, 2, 3, 4]

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 9), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 8A).

Symbol	Parameter	Speed (ns)									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX, tCE2HCE2L, tCE1LCE1H	Read-cycle Time	25	—	20	—	15	—	12	—	10	—
tADXDOV	Address Change to Output Valid[5, 6]	—	25	—	20	—	15	—	12	—	10
tADXDOX	Address Change to Output Change	3	—	3	—	3	—	3	—	3	—
tCE2HDOV, tCE1LDOV	Chip Enable Active to Output Valid[5, 7]	—	25	—	20	—	15	—	12	—	10
tCE2HDOZ, tCE1LDOZ	Chip Enable Active to Output Low-Z[8, 9]	3	—	3	—	3	—	3	—	3	—
tCE2LDOZ, tCE1HDOZ	Chip Enable Inactive to Output High-Z[8, 9]	—	10	—	8	—	8	—	5	—	4
tOELDOV	Output Enable Low to Output Valid	—	12	—	10	—	8	—	6	—	5
tOELDOZ	Output Enable Low to Output Low-Z[8, 9]	0	—	0	—	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z[8, 9]	—	10	—	8	—	5	—	5	—	4
tADXICH, tCE2HICH, tCE1LICH	Chip Enable Active or Address Change to Powerup[10, 11]	0	—	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[10, 11]	—	25	—	20	—	20	—	20	—	18

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE1}$ or $\overline{WE}$ must be high and CE2 must be low during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. During this state, the chip is continuously selected ($\overline{CE1}$ low, CE2 high).
7. All address lines are valid prior to or coincident with the later of $\overline{CE1}$ or CE2 transition to active.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 8B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) rising edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle[1, 2, 3, 4] (See Figures 5, 6, and 7.)

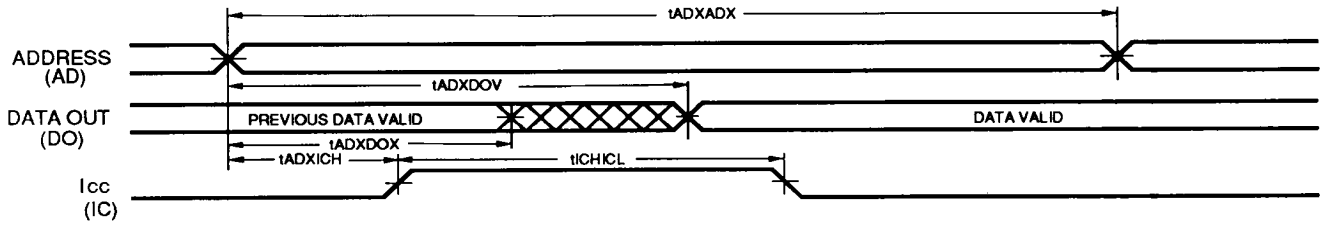
Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 9), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 8A).

Symbol	Parameter	Speed (ns)									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	Write-cycle Time	20	—	20	—	15	—	12	—	10	—
tCE2HCE2L, tCE1LCE1H	Chip Enable Active to End of Write	15	—	15	—	12	—	10	—	8	—
tADXWEL, tADXCE2H, tADXCE1L	Address Change to Beginning of Write	0	—	0	—	0	—	0	—	0	—
tADXWEH	Address Change to End of Write	15	—	15	—	12	—	10	—	8	—
tCE2LADX, tCE1HADX	End of Write to Address Change	0	—	0	—	0	—	0	—	0	—
tWELWEH	Write Enable Low to End of Write	15	—	15	—	12	—	10	—	8	—
tDIVWEH, tDIXWEH	Data Valid to End of Write	10	—	10	—	7	—	6	—	5	—
tWEHDIV, tWEHDIX	End of Write to Data Change	0	—	0	—	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[5, 6]	0	—	0	—	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z[5, 6]	—	7	—	7	—	5	—	4	—	4
tCE2HICH, tCE1LICH	Chip Enable Active to Powerup[7, 8]	0	—	0	—	0	—	0	—	0	—
tWELICH	Write Enable Low to Powerup [7, 8]	0	—	0	—	0	—	0	—	0	—
tCEHVCL	Chip Enable Inactive to Data Retention[7]	0	—	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[10, 11]	—	25	—	20	—	20	—	20	—	18

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t ADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE1}$ or $\overline{WE}$ must be high and CE2 must be low during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 8B. This parameter is sampled and not 100% tested.
7. This parameter is not 100% tested.
8. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) rising edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC2} to I_{CC1} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

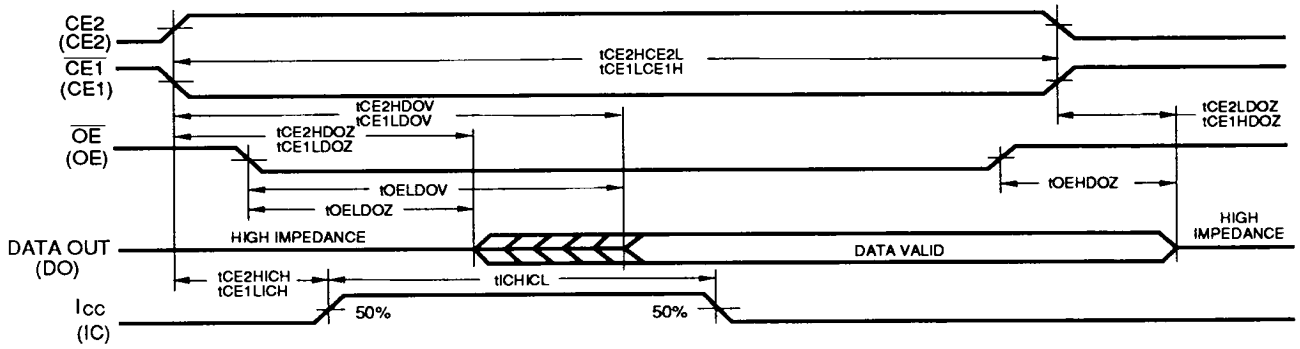
Timing Diagrams



Notes:
$\overline{WE}$ is high for the read cycle.

The chip is continuously selected ($\overline{CE1}$ low, CE2 high).

Figure 3. Read Cycle — Address-Controlled

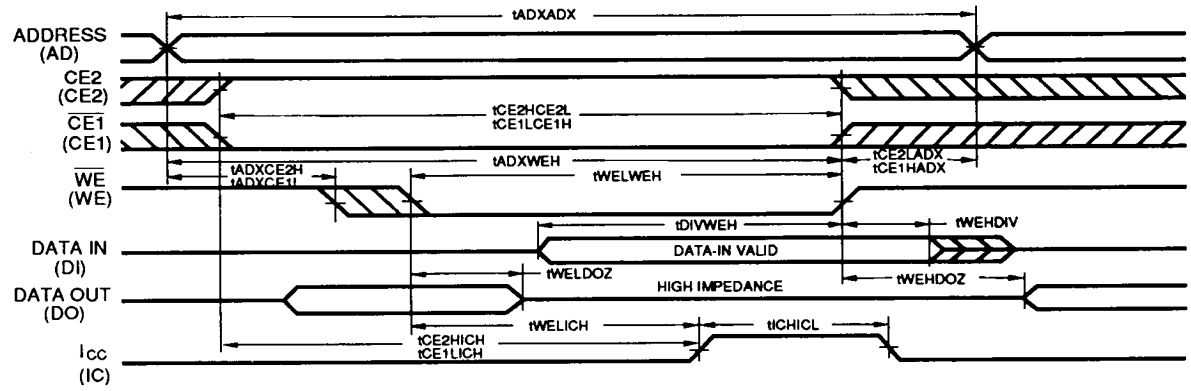


Notes:
$\overline{WE}$ is high for the read cycle.

All address lines are valid prior to or coincident with the later of $\overline{CE1}$ transition to low or the CE2 transition to high.

Figure 4. Read Cycle — $\overline{CE1}$ /CE2/ $\overline{OE}$ -Controlled

Timing Characteristics (continued)



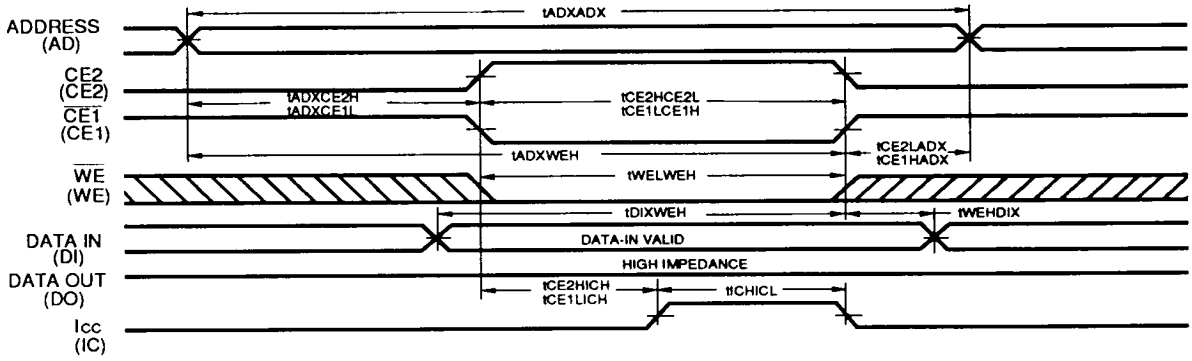
Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referred to the signal that goes inactive last or goes active first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE1}$ going low and CE2 going high, the output remains in a high-impedance state.

If $\overline{CE1}$ goes high or CE2 goes low before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) rising edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 5. Write Cycle — $\overline{WE}$ -Controlled



Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referred to the signal that goes inactive last or goes active first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE1}$ going low and CE2 going high, the output remains in a high-impedance state.

If $\overline{CE1}$ goes high or CE2 goes low before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) rising edge of CE2, (2) falling edge of $\overline{WE}$ ($\overline{CE1}$ and CE2 active), (3) transition on any address line ($\overline{CE1}$ and CE2 active), or (4) transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 6. Write Cycle — $\overline{CE}$ -Controlled

Timing Characteristics (continued)

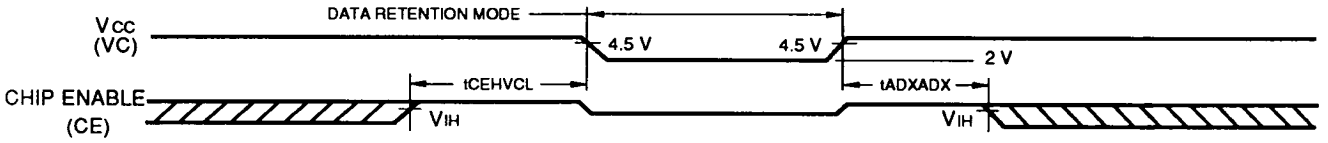


Figure 7. Data Retention

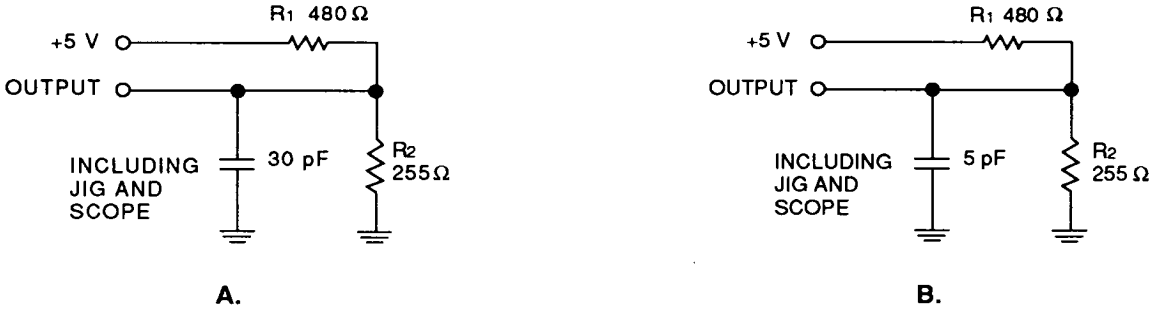


Figure 8. Test Loads

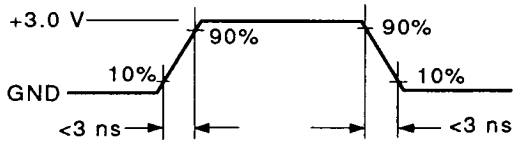
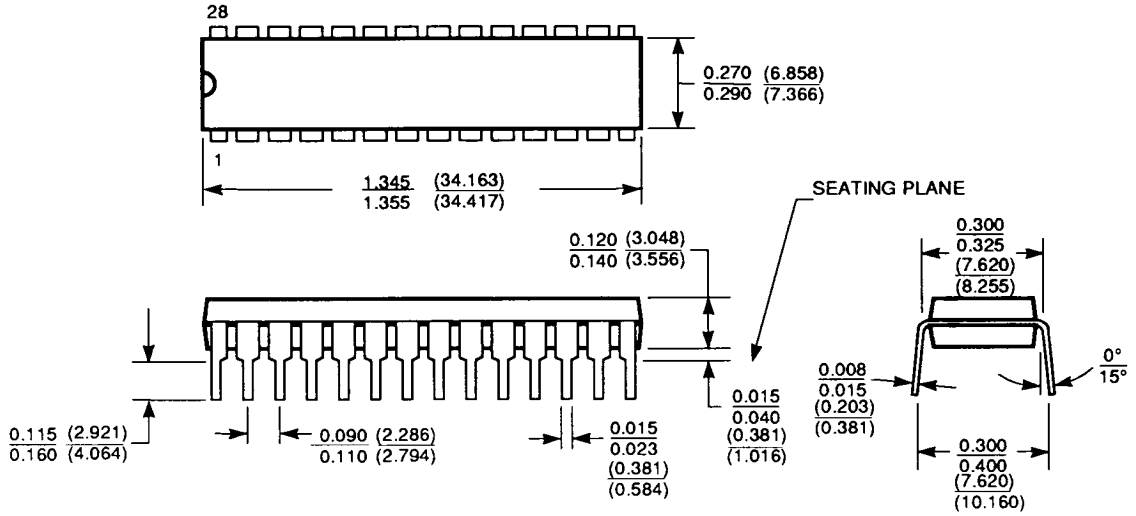


Figure 9. Transition Times

Outline Diagrams

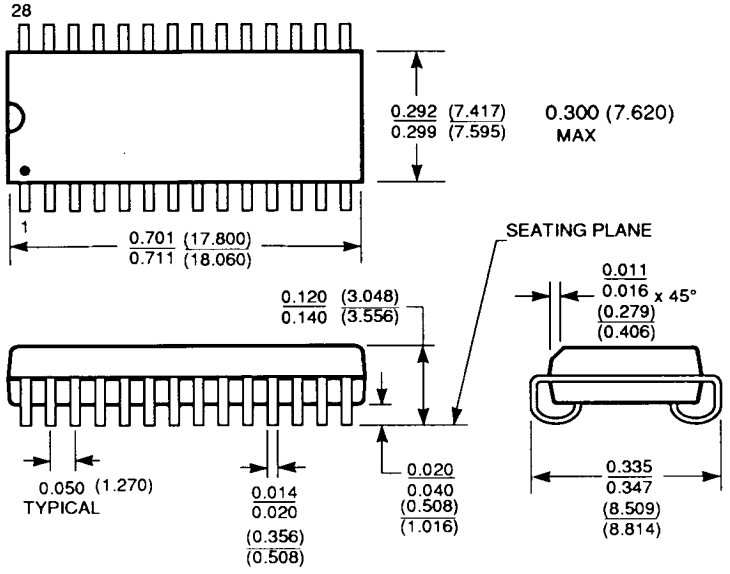
28-Pin, Plastic DIP

Dimensions are in inches and (millimeters).

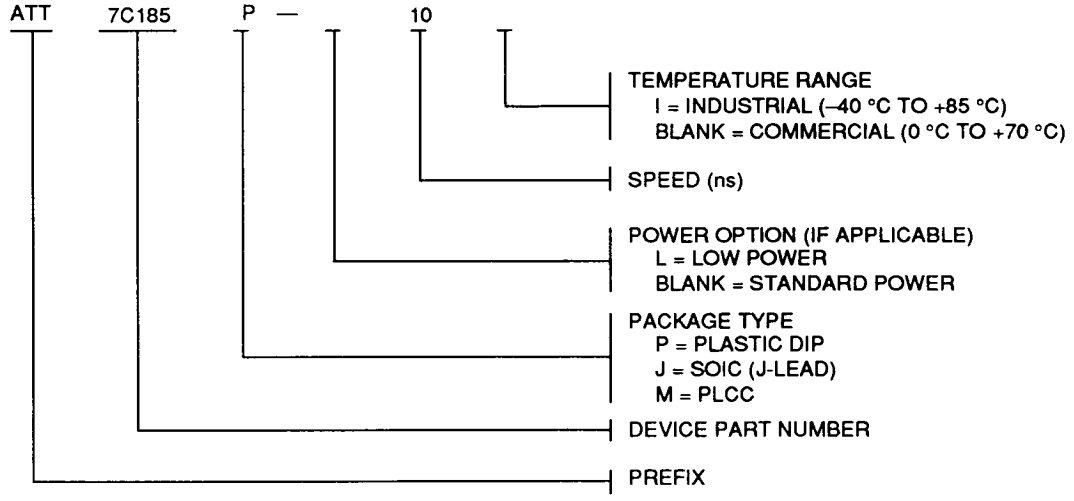


28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information



Operating Range 0 °C to 70 °C

Package Style	Performance Speed				
	25 ns	20 ns	15 ns	12 ns	10 ns
28-Pin, Plastic DIP	ATT7C185P–25	ATT7C185P–20	ATT7C185P–15	ATT7C185P–12	ATT7C185P–10
28-Pin, Plastic SOJ	ATT7C185J–25	ATT7C185J–20	ATT7C185J–15	ATT7C185J–12	ATT7C185J–10

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