SONY CXK5416P 35/35L/45/45L/55/55L

4096-word × 4 bit High Speed CMOS Static RAM

Description

The CXK5416P is a 16,384 bits high speed CMOS static RAM organized as 4,096 words by 4 bits and operates from a single 5V supply.

The CXK5416P is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: 35 ns/45 ns/55 ns (Max.)
- Low power standby: 5 μW (Typ.)—L-version
  100 μW (Typ.)—Standard version
- Low power operation: 200 mW (Typ.)
- Single +5V supply
- Fully static memory .... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)

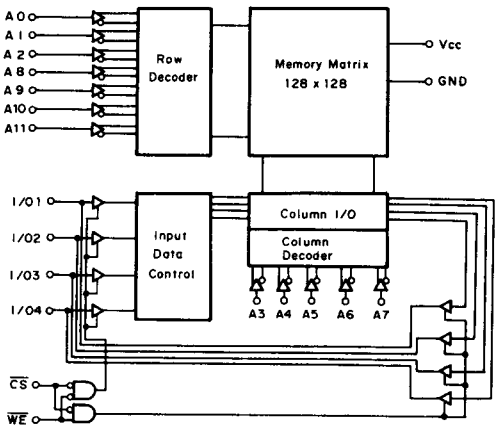
Structure

Silicon gate CMOS IC

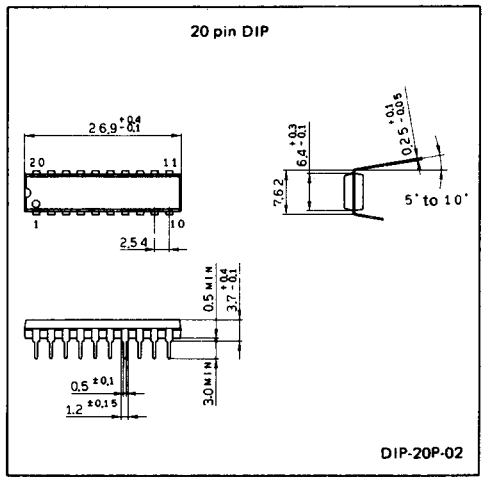
Function

4096-word × 4-bit static RAM

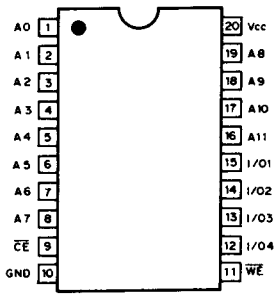
Block Diagram



Package Outline Unit: mm



Pin Configuration (Top View)



Symbol	Description
A0 to A11	Address Input
I/O 1 to I/O 4	Data Input Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	−0.5* to +7.0	V
Input Voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Input and Output Voltage	$V_{I/O}$	−0.5* to V_{CC}+0.5	V
Allowable Power Dissipation	P_D	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C
Soldering Temperature	Tsolder	260 • .10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ min=−3.5V for pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O 1 to I/O 4	V_{CC} Current
H	X	Not Selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	D_{OUT}	I_{CC1}, I_{CC2}
L	L	Write	D_{IN}	I_{CC1}, I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3**	—	0.8	V

* V_{CC}=5V, Ta=25°C

** V_{IL} min=−3.0V for pulse width less than 20 ns.

DC and Operating Characteristics

(V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test condition	CXK5416P -35/45/55			CXK5416P -35L/45L/55L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN}=GND to V_{CC} V_{CC}=5.5V	−2	—	2	−2	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CE}$=V_{IH} $V_{I/O}$=GND to V_{CC}	−2	—	2	−2	—	2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	40	70	—	40	70	mA
Average Operating Current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	60	100	—	60	100	mA
Standby Current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	0.02	1.0	—	0.001	0.05	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	10	20	—	10	20	mA
Output High Voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	—	—	0.4	V

Capacitance

(Ta=25°C, f=1 MHz)

Item		Test Condition	Symbol	Min.	Max.	Unit
Input Capacitance	A_0 to A_{11}, $\overline{WE}$	V_{IN}=0V	C_{IN}	—	5	pF
	$\overline{CE}$			—	7	
Input/Output Capacitance		$V_{I/O}$=0V	$C_{I/O}$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

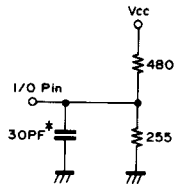
AC Operating Characteristics

• AC Test condition

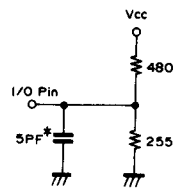
(V_{CC}=5V±10%, Ta=0 to +70°C)

Item	Condition
Input Pulse High Level	V_{IH}=3.0V
Input Pulse Low Level	V_{IL}=0V
Input Rise Time	t_R=5 ns
Input Fall Time	t_F=5 ns
Input and Output Timing Reference Level	1.5V
Output Load	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig
** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

Read Cycle

Item	Symbol	CXK5416P -35/35L		CXK5416P -45/45L		CXK5416P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns
Address Access Time	t_{AA}	—	35	—	45	—	55	ns
Chip Enable Access Time ($\overline{CE}$)	t_{CO}	—	35	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Enable to Output in Low Z ($\overline{CE}$)	t_{LZ}*	10	—	10	—	15	—	ns
Chip Disable to Output in High Z ($\overline{CE}$)	t_{HZ}*	0	20	0	20	0	20	ns
Chip Enable to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Disable to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

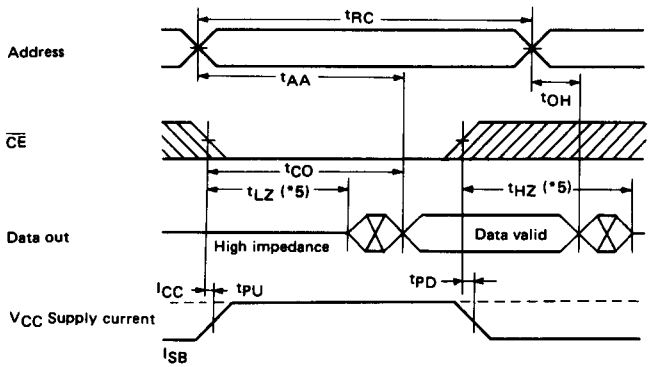
Write Cycle

Item	Symbol	CXK5416P -35/35L		CXK5416P -45/45L		CXK5416P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns
Address Valid to End of Write	t_{AW}	30	—	35	—	45	—	ns
Chip Enable to End of Write	t_{CW}	30	—	35	—	45	—	ns
Data to Write Time Overlap	t_{DW}	15	—	20	—	25	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	45	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}*	5	—	5	—	5	—	ns
Write to Output in High Z	t_{WHZ}*	0	15	0	15	0	20	ns

* Transition is measured ±500 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and not 100% tested.

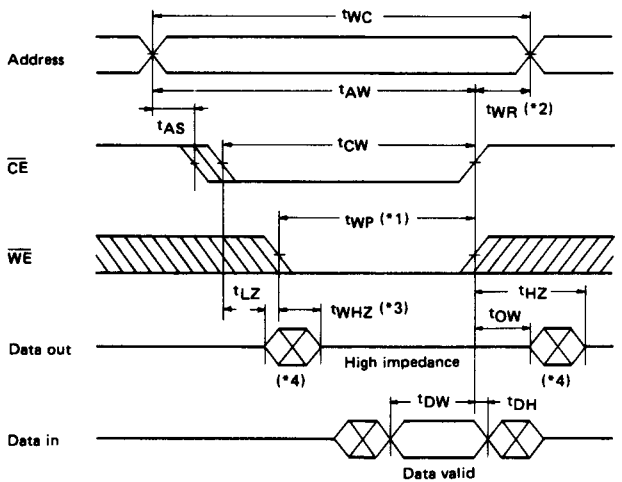
Timing Waveform

(1) Read Cycle [$\overline{WE}$=V_{IH}]

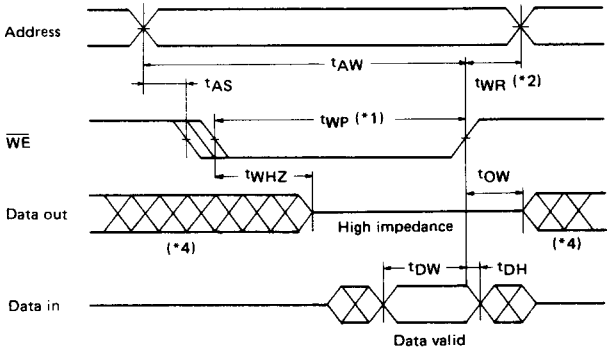


(2) Write Cycle

- Write Cycle No.1



• Write Cycle No.2: [$\overline{CE}$=V_{IL}]



*** Note)**

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. At any conditions, t_{HZ} is less than t_{LZ}.

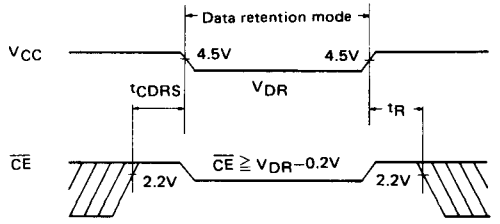
Data Retention Characteristics

(Ta=0 to +70°C)

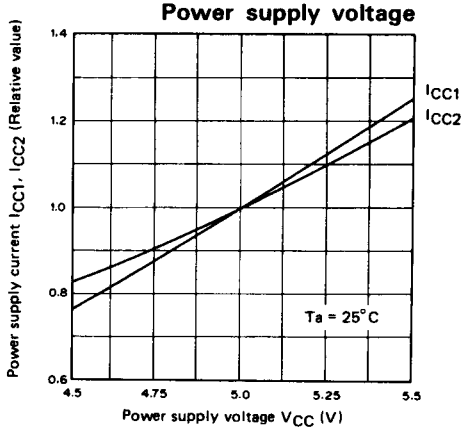
Item	Symbol	Test condition	CXK5416P -35/45/55			CXK5416P -35L/45L/55L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Retention Voltage	V_{DR}	$\overline{CE}\geqq V_{CC}-0.2V$	2.0	5.0	5.5	2.0	5.0	5.5	V
Data Retention Current	I_{CCDR1}	$\overline{CE}\geqq V_{CC}-0.2V$, V_{CC}=3.0V		12	600		0.6	30	μA
	I_{CCDR2}	$V_{IN}\leqq 0.2V$ or $V_{IN}\geqq V_{CC}-0.2V$, V_{CC}=2.0 to 5.5V		20	1000		1.0	50	μA
Data Retention Set up Time	t_{CDRS}	Chip disable to data retention mode	0			0			ns
Recovery Time	t_R		t_{RC}*			t_{RC}*			ns

*t_{RC}: Read Cycle Time

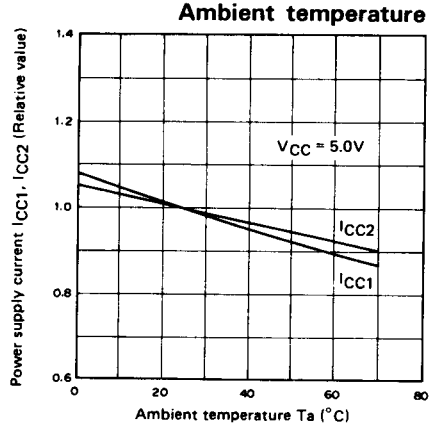
Data Retention Waveform



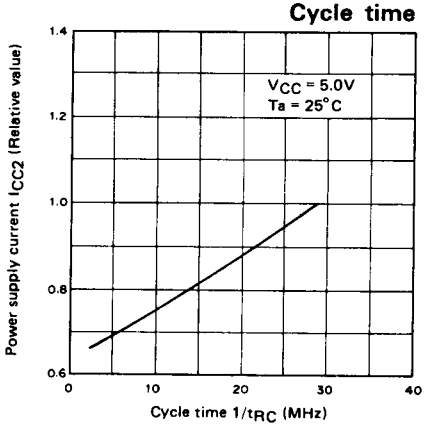
Power supply current vs. Power supply voltage



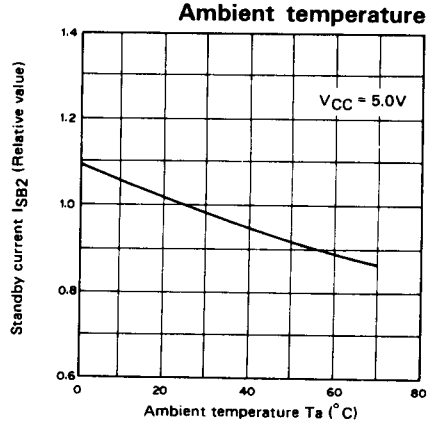
Power supply current vs. Ambient temperature



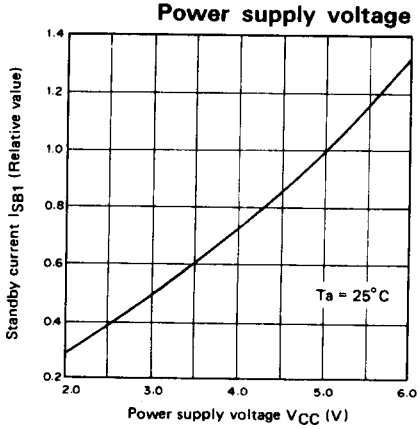
Power supply current vs. Cycle time



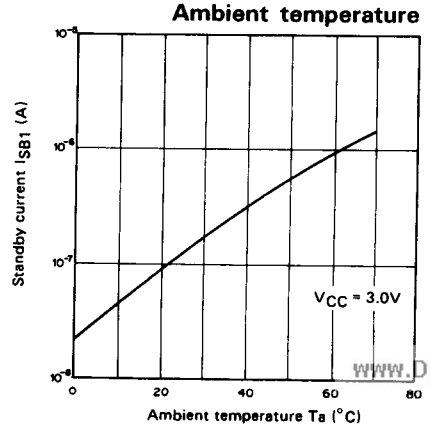
Standby current vs. Ambient temperature



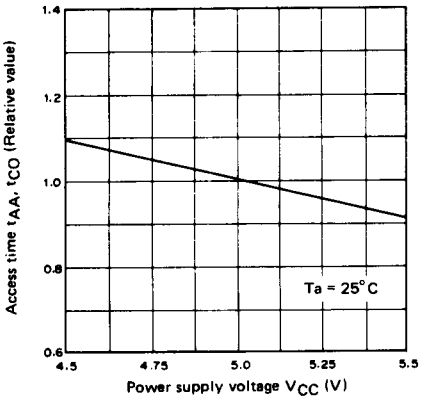
Standby current vs. Power supply voltage



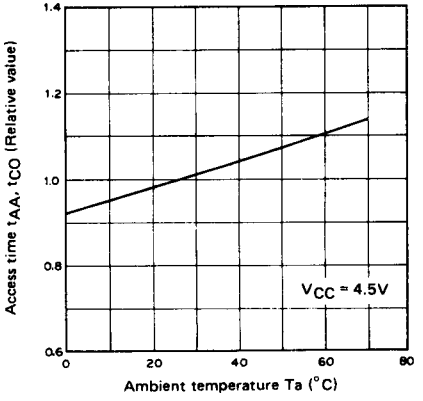
Standby current vs. Ambient temperature



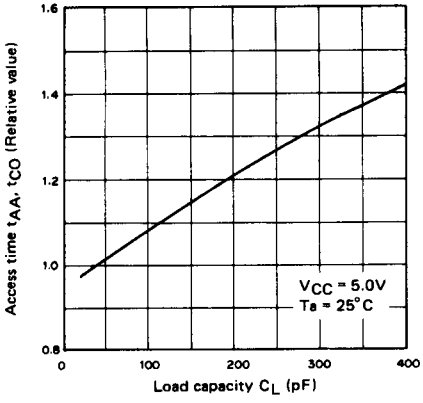
Access time vs. Power supply voltage



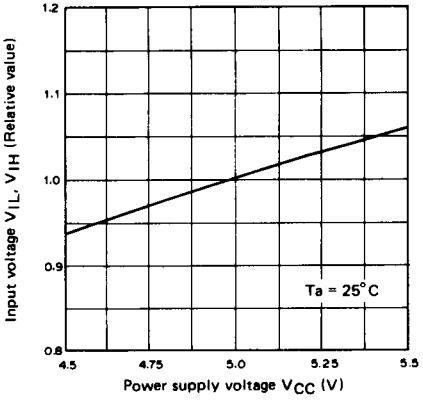
Access time vs. Ambient temperature



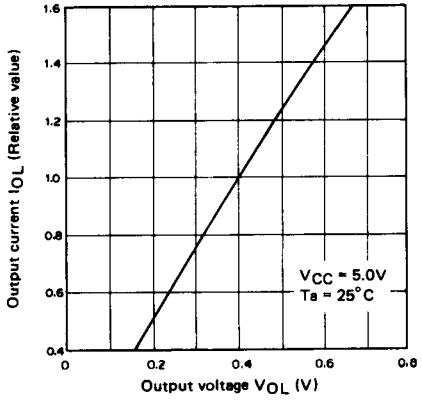
Access time vs. Load capacity



Input voltage vs. Power supply voltage



Output current vs. Output voltage



Output current vs. Output voltage