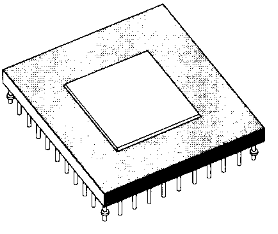
CASCADABLE SIGNAL PROCESSOR

- FULL 16 BIT, 32 STAGE, TRANSVERSAL FILTER
- FULLY CASCADABLE WITH NO SPEED DEGRADATION OR REDUCTION IN DYNAMIC RANGE
- COEFFICIENTS SELECTABLE AS 4, 8, 12, OR 16 BITS WIDE
- DATA THROUGHPUT TO 15.0 MHZ
- HIGH SPEED MICROPROCESSOR COMPATIBLE INTERFACE
- DATA INPUT AND OUTPUT THROUGH DEDICATED PORTS OR VIA THE MICROPROCESSOR INTERFACE
- FULLY STATIC HIGH SPEED CMOS IMPLEMENTATION
- SINGLE +5V ± 5% OR ± 10% POWER SUPPLY VARIANTS
- TTL AND CMOS COMPATIBILITY
- LESS THAN 2W POWER DISSIPATION
- STANDARD 84-PIN PGA



PGA84
(Grid Array Package)

APPLICATIONS

- Digital FIR filtering
- High speed adaptive filtering
- Correlation and Convolution
- Discrete Fourier Transform
- Speech processing using Linear Predictive Coding
- Image processing
- Waveform synthesis
- Adaptive and fixed equalizers and echo cancellers
- Spread spectrum communication
- Beamforming and beamscanning in sonar and radar
- Pulse compression
- High speed fixed point matrix multiplication

ORDERING INFORMATION

Part Number	Package	Clock Speed	Temperature
IMSA100-G21I	Ceramic Pin Grid Array	21MHz	-40°C, +85°C
IMSA100-G21S	Ceramic Pin Grid Array	21MHz	0°C, +70°C

A100-01.TBL

PIN CONNECTIONS

	1	2	3	4	5	6	7	8	9	10
A	GO	DIN [0]	DIN [2]	GND	DIN [5]	DIN [6]	DIN [9]	DIN [12]	DIN [13]	DOUT [1]
B	CIN [1]	GND	Vcc	DIN [1]	DIN [4]	DIN [8]	DIN [10]	DIN [14]	Vcc	DOUT [3]
C	CIN [2]	CIN [0]	Vcc	CLK	DIN [3]	DIN [7]	DIN [11]	DIN [15]	DOUT [0]	DOUT [5]
D	CIN [5]	CIN [4]	CIN [3]	Index				DOUT [2]	DOUT [4]	GND
E	CIN [7]	GND	CIN [6]			**IMSA100 84 pin grid array top view**		DOUT [6]	DOUT [7]	DOUT [8]
F	CIN [8]	CIN [9]	CIN [10]					DOUT [10]	DOUT [11]	DOUT [9]
G	CIN [11]	ADR [1]	ADR [3]					BUSY	Vcc	OUTRDY
H	ADR [0]	ADR [5]	$\overline{CE}$	Vcc	D[2]	D[6]	D[9]	D[13]	D[14]	$\overline{ERROR}$
J	ADR [2]	ADR [6]	$\overline{CS}$	GND	D[1]	D[5]	Vcc	D[11]	D[12]	D[15]
K	ADR [4]	$\overline{W}$	$\overline{RESET}$	D[0]	D[3]	D[4]	D[7]	GND	D[8]	D[10]

Note
All V_{CC} pins **must** be connected to the 5 Volt power supply.
All **GND** pins **must** be connected to ground.

A100-01.EPS

1. INTRODUCTION

The IMSA100 is a high speed, high accuracy 32 stage transversal filter. Its flexible architecture allows it to be used as a 'building block' in a wide range of Digital Signal Processing (DSP) applications. The part is capable of performing high speed DFTs, convolution and correlation, as well as many filtering functions.

The input data word length is 16 bits, and coefficients are programmable to be 4, 8, 12 or 16 bits wide; two's complement numerical formats are used for both data and coefficients. The coefficients can be updated asynchronously to the system clock during normal operation, allowing the chip to be used in a variety of adaptive systems. The IMSA100 can also be cascaded to construct longer transversal filters with no additional logic or degradation in speed, whilst preserving a high degree of accuracy. The device is controlled through a standard memory interface, allowing use with any general purpose microprocessor. Data communications can be either through the memory interface, or through dedicated data ports.

2. DESCRIPTION

The IMSA100 is a 32 stage, cascadable, digital transversal filter. The general canonical transversal filter is shown in Figure 1. An alternative, and functionally equivalent filter is shown in Figure 2. It is this second realisation that is used in the IMSA100, where the input signal is supplied in parallel to all 32 multipliers, and the delay and summation operations are performed in a distributed manner.

Each data sample loaded into the IMSA100 is fed in parallel to all 32 stages. At each stage the current input sample is multiplied by a coefficient stored in memory, and added to the output of the previous stage delayed by one clock cycle. The filter output at time t=kT is given by:

$$y(kT) = C(0) \times x(kT) + C(1) \times x((k-1)T) + \ldots$$
$$\ldots + C(N-1) \times ((k-N+1)T)$$

where $x(kT)$ represents the kth input data sample, and $C(0)$ to $C(N\text{-}1)$ are the coefficients for the N stages.

While the IMSA100 architecture is designed as a transversal filter it contains many features which allow it to be used in a wide range of signal processing applications, e.g. adaptive filtering, matrix multiplication, discrete Fourier transforms, correlation and convolution. Figure 3 shows the users view of the IMSA100.

The IMSA100 has four interfaces through which data can be transferred. The memory interface port allows access to the coefficent registers, the configuration and status registers and the data input and output registers for the multiplier accumulator array. Three dedicated ports are also provided, allowing high speed data input and output to the IMSA100 and the cascading of several devices.

Typically a microprocessor will configure the IMSA100 via the memory interface, then in a simple system data input and output can be performed through the data input (DIR) and data output (DOL, DOH) registers. Alternatively in a higher performance system data transfer may be performed via the dedicated input and output ports. A typical IMSA100 based system is shown in Figure 4. Simple high-throughput fixed-configuration systems can be implemented by clocking the configuration information into the IMSA100 from a ROM.

Figure 1 : Canonical Transversal Filter Architecture

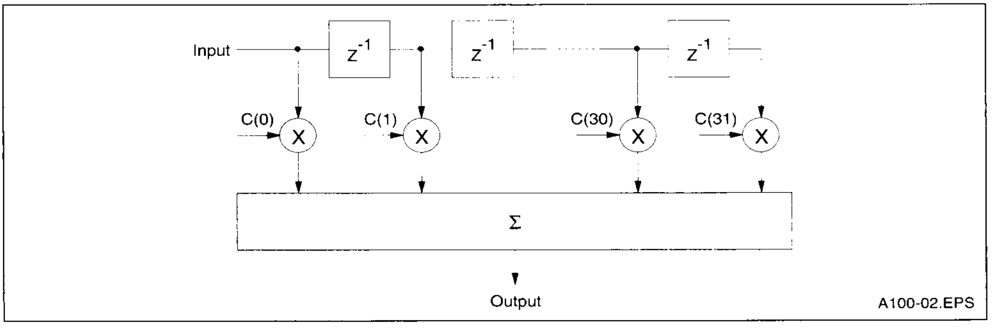


Figure 2 : Modified Transversal Filter Architecture

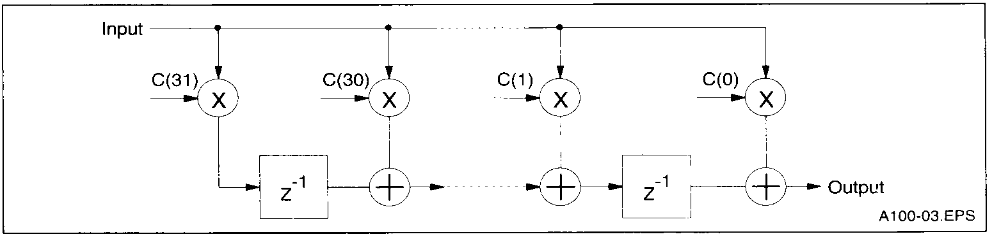


Figure 3 : IMSA100 User Model

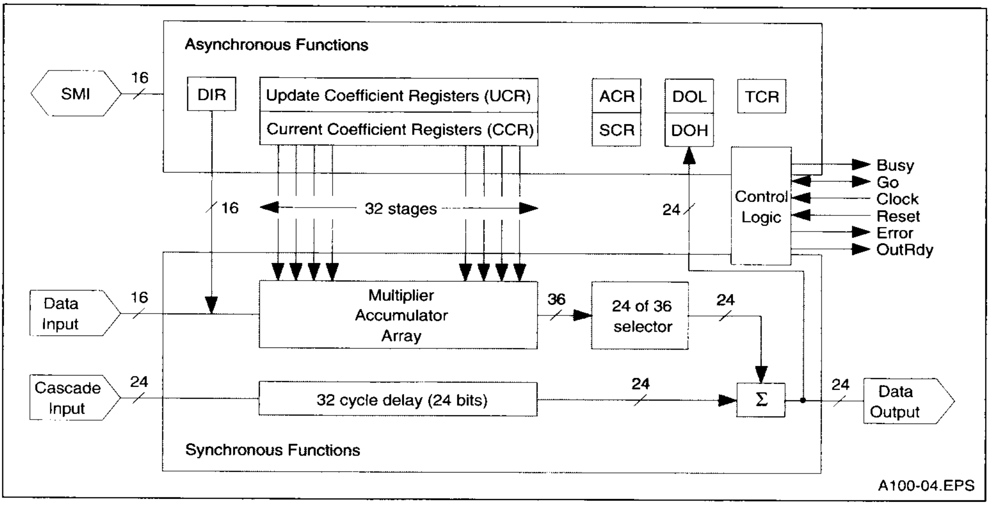
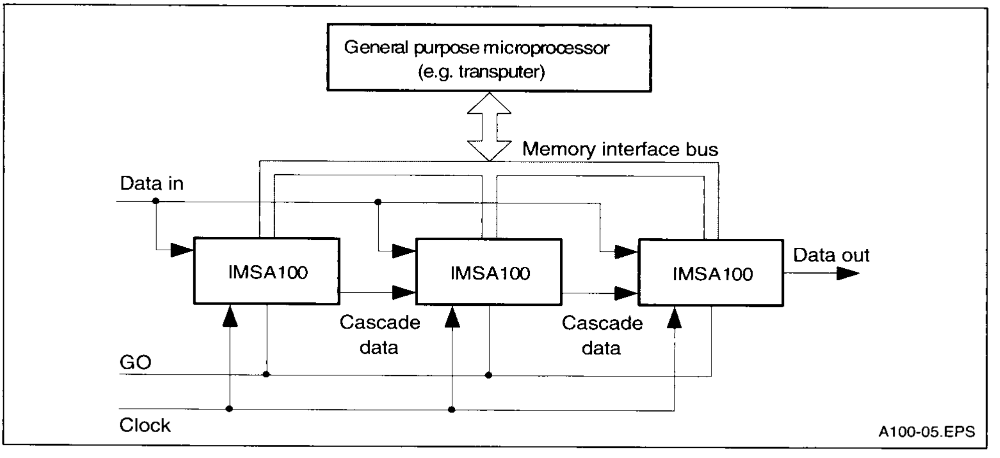


Figure 4 : Simple IMS100 Based System



The IMSA100 input data word width is 16 bits. The coefficient words can be programmed to be 4, 8, 12, or 16 bits wide. There is a trade off between the coefficient size and the speed of operation. If the coefficient word is L_C bits wide and the clock frequency applied to the IMSA100 is F then the maximum data throughput is $\frac{2 \times F}{L_C}$ So, for an IMSA100 operating from a 20.8MHz clock and using 4-bit coefficients the maximum data throughput is 10.4MHz, similarly for 16-bit coefficients the throughput is 2.6MHz.

To preserve complete numerical accuracy, no truncation or rounding is performed on the partial products in the multiplier accumulator array. The output of this array is calculated to full precision (36 bits). A programmable barrel shifter is located at the output of this array, which allows one of five 24 bit fields to be selected from the 36 bit result. The selected 24 bits are always correctly rounded and are sign extended before being output. The selection required can be determined from analysis of the coefficients and input data used in a given application.

Two banks of coefficients are provided. At any instant one set of coefficients is in use within the multiplier accumulator array, the other set being accessible via the memory interface. Once a new set of coefficients has been loaded, the two coefficient banks can be interchanged by performing a write operation to the 'Bank Swap' bit of a control register.

So that devices can be cascaded (eg. to construct longer transversal filters), a 32 stage, 24 bit wide, shift register and 24 bit adder is included on chip. The output of one chip is connected directly to the cascade input of the next. The output of the shift register is added internally to the output of the programmable barrel shifter to give the final 24 bit output from the chip. To minimise pin count and external buses, the data output and the cascade input ports transfer 24 bit words as a pair of 12 bit words across a 12 bit wide multiplexed interface.

As IMSA100s can be cascaded there is a price / performance trade off for most IMSA100 systems. For example, a correlation application could achieve high performance by using a cascade of IMSA100s sufficiently long to hold one of the waveforms being correlated in its coefficient registers and sending the other waveform involved in the correlation along the cascade of IMSA100s. A cheaper and slower solution would be to use a smaller number of IMSA100s and to decompose the single long correlation into a sequence of shorter correlations, the results of which are then summed.

3. PIN DESIGNATIONS

System services

Pin	In/out	Function
V_{CC}, GND		Power supply and return
CLK	in	Input clock
$\overline{\text{RESET}}$	in	System reset
$\overline{\text{ERROR}}$	out	Numerical overflow error
BUSY	out	Bank swap in progress

Synchronous input/output

Pin	In/out	Function
GO	in/out	Initiate input/computation/ output cycle
DIN[0-15]	in	Data input port
DOUT[0-11]	out	Data output port
CIN[0-11]	in	Cascade input port
OUTRDY	out	Output data ready

Asynchronous input/output

Pin	In/out	Function
D[0-15]	in/out	Memory interface data bus
ADR[0-6]	in	Memory interface address bus
$\overline{\text{CS}}$	in	Memory interface select
$\overline{\text{CE}}$	in	Memory interface enable
$\overline{\text{W}}$	in	Memory interface write enable

Notes

Signal names are shown with an $\overline{\text{overbar}}$ if they are active low, otherwise they are active high.

3.1 System services

System services include all the necessary logic to start up and maintain the IMSA100.

Power

Power is supplied to the device via the **V_{CC}** and **GND** pins. Several of each are provided to minimise inductance within the package. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100nF low inductance (e.g. ceramic) capacitor between **V_{CC}** and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

Input voltages must not exceed specification with respect to **V_{CC}** and **GND**, even during power-up and power-down ramping, otherwise *latchup* can occur. CMOS devices can be permanently damaged by excessive periods of latchup.

CLK

The clock input signal **CLK** controls the timing of input and output on the three dedicated ports and controls the progress of data through the multiplier accumulator array.

RESET

When the IMSA100 is reset the control logic within the IMS A100 will be reset and the ACR, SCR and TCR will be initialised to their default values.

Note that neither the internal data path registers nor the coefficient registers are affected by the reset. Resetting the device initialises the SCR to its default setting.

So, depending on the setting of SCR before a reset, a reset may also be a device reconfiguration. The sequence of operations required to return the device to a defined state following reconfiguration is described under SCR in the register description.

A reset is initiated automatically when power is first applied to the device.

This reset will be completed once four cycles of **CLK** have occured after **Vcc** is valid. Alternatively reset can be initiated by taking RESET low. This reset will be completed after at least two cycles of **CLK** have occured while RESET is held low. RESET should be held low for at least 200ns. Normal device operation can then continue after RESET is taken high.

The reset should be completed before either the synchronous or asynchronous parts of the device are used.

ERROR

If asserted, this pin indicates an error condition has occured, and that the condition has not been cleared. The error condition results from a numerical overflow in either the final adder or in the field selector. To allow this signal to be wire ORed between all the devices in a cascade and hence to be used as an interrupt signal to the host processor, the ERROR outputs are open collector.

If suitably armed before the error occured the ACR error bits can be read to discriminate the two error sources. The error bits in the ACR and the error condition can be cleared and then the error bits armed to detect further errors by writing values to the ACR. The sequence of values that should be written to the ACR error bits is 0 followed by 1. An error condition can only be cleared if the error bits were suitably armed before the most recent error occured.

The ACR error bits may not observe an error occuring between clearing and arming the error bits. So, when clearing an error and arming the error bits precautions should be taken to ensure that no new error occurs. For example, first prevent the IMSA100 from initiating computation on new data; second wait for any results pending to be output; then clear and rearm. The ACR error bits will observe any error occuring after they are armed. Thus, if an error occured before the ACR error bits were armed it may be necessary to arm the error and then force an error before proceeding to clear the error (as described above).

Following power up the contents of the multiplier accumulator array and cascade path are indeterminate. As this indeterminate data flushes through a system of one or more IMSA100s errors are likely to occur. Similarly, altering the device configuration defined by the SCR is likely to result in errors. The sequence of operations required to return the device to a defined state following reconfiguration is described under SCR in the register description section of this specification.

BUSY

When high this pin indicates that an exchange of data between the Current and Update Coefficient Registers is in progress. Under certain conditions the duration of **BUSY** may be vanishingly small. **BUSY** will be active if the bank swap is caused by setting ACR[0] to request a single bank swap or when SCR[2] is set selecting Continuous Swap mode. The detailed behaviour is described in the bankswap timing diagrams.

3.2 Synchronous input/output

GO

The **GO** signal initiates a cycle of data input, computation and output. An IMSA100 configured as a slave will monitor the **GO** signal on the rising edge of **CLK** one cycle before it is ready to accept more data and on every rising edge thereafter until **GO** is found to be high.If **GO** is high then data input will occur on the next rising edge of **CLK**. If **GO** is low when it is sampled no new data input will occur.

In a cascade of IMSA100s one IMSA100 may be configured as a master. The master IMSA100 will drive its **GO** pin high after data has been written into its Data Input Register indicating that new data is available and that the slave IMSA100s in the casacade should start an input, computation, output cycle. When the **GO** signal goes low new data can be written to the IMSA100s. Typically a host processor will write simultaneously to the Data Input Registers of all the IMSA100s in the cascade. The host will then monitor the **GO** signal before writing new data to the cascade.

DIN[0-15]

This 16 bit wide data input port allows high speed data input to the IMSA100. The timing of this input is controlled by the **CLK** and **GO** signals. In a cascade of IMSA100s the 16 bit wide input data path and the **CLK** and **GO** signals will be bussed to all devices.

DOUT[0-11]

This 12 bit data port outputs the result from the IMSA100. The 24 bit result is multiplexed through this port as two 12 bit words, the least significant word being output first. The most significant word is output second and remains on the data pins until a new data output sequence is about to start. The **OUTRDY** signal can be used to latch these words into external circuitry. In a cascade of IMSA100s the **DOUT** pins of one device connect to the **CIN** pins of the next device in the cascade.

CIN[0-11]

The Cascade Input allows multiple IMSA100s to be cascaded. A 24 bit word is input as two 12 bit words the least significant word being input first. The 24 bit word is delayed by a shift register and summed with the output of the multiplier accumulator array. The delay from a word being input on the cascade input to that word affecting the data output is 32 data input cycles. In a typical IMSA100 based system the cascade input of each device will be connected to the data output **DOUT[0-11]** of the previous IMS A100 in the cascade. The Cascade Input of the first device in the cascade will normally be connected to ground.

OUTRDY

The output ready signal **OUTRDY** goes low just after the least significant data output word is available on the **DOUT** pins and goes high just after the most significant word is available. The rising edge of **OUTRDY** also indicates that the Data Output registers (DOL, DOH) contain the new result word. Thus the **OUTRDY** signal can either be used to latch the output of the IMSA100 into external logic or to indicate that output of the IMSA100 can be read through the memory interface from the Data Output registers.

3.3 Asynchronous input/output

$\overline{CS}$

This pin selects the chip; if chip select $\overline{CS}$ is low an access to the memory interface will be enabled. This signal is usually asserted by the host processor's address decoder at the beginning of a memory cycle.

$\overline{CE}$

The chip enable pin. The memory interface on the IMSA100 appears to the system controlling it as 128 words of static RAM. The chip enable $\overline{CE}$ signal is similar in operation to the chip enable signal found on static RAMs. When $\overline{CE}$ is high the chip select, write enable and the address inputs are ignored and the memory interface data bus is tri-state. When chip enable is low a single read or write access is made to one of the registers within the IMSA100. Accesses to the memory interface can occur completely asynchronously to operations on the data in, cascade in and data output ports **DIN[0-15]**, **CIN[0-11]** and **DOUT[0-11]**.

$\overline{W}$

The write enable pin indicates whether the access to the IMS A100 memory interface is to be a write or a read. If $\overline{W}$ is low a write access is indicated.

ADR[0-6]

The seven bit address bus comprises pin **ADR[0-6]**. The seven bit binary value applied to the address inputs of the IMSA100 indicates which register is to be accessed.

D[0-15]

During a write to the memory interface a 16 bit word is applied to data bus pins **D[0-15]**. This word will be latched on the rising edge of chip enable $\overline{CE}$ at the end of the cycle. During a read cycle the contents of the location accessed are placed on the data pins. When $\overline{CE}$ is high the data signals are tri-state.

4. REGISTER DESCRIPTION

The memory map shown below indicates the primary addresses for each register. All locations between decimal addresses 64 and 75 inclusive are uniquely decoded. This group of registers is shadowed at other locations up to the 128 word boundary. The effect of reading and writing to areas in the memory map other than those shown in the table is undefined.

If the user wishes to initialise the device from a ROM addressed by a clocked counter, one of the following options applies:

1 Restrict the counter to count only from 0 to 68; this avoids writing to the data registers as well as the shadow locations.

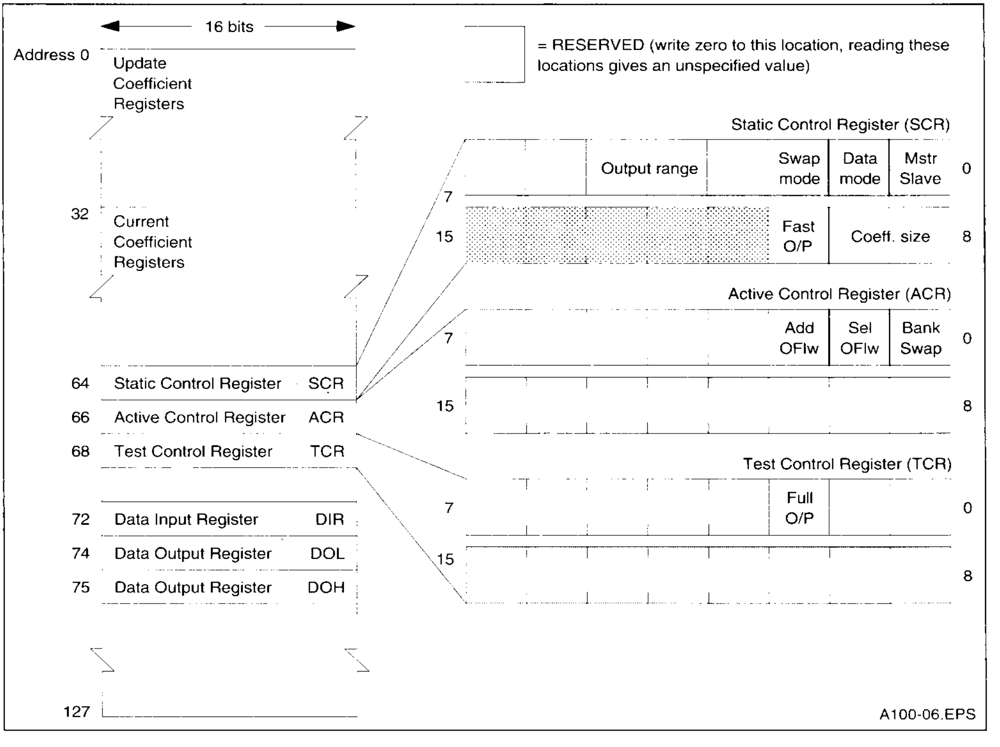
2 Count down from 127 to zero. The initialization at the lower addresses will override spurious ones at the higher shadowed addresses.

4.1 Memory Map*

Register	Address decimal	Address hex	Function
CCR[0-31]	32-63	20-3F	Current Coefficient Registers
UCR[0-31]	0-31	00-1F	Update Coefficient Registers
SCR	64 65	40 41	Static Control Register Unused location
ACR	66 67	42 43	Active Control Register Unused location
TCR	68	44	Test Control Register
DIR	72	48	Data Input Register
DOL	74	4A	Data Output Register (Least Significant Word)
DOH	75	4B	Data Output Register (Most Significant Word)

* All other locations accessible via the memory interface of the IMSA100 are reserved.

Figure 5 : IMSA100 Memory Map



4.2 Registers

CCR[0–31]

The Current Coefficient Registers contain the coefficients currently being used by the multiplier accumlator array. CCR[0] (decimal address 32) corresponds to the coefficient register of the multiplier accumlator nearest the output of the IMSA100; i.e. this location is equivalent to C(0) in Figure 2.

Similarly CCR[31] (decimal address 63) corresponds to C(31). The Current Coefficient Registers can be read from at any time and can be written to provided that no data processing is taking place. The effect of writing to the Current Coefficient Registers while data is being processed is undefined.

UCR[0–31]

The Update Coefficient Registers are equivalent to the Current Coefficient Registers, with the exception that the values in the Update Coefficient Registers are not currently in use within the multiplier accumlator array and can therefore be written to at any time.

A bank swap operation is equivalent to an exchange of data between the Update Coefficient Registers and the Current Coefficient Registers.

SCR

The Static Control Register contains the control bits which configure the IMSA100 and are unlikely to need updating after their initial configuration. The contents of the Static Control Register are not affected by the IMSA100 and can be read at any time.

Reconfiguring the SCR may result in indeterminate data values within the IMSA100 system. These values may in turn result in errors. After reconfiguring the SCR the following sequence should be followed to return the IMSA100 system to a defined, error free condition:

1. Arm error bits in ACR.
2. After SCR has been reconfigured **GO** should be held low for 20 cycles of **CLK**.
3. A series of suitable data values should then be flushed through the IMSA100 system.
4. Any errors generated should then be cleared.
5. The IMSA100 system is then ready to commence normal operation.

ACR

The Active Control Register contains status and control bits which are likely to be accessed during normal operation of the IMS A100; i.e. when handling error conditions and when requesting single coefficient bank swaps.

TCR

The Test Control Register is used for test purposes. One of the test modes provides access to the least significant part of the multiplier accumulator array output.

DIR

The Data Input Register. The IMSA100 can be configured to either take its input data from the **DIN** pins or from the Data Input Register. If the IMSA100 is configured as the master of a cascade of IMSA100s the **GO** signal will be driven in response to writing data into the Data Input Register.

In a small IMSA100 based system the Data Input Registers of all the devices in the cascade will normally be mapped into the same location within the address space of the processor controlling the cascade. Thus a single write operation can write data to all devices, the master IMSA100 generating the **GO** signal for the slaves. The Data Input Register is write only.

DOL

The least significant word of the Data Output Register. The output data from the IMSA100 is available from both the **DOUT[0–11]** pins and from the Data Output Registers. The value held in the Data Output Registers is the 24 bit output word, sign extended to 32 bits. DOL contains the least significant 16 bits of the 24 bit result; the register is read only.

DOH

The most significant word of the Data Output Register. The DOH register contains the most significant 8 bits of the 24 bit output word generated by the IMSA100. The most significant 8 bits of DOH are the sign extension of the output word. DOH is read only.

The remainder of this section describes the register details bit by bit. Each section commences with the name of the register with the bit number(s) followed by the default value, in the general format:

• **Name**

REGISTER[MSB–LSB]	Default: MSB LSB

The least significant bit of a register is bit 0.
* in the tables indicates the default state of the register bit(s).

4.3 Static control register

• **Fast Output**

SCR[10]	Default: 0

The Fast Output bit controls the way in which the 24 bit output of the IMSA100 is multiplexed across the 12 bit wide **DOUT** port. The interval between data output cycles is the same for both Normal and Fast output modes.
The difference between the modes is the time division between the least and most significant words. In fast output mode the least significant 12 bit word is available for the minimum period possible, thus allowing the most significant word to be output at the earliest possible instant. In normal output mode the least significant word is available for the same length of time as the most significant word (unless the duration of the most significant word is extended by idle cycles).
The timing constraints on data output in Normal mode are significantly simpler than those in Fast mode. Fast mode should be considered a special mode which is only used where the early availability of the output words is important, e.g. an adaptive system where the filter coefficients are being modified in response to the output data.
All devices in a cascade of IMSA100s should be configured for the same output mode. The Fast Output bit should not be altered during data processing. If it is altered the data output of the cascade will be undefined until new input data has flushed through all stages of the cascade. If the coefficient size is 4 bits there is no difference between the fast and normal modes.

SCR[10]	Output mode
0	Normal*
1	Fast

• **Coefficient Size**

SCR[9–8]	Default: 1 1

Defines size of coefficient used, in terms of word width. This also determines the minimum interval between data input cycles and thus the data throughput of the IMSA100. The Coefficient Size bits should not be altered during data processing. If they are altered the data output of the cascade will be undefined until new input data has flushed through all stages of the cascade.
In each mode the coefficient data is the least signifcant bits of the 16 bit word; e.g. in 4 bit mode, a two's complement number should be programmed into bits 0–3 of the 16 bit register. The remaining bits 4–15 are ignored.

SCR[9–8]	Coefficient size	Data input interval
0 0	4 bits	2 cycles
0 1	8 bits	4 cycles
1 0	12 bits	6 cycles
1 1	16 bits	8 cycles *

• **Reserved**

SCR[7–6]	Default : 0 0

These locations are reserved. The user should write 0,0 to these locations to maintain compatability with future products. The value read from this location is undefined.

• **Reserved**

SCR[3]	Default: 0

This location is reserved. The user should write 0 to this location to maintain compatability with future products. The value read from this location is undefined.

• **Output Word Selection**

SCR[5–4]	Default: 1 0

These bits determine the 24 bit wide field selected from the 36 bit wide output of the multiplier accumulator array (bit positions numbered 0 to 35).
The word selected will be rounded and sign extended before being output. Note that ranges '10' and '11' imply sign extension of the result.
The Output Word Selection bits should not be altered during data processing. If they are altered the data output of the cascade will be undefined until new input data has flushed through all stages of the cascade.

SCR[5–4]	Field
0 0	[7–30]
0 1	[11–34]
1 0	[15–38] *
1 1	[20–43]

- **Continuous Swap**

SCR[2]	Default: 0

The Continuous Swap bit selects whether the two banks of coefficient registers are automatically exchanged after each data input and computation cycle or if individual bank swaps occur under the direction of the Bank Swap bit in the Active Control Register, ACR[0]. SCR[2] should not be set if a bankswap has been requested (by setting ACR[0]) and is still pending.

SCR[2]	Swap Mode
0	Swap on asserting ACR[0] *
1	Swap after end of each input cycle

- **Input Data Source**

SCR[1]	Default: 0

The data source for the multiplier accumulator array can come from one of two sources, selected by SCR[1]. Data can either be input from the **DIN** port or it can be written into the Data Input Register via the memory interface. See also the following section.

SCR[1]	Data Source
0	From **DIN** port *
1	From DIR

- **Master not Slave**

SCR[0]	Default: 0

The Master not Slave bit selects whether the IMSA100 samples the **GO** input to determine the start of a data input cycle (slave mode), or drives the **GO** pin when data is written to the DIR (master mode). If input data is supplied through the DIR one IMSA100 in the cascade should be configured as a master. If data is supplied to the **DIN** port by an external data source all the IMSA100s in the cascade should be configured as slaves and **GO** should be driven by an external system. Note that an illegal mode results if SCR[1] is 0 and SCR[0] is 1; i.e. a master cannot obtain data from the **DIN** port.

SCR[0]	Mode
0	Slave *
1	Master

4.4 Active control register

- **Cascade Adder Overflow**

ACR[2]	Default: 0

If previously armed this status bit will be set if the addition of the 24 bit words output by the 24 from 36 bit selector (on the output of the multiply accumulator array) and the cascade shift register causes an arithmetic overflow.

The **ERROR** pin will be driven low while this or any other error condition is active. This error bit and the error condition can be cleared by writing a zero to ACR[2], provided the data in the adder is no longer in error. After clearing this error bit the error bit should be armed (by writing a one to ACR[2]) to ensure that any future error is detected. See **ERROR** section.

- **Selector Overflow**

ACR[1]	Default : 0

If previously armed this status bit will be set if the 24 bit output range of the selector does not include all the significant binary digits in the 36 bit result generated by the multiply accumulator array. The **ERROR** pin will be driven low while this or any other error condition is active. This error bit and the error condition can be cleared by writing a zero to ACR[1]. After clearing this error bit the error bit should be armed (by writing a one to ACR[1]) to ensure that any future error is detected. See **ERROR** section.

- **Initiate Bank Swap**

ACR[0]	Default : 0

Writing a one into this control bit requests an exchange of data between the Current and Update Coefficient Registers. The bank swap will occur as soon as the current computation cycle is completed, or on the next clock cycle if the IMSA100 is idle. This control bit is cleared to zero by the IMSA100 when the bank swap is complete. No access should be made to either set of coefficient registers while a bank swap is in progress. ACR[0] should not be set if SCR[2] is already set. For a detailed description of the behaviour see the bank-swap and coefficient access timing diagrams.

4.5 Test control register

- **Examine Full Output Word**

TCR[2]	Default: 0

This bit overrides the output word selection normally made by bits SCR[5–4]. The output word selection determines the 24 bit wide field selected from the 36 bit wide output of the multiply accumulator array (bit positions numbered 0 to 35). When TCR[2] is set to '1' the output word selection is bits '-1' to 22, where bit '-1' is set to zero. The output word selection should not be altered during data processing. If altered the data output of the cascade will be undefined until new input data has flushed through all stages of the cascade.

TCR[2]	Field
0	Set by SCR[5–4] *
1	[–1 to 22]

- **Reserved**

TCR[1]	Default: 0

This location is reserved for test purposes. For normal operation the user should write 0 to this location.

- **Reserved**

TCR[0]	Default: 0

This location is reserved for test purposes. For normal operation the user should write 0 to this location.

5. DEVICE APPLICATIONS

The IMS A100 can be used in a variety of different applications requiring high performance computation. Some of these are described below, and are covered in detail in the IMS A100 Application Note series.

5.1 Filtering and adaptive filtering

The IMS A100 device can be used to implement high speed FIR and IIR digital filters. The maximum sampling frequency of the input signal ranges between 2.125MHz and 15MHz, depending on the coefficient word length and speed variant that has been selected.

The continuous bank swap mode allows a single device to filter complex (I & Q) data streams. High speed random access coefficient registers enable high performance adaptive filters and equalisers to be realised with minimal complexity.

The cascadability of the device enables FIRs of greater than 32 stages to be constructed, with no degradation in data throughput.

5.2 Convolution and correlation

The IMS A100 is the first single-chip digital correlator capable of highly accurate computation of correlation and convolution functions (16-bit coefficients, 16-bit data and 36-bit accumulation). These functions have applications in matched filtering, noise reduction and pulse compression in communication, radar and sonar systems. For correlations and convolutions involving a large number of data points, devices can be cascaded to several thousand stages with careful design. Alternatively, it is possible to use algorithms which allow decomposition of long correlation and convolutions into several smaller ones, which can then be carried out by a single or smaller number of devices.

5.3 Matrix multiplication

The architecture of the IMS A100 allows very high speed fixed point matrix multiplication. In this application the columns of the multiplier matrix are circulated as inputs to the chip while the coefficients are programmed in a suitable manner with the elements of the multiplicant matrix. Larger matrices can be handled by either cascading several chips or by decomposing the matrices into smaller ones.

5.4 Fourier transforms

Two algorithms, namely the Prime Number Transform (PNT) and the Chirp-Z Transform (CZT), can be used to perform high speed Fourier transforms using IMS A100s. The Fourier transform of long data sequences can be evaluated either by using cascaded IMS A100s or by using decomposition algorithms to convert a long transform into a number of short transforms (e.g. <32 points). These short transforms can then be carried out using the IMS A100s and a host processor.

The speed of transform can be traded off against the number of chips employed. Any microprocessor with a standard memory interface could be used to handle intermediate results and to control the overall system. Two IMS A100s can be used to perform a transform of about 1000 points in around

1ms to 2ms using look-up ROMs for address generation and high speed DSP controllers, or 5ms to 10ms using a microprocessor as the controller. More IMS A100s can be used if higher performance is required.

5.5 Waveform synthesis

The programmability of this digital transversal filter allows the IMS A100 to be used for flexible waveform generation and synthesis, by exploiting the ability to change coefficients randomly, quickly and simply. Such a configuration could be attractive for PC based synthesisers, as the chip can generate very accurate high bandwidth signals.

5.6 General purpose accelerator

By attaching one or more IMS A100s to any computer with DMA capability, a useful accelerator can be constructed, capable of handling all of the above applications without reconfiguration. The cascadability of the device enables users to add IMS A100s as required for extra processing performance, with minimal impact on the driving software.

6. ELECTRICAL SPECIFICATION

The IMS A100 is available in several temperature variants and the electrical characteristics of each are described in this section. When no variant is identified the information refers to all variants.

6.1 DC electrical characteristics

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Units	Note (1)
V_{CC}	DC supply voltage	0		7.0	V	2,3
V_I, V_O	Voltage on input and output pins	-1.0		V_{CC}+0.5	V	2,3
T_{stg}	Storage temperature	-65		150	°C	2
T_A	Temperature under bias	-55		125	°C	2
P_{Dmax}	Power dissipation			2.0	W	2

Notes

1 All voltages are with respect to **GND**.

2 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedence circuit. Unused inputs should be tied to an appropriate logic level such as V_{CC} or **GND**.

DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
V_{CC}	DC supply voltage	4.5 4.75		5.5 5.25	V V	4 5
V_{IH}	Input Logic '1' Voltage CLK	4.0		V_{CC}+0.5	V	2
	Input Logic '1' Voltage $\overline{RESET}$	2.4		V_{CC}+0.5	V	2
	Input Logic '1' Voltage other pins	2.0		V_{CC}+0.5	V	2
V_{IL}	Input Logic '0' Voltage { CLK}	-0.5		0.5	V	2
	Input Logic '0' Voltage $\overline{RESET}$	-0.5		0.8	V	2
	Input Logic '0' Voltage other pins	-0.5		0.8	V	2
T_A	Ambient Operating Temperature	0 -40		70 85	°C °C	3,4 3,5

Notes

1 All voltages are with respect to **GND**. All **GND** pins must be connected to **GND**.
2 Input signal transients up to 10 ns wide, are permitted in the voltage ranges (**GND** - 0.5 V) to (**GND** - 1.0 V) and $\mathbf{V_{CC}}$ + 0.5 V to $\mathbf{V_{CC}}$ + 1.0 V.
3 400 linear ft/min transverse air flow.
4 IMS A100-G21S.
5 IMS A100-G21I

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2)
V_{OH}	Output Logic '1' Voltage	2.4		V_{CC}	V	4
V_{OL}	Output Logic '0' Voltage	0		0.4	V	5
I_I	Input current @ GND<VI<VCC			±10	μA	
I_{OZ}	Tristate output current @ $GND<V_I<V_{CC}$			±10	μA	
I_{CC}	Average power supply current			360	mA	3

Notes

1 All voltages are with respect to **GND**.All **GND** pins must be connected to **GND**.
2 Parameters measured over variants full voltage and temperature operating range.
3 Power dissipation is application dependent and varies with output loading. The maximum given here is for worst case data patterns and activity on all interfaces, with no DC load on outputs.
4 **OUTRDY**, $\mathbf{D_{OUT}}$: $\mathbf{I_{OUT}} \leq$ -4.4 mA; **$\overline{\text{ERROR}}$** is open collector; other outputs: $I_{OUT} \leq$ -5.5 mA.
5 **OUTRDY**, $\mathbf{D_{OUT}}$: $\mathbf{I_{OUT}} \leq$ 4.4 mA; $\overline{\text{ERROR}}$: $\mathbf{I_{OUT}} \leq$ 5.5 mA; other outputs: $\mathbf{I_{OUT}} \leq$ 5.5 mA.

CAPACITANCE

Pin	Min.	Typ.	Min.	Units	Notes
CLK		12		pF	1,2
All other pins		5		pF	1,2

Notes

1 This parameter is supplied for engineering guidance and is not guaranteed.
2 T_A = 25°C , f=1MHz.

6.2 Thermal Characteristics

PIN GRID ARRAY THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Typ.	Max	Units	Notes
θ JA	Junction to ambient thermal resistance			35	°C/W	1,2

Notes

1 Measured at 400 linear ft/min transverse air flow.
2 This parameter is sampled and not 100% tested.

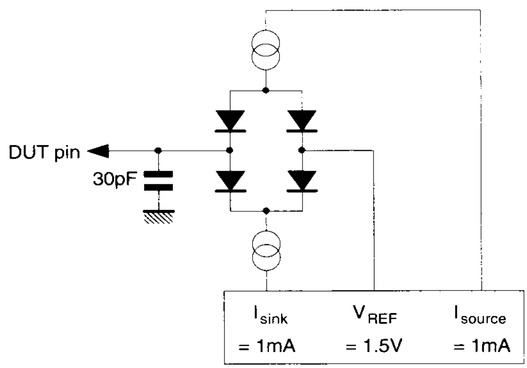
6.3 AC Timing Characteristics

AC TEST CONDITIONS

Output loads (except output turn-off tests)

Pin	Device mode	Load	Unit
GO	Master	20	pF
DOUT, OUTRDY	Fast output	15	pF
DOUT, OUTRDY	Normal output	30	pF
All other outputs	All modes	30	pF

Figure 6 : Output Load (Output Turn-Off tests)



TIMING REFERENCE LEVELS

Pin	Reference levels	Notes
INPUTS	0.8V, 2.0V	1
CLK	0.5V, 4.0V	
OUTPUTS	0.4V, 2.4V	2,3
OUTPUTS	±100mV change from previous steady output voltage	4

Notes

1 Except **CLK**.
2 Output continuously driven.
3 Timings are tested using VOL=0.8V and with a suitable allowance for the time taken for the output to fall from 0.8V to 0.4V
4 Output turn-off tests.

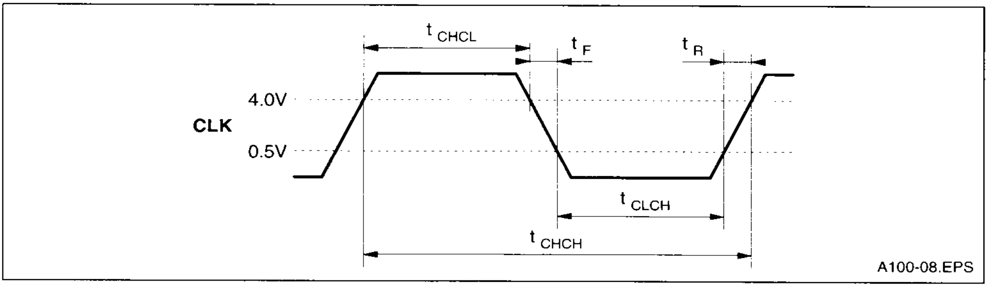
CLOCK

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{CHCL}	Clock pulse width high	19			ns	
t_{CLCH}	Clock pulse width low	19			ns	
t_{CHCH}	Clock period	48			ns	
t_R	Clock rise time	0		50	ns	1
t_F	Clock fall time	0		50	ns	1

Note :

1 Clock input transitions should be monotonic between the input thresholds of 0.5 V and 4.0 V.

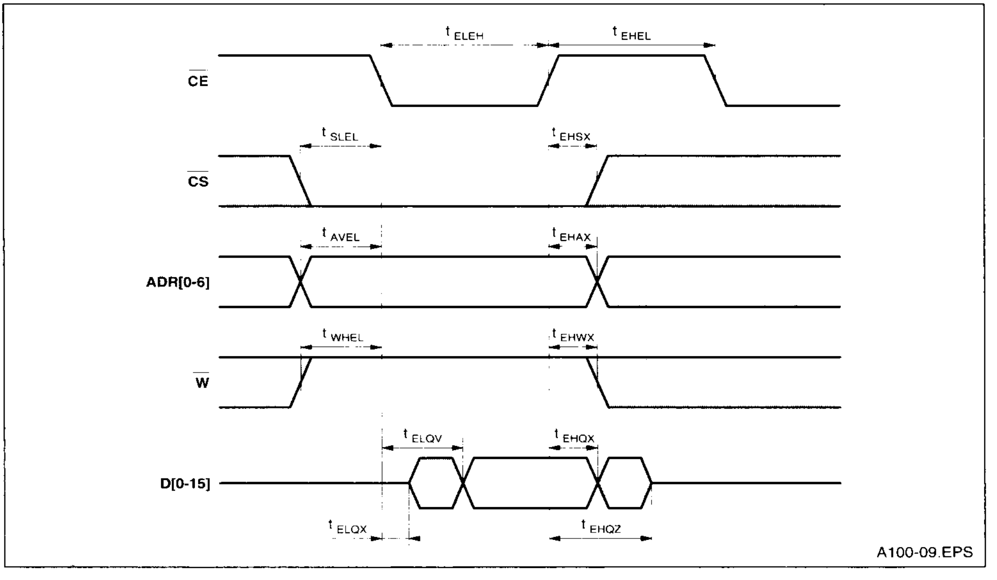
Figure 7



MEMORY INTERFACE READ CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{ELEH}	$\overline{CE}$ pulse width low	60			ns	
t_{EHEL}	$\overline{CE}$ pulse width high	50			ns	
t_{SLEL}	$\overline{CS}$ setup time	15			ns	
t_{EHSX}	$\overline{CS}$ hold time	5			ns	
t_{AVEL}	Address setup time	15			ns	
t_{EHAX}	Address hold time	5			ns	
t_{WHEL}	Read Command setup	15			ns	
t_{EHWX}	Read Command hold	5			ns	
t_{ELQX}	Output turn on delay	0			ns	
t_{ELQV}	Read data access			60	ns	
t_{EHQX}	Read data hold	0			ns	
t_{EHQZ}	Output turn off delay			25	ns	

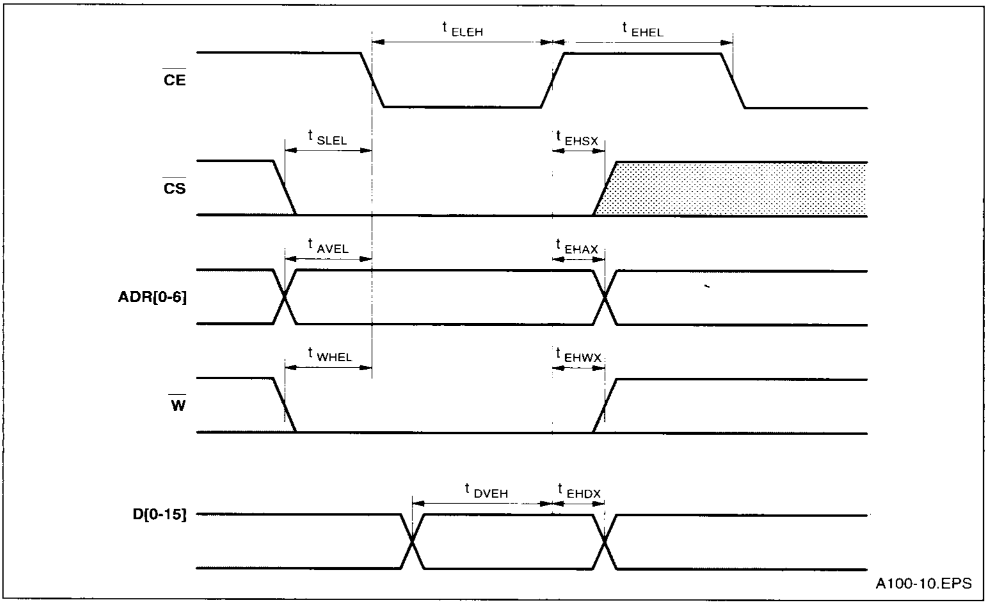
Figure 8



MEMORY INTERFACE WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{ELEH}	$\overline{CE}$ pulse width low	50			ns	
t_{EHEL}	$\overline{CE}$ pulse width high	50			ns	
t_{SLEL}	$\overline{CS}$ setup time	15			ns	
t_{EHSX}	$\overline{CS}$ hold time	5			ns	
t_{AVEL}	Address setup time	15			ns	
t_{EHAX}	Address hold time	5			ns	
t_{WLEL}	Write Command setup	15			ns	
t_{EHWX}	Write Command hold	5			ns	
t_{DVEH}	Write data setup	45			ns	
t_{EHDX}	Write data hold	5			ns	

Figure 9



STATIC READ ACCESSES TO DOL AND DOH REGISTERS

Certain applications require to read results from the IMS A100 at high speeds. To ensure full system performance it may be necessary to read results from the DOL and DOH registers using a continuous 'static' access rather than using the normal clocked access.

During static access the $\overline{CE}$ signal is held low continuously. Under this condition it is possible to monitor either DOL or DOH continuously to observe new output words as they become available or alternatively to switch between DOL and DOH without the restriction of having to sequence $\overline{CE}$.

Symbol	Parameter	Min	Typ.	Max	Units	Notes
t_{AVQV}	Address access time			75	ns	1
t_{CHQV}	Data input access time			τ+75	ns	2
t_{ELQV}	$\overline{CE}$ access time			60	ns	3
t_{AXQX}	Data hold after address change	0			ns	
t_{CHQX}	Data hold after new data input	τ+0			ns	2
t_{EHQX}	Data hold after end of read	0			ns	

Notes

1 The address access time is specified for address transitions between decimal 74 (DOL register) and decimal 75 (DOH register) only.

2 The parameter τ describes the time taken from the input of a data word to that data word first affecting the most significant word (MSW) output. This is the time at which the DOL and DOH registers are updated.
The duration of τ depends on the coefficient size selected and whether fast or normal output is selected.

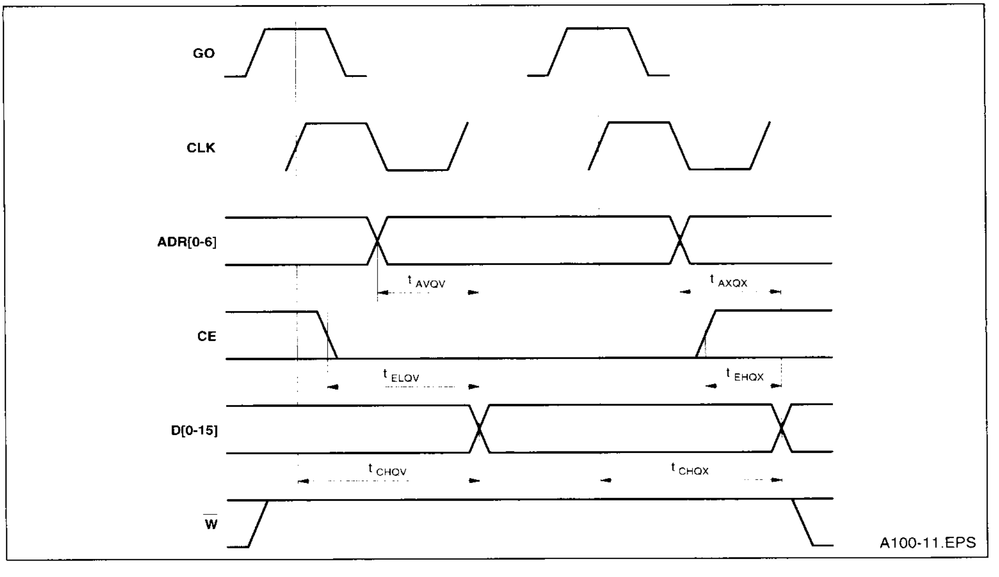
Coefficients	Output mode	τ time
4 bit	Fast	8 CLK cycles
8 bit		10 CLK cycles
12 bit		12 CLK cycles
16 bit		14 CLK cycles

Coefficients	Output mode	τ time
4 bit	Normal	Not defined
8 bit		11 CLK cycles
12 bit		14 CLK cycles
16 bit		17 CLK cycles

N.B. The data value read from either DOL or DOH will change as new results are computed by the device.

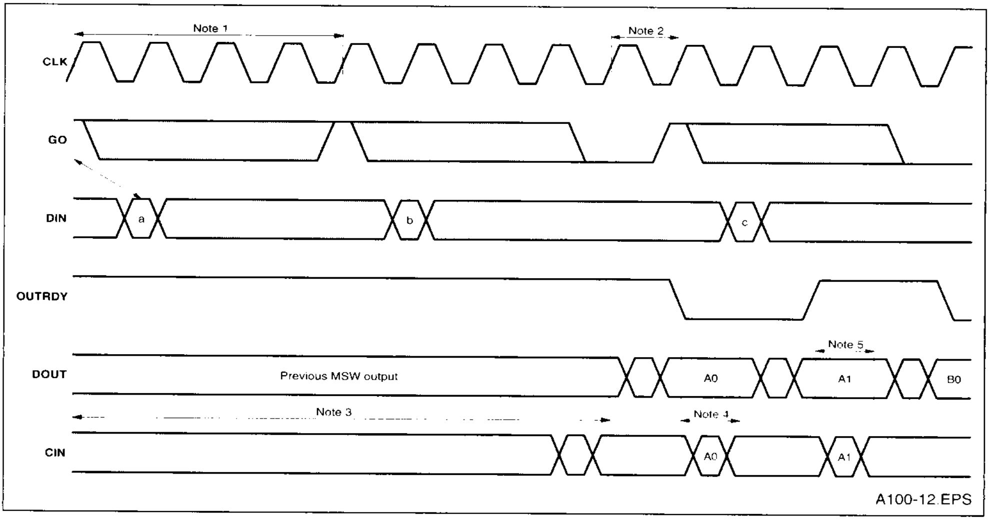
3 This parameter is the normal read access time for reading any register through the microprocessor interface. In the special case of performing reads from only DOL and DOH any number of reads from these registers can be made with $\overline{CE}$ held low continuously.
It is required that a static access (as described above) should commence like a normal clocked, random, read access to either DOL or DOH. That is **ADDRESS**, $\overline{CS}$ and $\overline{W}$ should be established with setup times to $\overline{CE}$ specified for a normal read access.
During a DOL/DOH static access sequence accesses to locations other than DOL and DOH are undefined.

Figure 10



TYPICAL SEQUENCE - 8 BIT COEFFICIENTS, NORMAL OUTPUT

Figure 11



Notes

1 The minimum period between sampling the **GO** input is four clock cycles for 8 bit coefficients, see the table below for the other cases.

2 After the minimum period described in note 1 has elapsed **GO** is sampled on every rising edge of **CLK** until **GO** is high.

3 The delay from an output being initiated by **GO** to the output completing its previous output sequence and starting the new output sequence is 8 clock cycles for 8 bit coefficients, see the table below for the other cases.

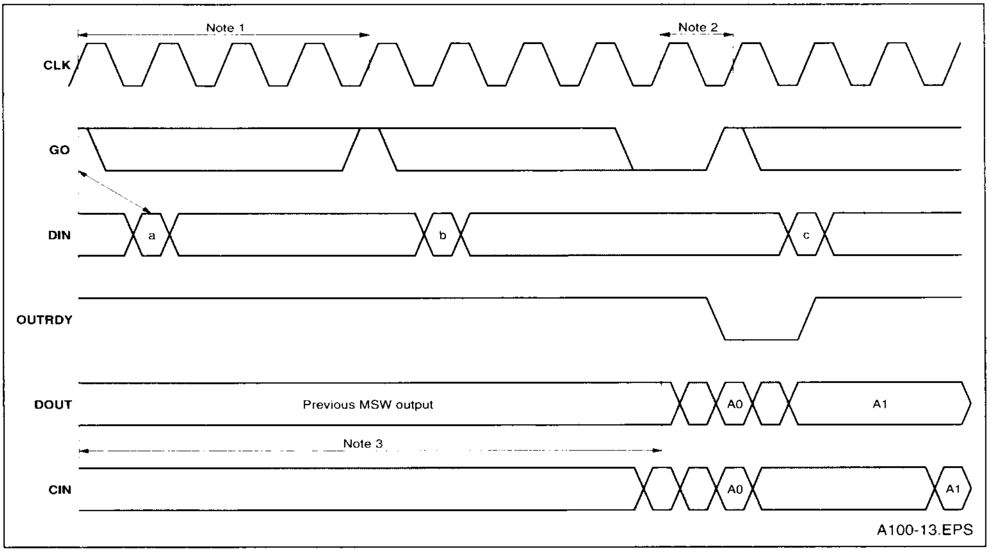
4 The least significant word is available at the output across one complete **CLK** cycle for the 8 bit coefficient, normal output case, see the table below for the other cases.

5 The most significant word is available for the minimum period described in note 4, but will be extended by a clock cycle for each additional idle cycle inserted between data inputs.

Coefficients	Min. Output Period note 1	Delay To Output note 3	Min. LSW Output Duration notes 4 and 5
4 bit	2 CLK cycles	6 CLK cycles	Undefined. no normal output
8 bit	4 CLK cycles	8 CLK cycles	1 CLK cycle
12 bit	6 CLK cycles	10 CLK cycles	2 CLK cycles
16 bit	8 CLK cycles	12 CLK cycles	3 CLK cycles

TYPICAL SEQUENCE - 8 BIT COEFFICIENTS, FAST OUTPUT

Figure 12



Notes

1 The minimum period between sampling the **GO** input is four clock cycles for 8 bit coefficients, see the table below for the other cases.

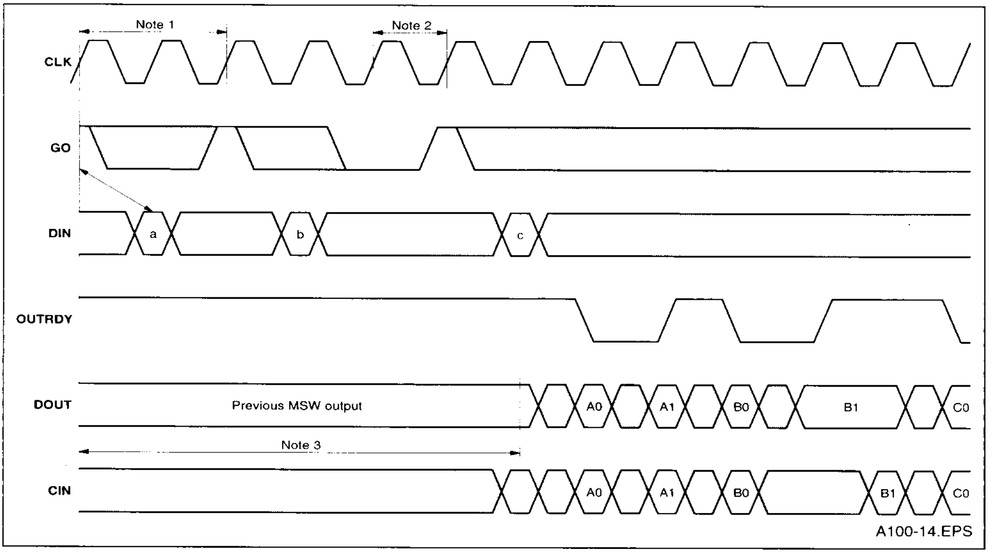
2 After the minimum period described in note 1 has elapsed **GO** is sampled on every rising edge of **CLK** until **GO** is high.

3 The delay from an output being initiated by **GO** to the output completing its previous output sequence and starting the new output sequence is 8 clock cycles for 8 bit coefficients, see the table below for the other cases.

Coefficients	**Min. Output Period** note 1	**Delay To Output** note 3
4 bit	2 CLK cycles	6 CLK cycles
8 bit	4 CLK cycles	8 CLK cycles
12 bit	6 CLK cycles	10 CLK cycles
16 bit	8 CLK cycles	12 CLK cycles

TYPICAL SEQUENCE - 4 BIT COEFFICIENTS

Figure 13



Notes

1 The minimum period between sampling the **GO** input is two clock cycles for 4 bit coefficients, see the table below for the other cases.

2 After the minimum period described in note 1 has elapsed **GO** is sampled on every rising edge of **CLK** until **GO** is high.

3 The delay from an input being initiated by **GO** to the output completing its previous output sequence and starting the new output sequence is 6 clock cycles for 4 bit coefficients, see the table below for the other cases.

Coefficients	Min. Output Period note 1	Delay To Output note 3
4 bit	2 CLK cycles	6 CLK cycles
8 bit	4 CLK cycles	8 CLK cycles
12 bit	6 CLK cycles	10 CLK cycles
16 bit	8 CLK cycles	12 CLK cycles

NORMAL OUTPUT TIMING–8 BIT COEFFICIENT CASE SHOWN

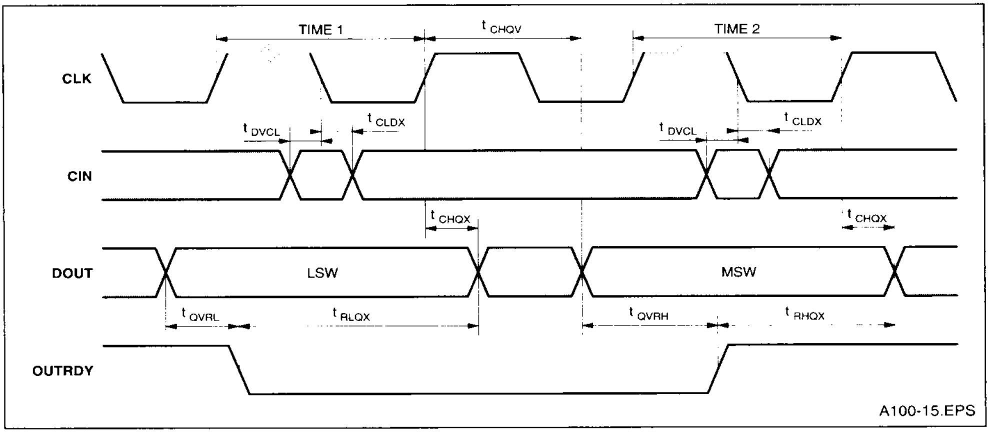
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{CHQV}	CLK high to DOUT valid delay			36	ns	
t_{CHQX}	DOUT hold time after CLK high	2			ns	
t_{QVRL}	DOUT to OUTRDY low lead	15			ns	
t_{RLQX}	DOUT hold time after OUTRDY low	10			ns	1
t_{QVRH}	DOUT to OUTRDY high lead	15			ns	
t_{RHQX}	DOUT hold time after OUTRDY high	10			ns	1,2
TIME1	LSW output duration	1		3	t_{CHCH}	1
TIME2	MSW output duration	1		3 ,t_{CHCH}	1,2	
t_{DVCL}	CASIN setup time to CLK low	10			ns	
t_{CLDX}	CASIN hold time from CLK low	10			ns	

Notes

1 This parameter is determined by the coefficient size in use. The minimum value given is correct for 8 bit coefficients. This parameter is extended by 1 (or 2) periods of **CLK** if 12 (or 16) bit coefficients are used. This mode of operation is not defined if 4 bit coefficients are used.

2 These parameters are extended by one tCHCH for each idle cycle inserted between data input sequences

Figure 14



FAST OUTPUT TIMING–4 BIT COEFFICIENT CASE SHOWN

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{CHQV}	CLK high to DOUT valid delay			36 22	ns ns	1 1
t_{CHQX}	DOUT hold time after CLK	2			ns	2
t_{QVRL}	DOUT to OUTRDY low lead				ns	
t_{RLQX}	DOUT hold time after OUTRDY low	10			ns	
t_{QVRH}	DOUT to OUTRDY high lead	5			ns	1
t_{RHQX}	DOUT hold time after OUTRDY high	10			ns	2
t_{DVCH}	CASIN setup time to CLK high	10			ns	
t_{CHDX}	CASIN hold time to CLK high	0			ns	3

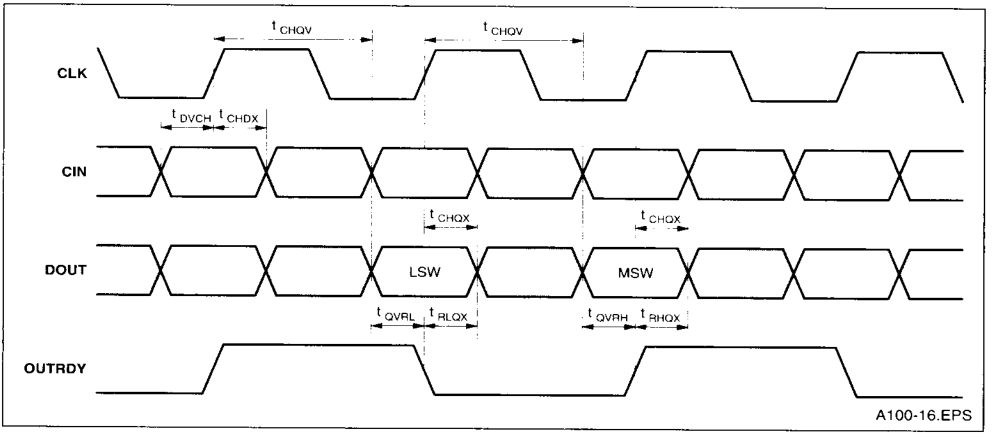
Notes

1 These parameters assume that each **DOUT** signal is loaded with a maximum of 15 pF.

2 t_{CHQX} and t_{RHQX} for the MSW are shown here for the case where 4 bit coefficients are being used. In the other cases (8, 12 and 16 bit coefficients) the MSW is available for an additional 2, 4 or 6 **CLK** periods. In all cases the MSW will be available for an additional period of **CLK** for each idle cycle inserted between data input sequences.

3 Not tested. Guaranteed by design.

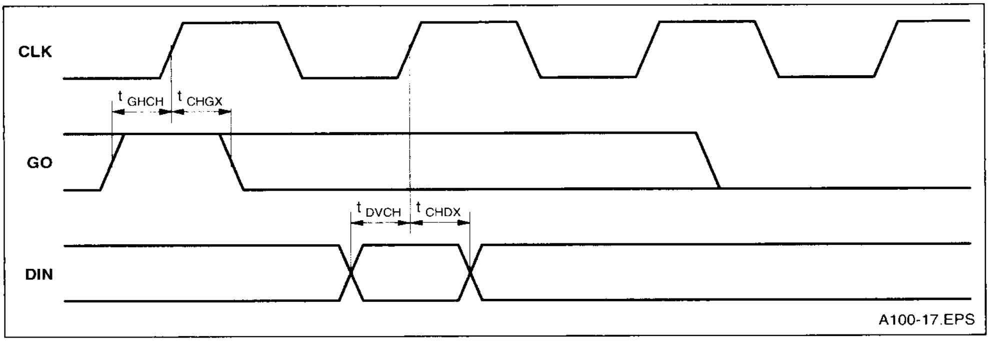
Figure 15



EXTERNAL GO AND DATA INPUT TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{GHCH}	GO setup time	10			ns	
t_{CHGX}	GO hold time	5			ns	
t_{DVCH}	DIN setup time	30			ns	
t_{CHDX}	DIN hold time	5			ns	

Figure 16



MASTER GENERATED GO

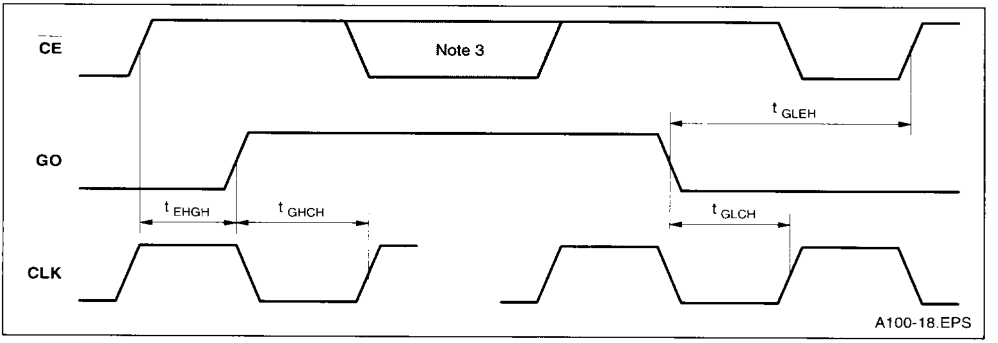
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{EHGH}	Write to DIR to GO high delay	25			ns	1
t_{GHCH}	GO high before GO sampled	10			ns	2
t_{GLEL}	GO low to write to DIR	0			ns	
t_{GLCH}	GO low before GO next sampled	10			ns	2

Notes

1 The maximum delay from a write to the DIR to **GO** going high is 2 * t_{CHCH} + 50 ns.

2 This parameter assumes the capacitive load on **GO** is less than 20 pF. **GO** is specified so that one master IMS A100 can drive three slave IMS A100s without buffering.

Figure 17



BANKSWAP TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{EHBH}	ACR[0] set to BUSY high delay			55	ns	
t_{CHBL}	BUSY hold after bankswap			50	ns	
t_{CHEH}	ACR[0]=0 hold after last input	20			ns	3
t_{EHCH}	ACR[0]=1 setup to next input	10			ns	3

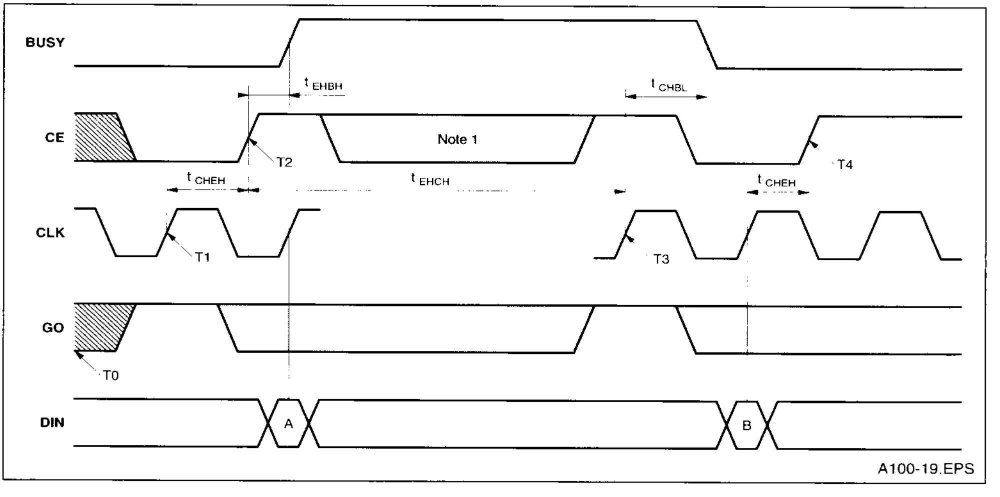
Notes

1 The activity on $\overline{CE}$ shown is for writing ACR[0]=1. During the period **Note 1** it may be possible to access other registers (subject to their own access constraints).

2 For small t_{EHCH}, **BUSY** may only occur for a short time or not occur at all.

3 If t_{CHEH} or t_{EHCH} is exceeded then bankswap may be synchronised to the previous or next input cycle.

Figure 18



The bankswap timing diagram shows how successive data samples (A and B) can be processed by different sets of coefficients by causing a bankswap to occur between the input of sample A and sample B.

The sequence of events is as follows:

T0 No bankswap pending.

T1 GO sampled and found to be high, thus initiating input of data sample A.

T2 Bankswap requested by writing ACR[0]=1. If the minimum timing requirement, t_{CHEH}, from T1 to T2 is not met it is possible (but not guaranteed) that the bankswap requested at T2 will occur immediately and thus affect the processing of data sample A.

T3 Bankswap occurs on the first rising edge of **CLK** upon which **GO** is sampled (without reference to the state of **GO**). If the minimum timing requirement, t_{EHCH}, from T2 to T3 is not met it is possible (but not guaranteed) that the bankswap requested at T2 will not occur at T3 but at the next sampling of **GO**.

T4 This is the earliest time at which another bankswap can be requested.

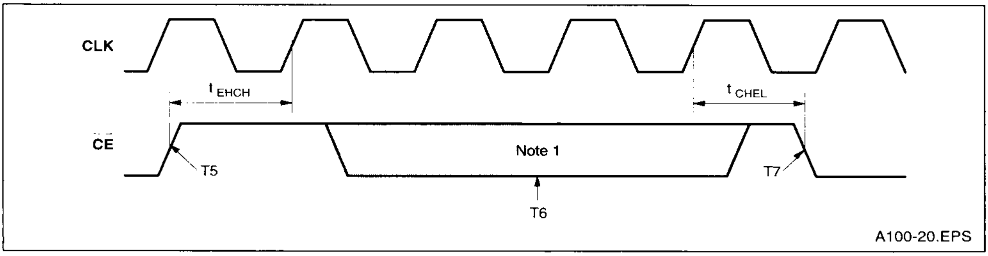
COEFFICIENT ACCESS TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{EHCH}	End coefficient access before bankswap	0			ns	
t_{CHEL}	Start coefficient access after bankswap	0			ns	

Notes

1 During this period accesses may be made to registers other than the coefficient registers (subject to their own access constraints).

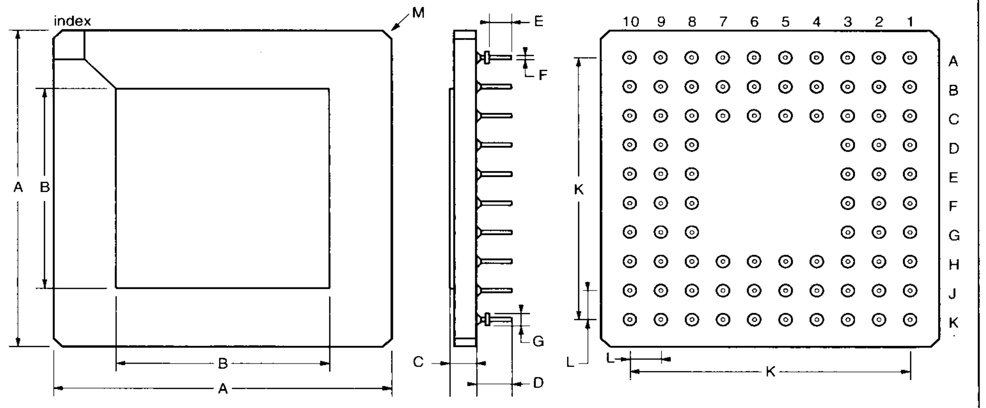
Figure 19



If a bankswap (caused by setting either ACR[0]=1 or SCR[2]=1) occurs at the **GO** sampling point T6, then no access should be made to the coefficient registers between T5 and T7.

PACKAGE MECHANICAL DATA

84 PINS - GRID ARRAY PACKAGE



DIM	Millimètres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	26.924	± 0.254	1.060	± 0.010	
B	17.019	± 0.127	0.670	± 0.005	
C	2.456	± 0.278	0.097	± 0.011	
D	4.572	± 0.127	0.180	± 0.005	
E	3.302	± 0.127	0.130	± 0.005	
F	0.457	± 0.025	0.018	± 0.001	Pin diameter
G	1.143	± 0.127	0.045	± 0.005	Flange diameter
K	22.860	± 0.127	0.900	± 0.005	
L	2.540	± 0.127	0.100	± 0.005	
M	0.508		0.020		Chamfer
Package weigth is approwimately 2.2 grams					

PGA84.TBL